

# Brief Overview of the Technical Status of the Run IIb Upgrade Project

DZero Collaboration  
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## Design Overview

The upgraded D0 silicon microstrip tracker (SMT) is designed to optimize the physics performance of the detector and builds upon the experience generated from the design and construction of many silicon detectors at the laboratory, most recently the silicon detectors for both collider detectors for Run IIa. This new detector will have sensors positioned closer to the interaction point than the current detector and has two additional layers of sensors for improved impact parameter resolution and enhanced b-tagging capability. The design of the detector satisfies various stringent boundary conditions. To expedite the construction of the detector and to minimize the shutdown time needed for installation, the design is modular and uses a minimum of different types of components. The detector also is designed to be installed inside the collision hall, without the D0 detector having to roll out into the assembly hall. To achieve this in-situ installation, no elements of the detector are supported from the beam pipe, and the upgraded silicon detector will leave the Silicon Detector Facility as two independent barrel assemblies that will be mated inside the D0 collision hall. Moreover, the readout of the detector has been arranged such that the total number of readout channels of the detector fits within the current cable plant and satisfies the symmetry requirements of the Silicon Track Trigger.

The detector consists of 2304 silicon sensors, designed to withstand the full radiation dose anticipated for Run II. The detector uses only single-sided silicon sensors, and only three types of sensors are employed. The detector has six layers of silicon in a barrel geometry, with the innermost layer at a radius of 18 mm from the beam centerline and the outermost layer at a radius of 163mm.

The sensors in the two innermost layers have strips aligned along the beam direction (axial), while the outer layers provide both axial and small-angle stereo measurements. The sensors on the innermost layer (Layer 0) have a 50  $\mu\text{m}$  readout pitch while the sensors on the second layer (Layer 1) have a 58  $\mu\text{m}$  readout pitch. The sensors used for the outer four layers (Layers 2 through 5) have a 60  $\mu\text{m}$  readout pitch. All sensors have intermediate strips. Layers 0 and 1 will be mounted directly on integrated carbon fiber support structures that have cooling tubes built into those structures. The sensors for Layers 2 through 5 will be mounted on assemblies known as staves that provide the mechanical support and cooling for these sensors. The six sensors on one side of a staff will be oriented with strips parallel to the beam while the six sensors on the opposite side of a staff will be mounted to achieve small-angle stereo measurements. Layers 2 through 5 are composed of a total of 168 such staves.

The readout of the silicon sensors employs 7440 SVX4 readout chips that have been jointly developed by LBL and Fermilab for CDF and D0. The SVX4 chip builds on the

previous generations of readout chips for the Fermilab collider detectors - the SVX, SVX2, and SVX3 chips. It uses 0.25  $\mu\text{m}$  technology and is intrinsically radiation hard. Each SVX4 chip instruments 128 readout strips. Each individual channel integrates the input charge from a silicon sensor strip and transfers the charge to a switched capacitor array for temporary buffering. When a Level 1 trigger is received, the SVX4 chip digitizes the appropriate charge and the digitized data are propagated through the data acquisition system.

The SVX4 chips will be mounted on ceramic hybrids. For the outer five layers, the hybrids will be mounted directly on the silicon sensors. Due to space and thermal constraints, the Layer 0 sensors will be connected to ceramic hybrids via fine-pitch, low-mass, flexible printed circuits referred to as analog cables. There are four types of hybrids: Layer 0 hybrids, Layer 1 hybrids, Outer Layer Axial hybrids and Outer Layer Stereo hybrids. These thick-film ceramic hybrids are fabricated on Beryllia substrates and have six conductor layers and five dielectric layers on the top side. The top layer features pads that must be solderable as well as pads that must be wire-bondable.

Digital signals are transferred to and from the hybrids through passive Junction Cards positioned just outside the sensor volume and flexible circuits called Digital Jumper Cables, which can be up to 1m in length. The signals are transferred between the Junction Cards and active Adapter Cards (located on the ends of the Central Calorimeter) via  $\approx$ 8-foot-long Twisted Pair Cables. The Adapter Cards provide voltage regulation and signal translation. Signals are transferred between the Adapter Cards and Interface Boards located in the cathedral (along the sides of the Central Calorimeter) via  $\approx$ 19-foot-long 80-conductor shielded 3M cables. Signals are transferred between the Interface Boards and Sequencers (located on the platform beneath the D0 detector) using 50-conductor 3M cable. From there, the signals are transferred via optical fibers to readout buffers in the Movable Counting House.

To minimize the commissioning time and reduce costs, the SVX4 chip will be readout in SVX2 mode so that the higher level readout of the upgraded detector can rely upon the Sequencers, Sequencer Controllers, VME Readout Buffers, and VME Readout Buffer Controllers currently in use in Run IIa to generate the necessary control signals and coordinate and control the readout and higher level buffering of the data.

## **Status**

The detector design is essentially complete, and the prototyping phase is nearing completion. A summary of the status of various components is shown in Figure 1. Details are provided below.

### ***Sensors***

Prototype versions of the three silicon sensor types were specified, designed, ordered, produced, probed, and tested during 2002 and through early 2003. Some of the prototype sensors also were subjected to detailed irradiation tests to ensure that they will withstand the anticipated radiation doses. The prototype sensors manufactured by Hamamatsu were of very high quality, exhibiting very few defects.

Prototype sensors also have been used to prepare, refine, and certify our sensor Quality Assurance equipment and procedures, and to train personnel in anticipation of the delivery of the first production sensors.

The sensors for layers 2 through 5 represent the largest single procurement of the D0 silicon upgrade project. A Production Readiness Review with external committee members carefully reviewed the performance of the prototype sensors and the QA program, and the order for production of the outer layer sensors was released on 17 April 2003. On 1 August 2003, we received the first 130 production sensors from Hamamatsu, on schedule. We currently are evaluating these sensors, and initial results look encouraging. Recently, the order for the inner layer sensors, which will receive large radiation doses, was reviewed and the project is preparing the release of that order.

### ***SVX4***

The first full prototype version of the SVX4 readout chip was received in June 2002, and chips have been tested and mounted on hybrids. Some hybrids were mounted on prototype silicon sensors and are routinely employed in testing. Although this first pre-production version of the readout chip was fully functional and could be used in the experiment, there were a few undesirable features, such as a non-uniformity of the pedestal from channel to channel, which were addressed. A second version of the SVX4 chip was designed, and a full pre-production run of 24 wafers was submitted in April and received on 16 May 2003. Initial results from the testing of these new SVX4 chips are very encouraging. The yield is quite high and no undesirable features have been observed. The project is completing its testing of the chip, and official sign-off and release for production is anticipated to occur within the next month.

### ***Hybrids***

Prototypes of all four versions of the ceramic hybrids have been designed, fabricated, and tested. SVX4 chips have been surface-mounted for all four versions. The hybrids also were mounted on sensors to study readout performance. All four types of hybrids have been successfully read out, and the noise performance was found to be excellent. Pre-production versions of all the hybrid types have been designed, and the outer-layer pre-production hybrids are currently being fabricated.

### ***Cables and Cards***

The analog cables which carry the analog signals from the Layer 0 sensors to the readout hybrids are technically very challenging. The length of the cables, the small trace width, the requirements to minimize mass and overall load capacitance are all features that make these cables very hard to manufacture. Our prototyping efforts on these cables have been extremely successful. The project has gone through four sets of prototype cables and the last set received was both mechanically and electrically flawless. The cables were used in the construction of full-scale Layer 0 modules, equipped with the pre-production version of the Layer 0 hybrid, and the modules met all our electrical and noise requirements. A few details, like the exact length of the cable and options to further minimize the load capacitance, are still being studied.

Prototypes of the Digital Jumper Cable, which are used in the test stands, have been fabricated and testing is in progress. The prototype version of the Junction Card has been designed, and the printed circuit boards are being fabricated. This version of the Junction Card is expected to be available by late summer. Prototypes of the twisted-pair cables have been designed and fabricated. A prototype Adapter Card was fabricated, and a pre-production version of the bare board was completed. The first pre-production Adapter Card board has been stuffed and its functionality is under test.

### ***Mechanical Structures***

A prototype version of the carbon-fiber support structures for the Layer 0 and 1 sensors has been designed and tests of the performance of prototype modules on those support structures were performed to evaluate details of the grounding to minimize noise. All mechanical and thermal Finite Element Analyses of these support structures are complete, and fabrication of a pre-production support structure with co-bonded flex-circuits for grounding is in progress.

A mechanical version of the stave has been produced and evaluated. The first electrical-grade stave is being produced, and the sensors on the axial side of the stave have been read out. The carbon-fiber support structures for the staves are also being prototyped. Positioning bearings have been accurately placed on a prototype bulkhead.

### ***Quality Assurance and Testing***

The Quality Assurance process for the construction of the upgraded silicon detector calls for a rigorous testing program. Each part, sub-assembly and module will be subjected to rigorous testing. Most of the testing during fabrication will be performed with so-called "burn-in" test stands. All burn-in test stands needed for hybrid and module burn-in have been erected at the Silicon Detector Facility and are operational. A special-purpose card referred to as the Purple Card is used at this stage in the testing. This card has been designed, fabricated, and installed at these burn-in test stands. These burn-in test stands have been assembled and reviewed, and are fully functional. They have been reviewed by Fermilab Safety Management and are certified for round-the-clock operation. Long-term tests of hybrids have begun. A laser test stand and debugging stations also have been set up and are operational.

The hardware necessary to perform a full system test in the readout configuration, identical to the one employed at D0 during collider operation, is installed at the Silicon Detector Facility and is being debugged. The software needed to support this test system and to integrate the upgraded detector into the D0 system also is being developed. This system setup is being used to test all aspects of running the detector, including operating the new low-voltage power supplies, storage and retrieval of calibration constants, and monitoring of all vital parameters of the detector. These new power supplies will be installed in the Movable Counting House at D0 rather than inside the collision hall, providing improved accessibility and serviceability, but requiring long-distance remote sensing. This also will be tested using the test stand now being developed at the Silicon Detector Facility. The high-voltage supplies also have also been ordered and are being delivered.

### ***Monitoring Systems and Software***

Prototypes of the temperature monitoring and radiation monitoring systems are under development and testing has begun. Monitoring software also is being written in preparation for the full-scale testing effort. Database development for detector production, commissioning, and operation also has started. The database being used is an Oracle database, built on the database design used by the ATLAS experiment.

### ***Summary***

Good progress has been made on all hardware and software. All components of the upgraded silicon detector design have been prototyped. Pre-production versions of most components are in progress. No major unresolved technical issues remain, and the project has started placing final production orders for components. The project continues to make steady progress, and currently is projected to be ready for installation in the collision hall by early December 2005.

A strong, knowledgeable, experienced, and very dedicated team is working hard to build an upgraded silicon detector which will significantly increase the physics capabilities of the D0 detector for Run IIb.

Component	Vendor	First Prototype		Second Prototype		Final		
		Design	Ordered	Delivered	Ordered	Delivered	Order	Delivered
L0 Sensors	ELMA	✓	✓	✓				
	HPK	✓						
L1 Sensors	ELMA	✓	✓	✓				
	HPK	✓	✓	✓				
L2 Sensors	HPK	✓	✓	✓			✓	in progress
Analogue Cable	Dycx	✓	✓	✓	✓	✓		
L0 Hybrid	Amitr.	✓	✓	✓	✓			
L1 Hybrid		✓	✓	✓				
L2A Hybrid	CPT	✓	✓	✓	✓			
	others	✓	✓	✓	✓			
L2S Hybrid		✓	✓	✓	✓			
Digital Cable	Honey	✓	✓	✓	✓	✓		
	Basic	✓	✓	✓	✓	✓		
Junction Card		✓	✓	✓	✓			
Twisted Pr. Cable		✓	✓	✓	✓	✓		
Adapter Card		✓	✓	✓	✓	partial		
Purple Card		✓	✓	✓	✓	✓	✓	✓
Test Stand Elctr.		✓	✓	✓			✓	✓

Figure 1 – Major component status summary for the upgraded D0 silicon detector

### **D0 Run IIb Trigger Progress**

The Run IIb upgrades to the D0 trigger system began with a task force study in the Summer of 2001. From that study, a carefully targeted set of five upgrades were selected for implementation: a new Level 1 Calorimeter Trigger (L1Cal), an enhancement to the Level 1 Central Track Trigger (CTT) to use finer granularity, the addition of a Level 1

Calorimeter-Track matching system (L1 Cal-track), a processor upgrade for the Level 2 Beta System, and an expansion of the Level 2 Silicon Track Trigger (STT) to take advantage of the new SMT geometry. A collaboration of approximately twenty university and laboratory groups was assembled to pursue these upgrades, and work on prototype designs began in earnest early in 2002. Since that time, enormous technical progress has been made in the trigger upgrades.

### ***L1Cal***

The most extensive upgrade is the new L1Cal, and this is the system that is most advanced. Full prototypes have been designed, laid out, fabricated, and assembled for almost all of the major electronics boards of the system: the ADC-Digital Filter card (ADF), made by the Saclay group, and the Trigger Algorithm Board (TAB) and VME-Serial Command Link interface (VME/SCL) made by the Columbia/Nevis group. These prototypes currently are undergoing bench testing, and no major problems have been discovered. In addition, in July 2003, we began a prototype integration test at D0 that tests the boards with real control signals from the trigger framework. The same area established for these tests (with special power, grounding, and network requirements) will serve to commission the full L1Cal system in parallel with the existing L1Cal before the shutdown for silicon installation. Special analog splitters have been made and tested which can split the input signals from the calorimeter so that they can be used concurrently by the existing L1Cal and the new L1Cal.

### ***Central Track Trigger***

The CTT upgrade requires only the replacement of 80 daughter cards, known as DFEAs, in the current CTT system. The new DFEAs will contain the larger FPGAs required for selecting tracks based on individual fiber hits in each layers, rather than pairs of fibers. Extensive simulation work was done to obtain sets of equations that would select tracks efficiently and accommodate the as-built geometry of the fiber tracker, fiber hit inefficiency, the high rate of multiple interactions expected in Run 2b, and variations in the beam position. The firmware for the target algorithm was fully coded by an engineer at Boston University, and tested with FPGA simulation tools. Based on the successful firmware design, a new DFEA layout has begun and FPGAs have been procured for the preproduction boards.

### ***L1 Cal Track***

The L1 Cal-Track is being built by the Arizona group, and it leverages their design of successful L1 muon trigger for Run IIa. All of the L1 Cal-Track electronics are essentially clones of L1 muon cards, with the exception of one daughter card called the Universal Flavor Board (UFB). The design and layout of the UFB are complete and a prototype board is currently being fabricated. In addition, procurement is well advanced for many of the components for the other boards and infrastructure items such as cables, crates, and power supplies. The cables are scheduled to be installed during the upcoming Fall '03 accelerator shutdown. A production readiness review of this system was held recently, and the reviewers agreed that the production the system could begin upon completion of prototype testing.

### ***L2 Beta and Silicon Track Trigger***

The Level 2 upgrades generally require much less time and effort than the Level 1 upgrades. Some procurements have been made for the STT upgrade, but most of the activity is not scheduled until FY04. The purchase of the new processors for the L2 Beta upgrade is intentionally scheduled to be near the end of Run IIa in order to benefit from the performance/cost evolution of commercial processors.

### ***Summary***

Overall, the trigger upgrades are more than one-third complete, in terms of budgeted cost of work performed, including all sources of funding (NSF MRI, R&D funds, DOE equipment, and foreign and university in-kind contributions). All of the upgrades are on track for timely completion well in advance of the shutdown for silicon installation in late 2005.

We have recently reviewed the installation plan for the trigger upgrades. This led us to the conclusion that these upgrades can be installed without an extensive shutdown period.