

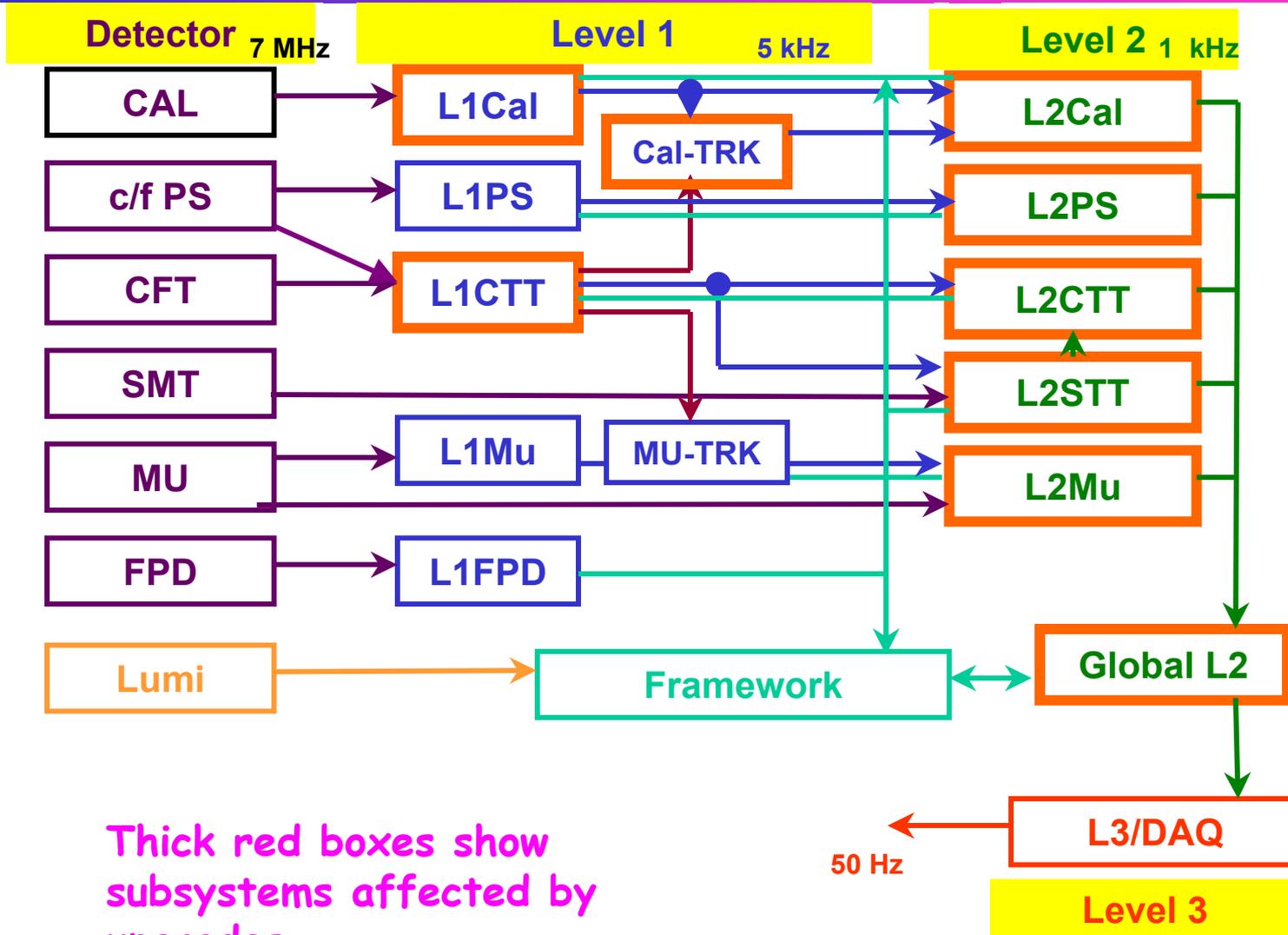


DØ Trigger Upgrade

Paul Padley, Rice Univ.
for the DØ Trigger Upgrade Group



The Run IIb Trigger System



Thick red boxes show subsystems affected by upgrades



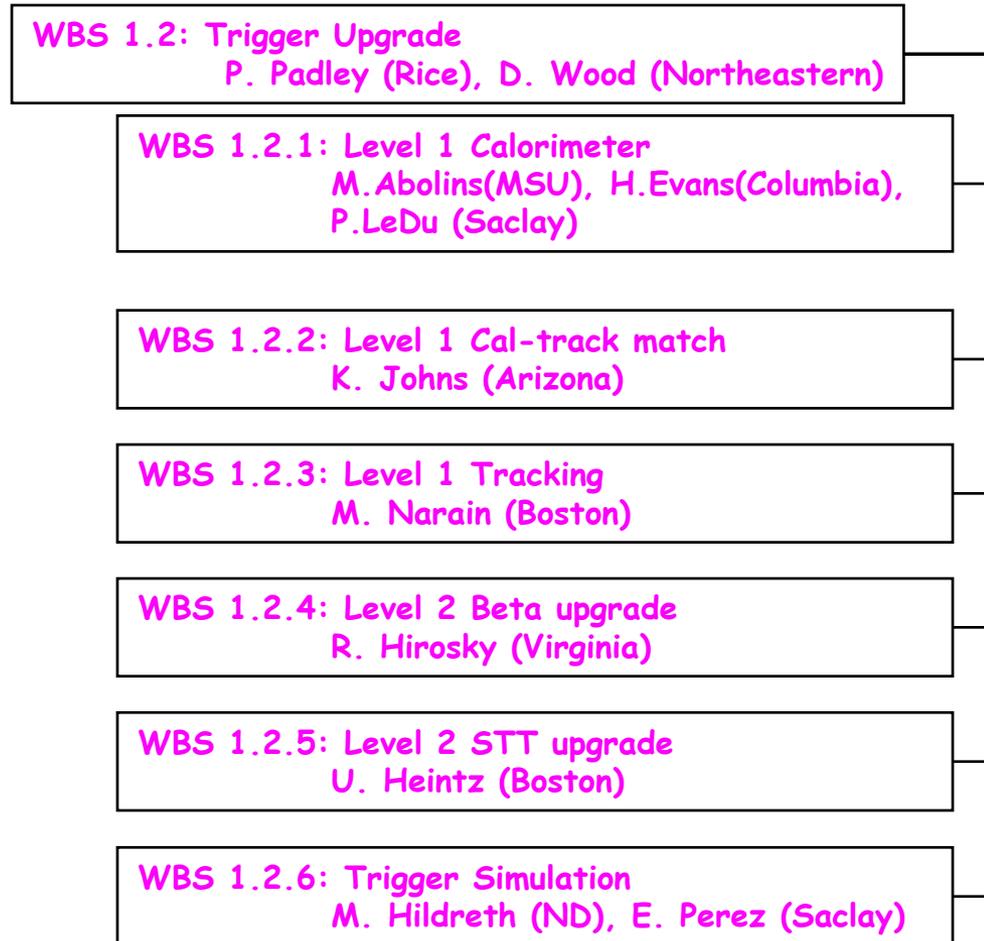
Strategies for Trigger Upgrades

- Run efficient high- p_T trigger menu at $L=2e32$ @ 396 ns
 - ◆ allow headroom for running at $L>2e32$
 - ◆ allow capability of 132 ns operation (probably not needed)
- Increase trigger rejection at Level 1
 - ◆ 1.2.1: L1 Calorimeter trigger upgrade to sharpen thresholds
 - ◆ 1.2.2: Additional rejection from cal-track matching
 - ◆ 1.2.3: L1 Tracking trigger upgrade to maintain rejection
- Combat backgrounds at Level 2
 - ◆ 1.2.4: L2 Processor upgrades \Rightarrow more complex algorithms possible
 - ◆ 1.2.5: Expand Silicon Track Trigger (STT) for new silicon detector geometry



Project Organization

May 03: Paul Padley replaced Hal Evans as WBS L2 Manager





Trigger Upgrade Project Institutions

Sub-project	Institution(s)
Calorimeter: ADF	Saclay, MSU
Calorimeter: TAB	Columbia
Track trigger	Boston U., FNAL
Cal-Track match	U. of Arizona
Simulation & algorithms	Notre Dame, Saclay, Kansas, Manchester, Brown
Online software & integration	MSU, Northeastern, FSU, Langston
Level 2 β	Orsay, Virginia, MSU
STT upgrade	Boston, Columbia, Stony Brook, FSU

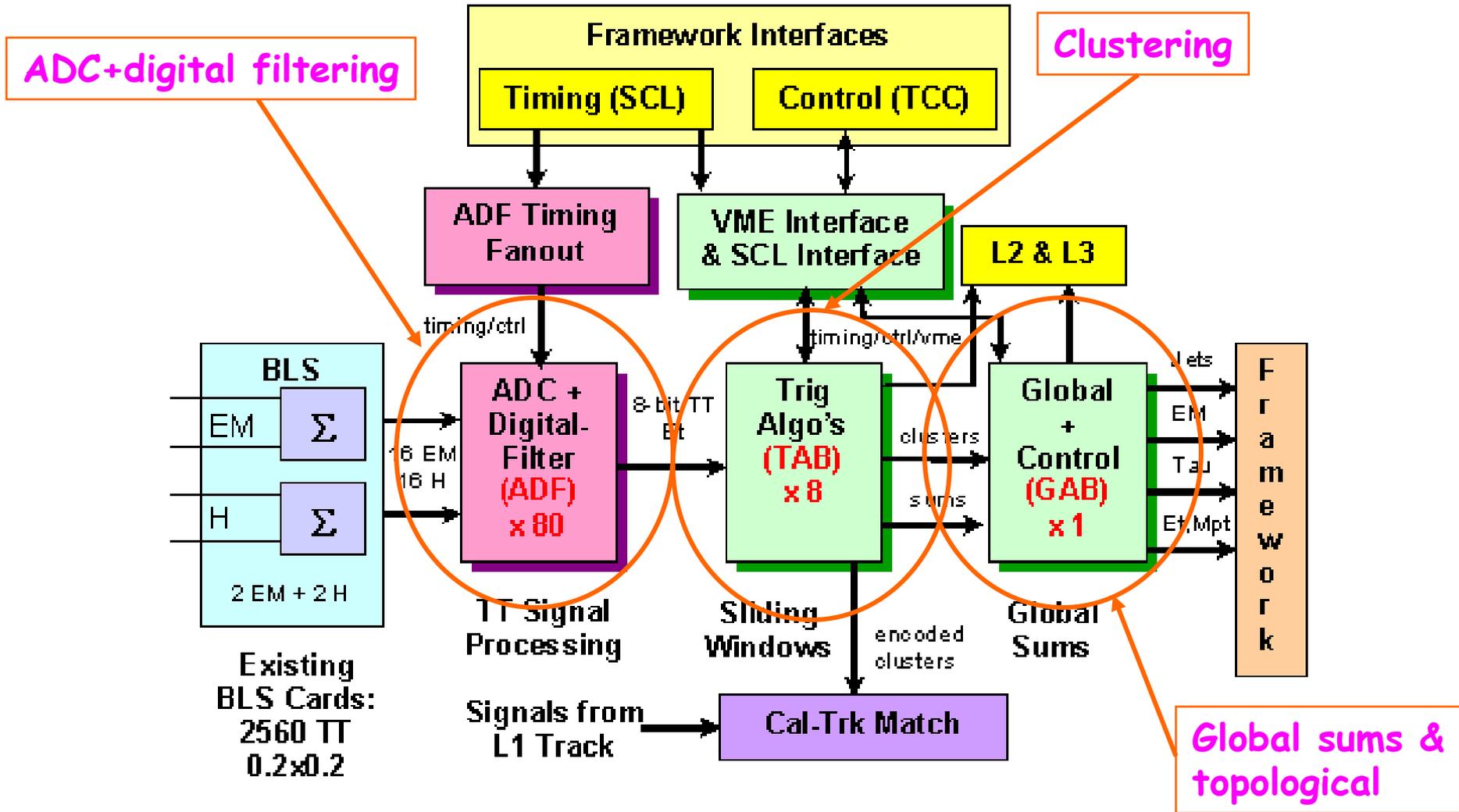


L1Cal Upgrade

- **Saclay**
 - ◆ D. Calvet
 - ◆ P. LeDu
 - ◆ E. Perez
 - ◆ J. Bystricky
 - ◆ G. Tarte
- **MSU**
 - ◆ M. Abolins
 - ◆ D. Edmunds
 - ◆ P. Laurens
- **Columbia/Nevis**
 - ◆ J. Ban
 - ◆ H. Evans
 - ◆ J. Jin
 - ◆ C. Johnson
 - ◆ J. Mitrevski
 - ◆ J. Parsons
 - ◆ W. Sippach

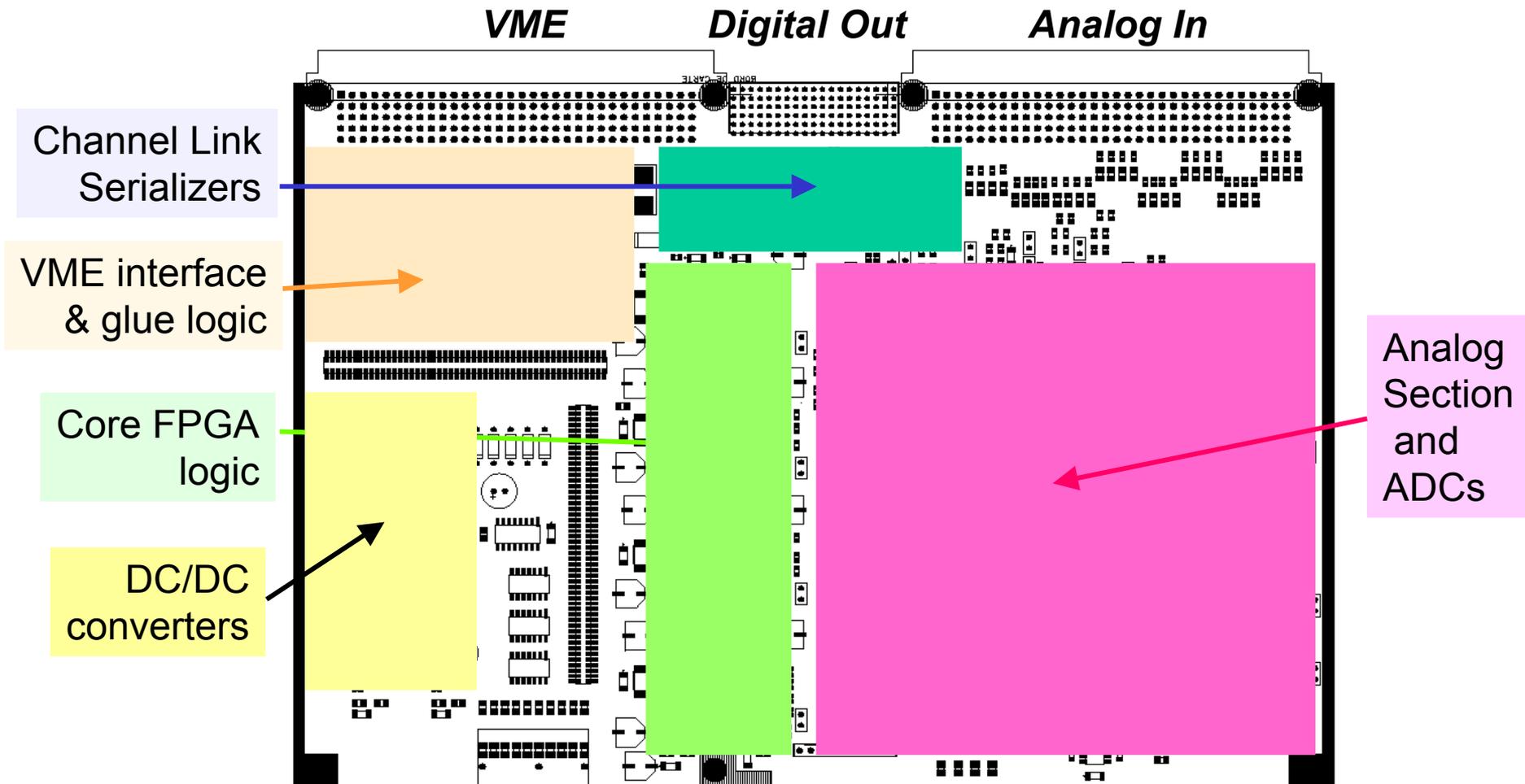


Technical progress: L1Cal





ADF Prototype (Saclay)



~1300 components on both sides of a 14-layer class 6 PCB

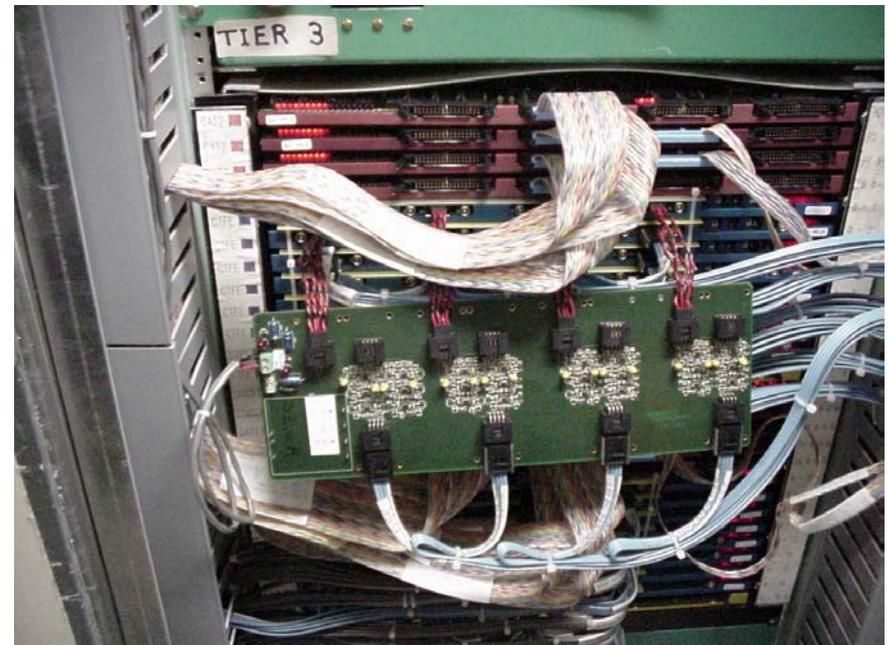
Stuffed board should be in hand

July 2003



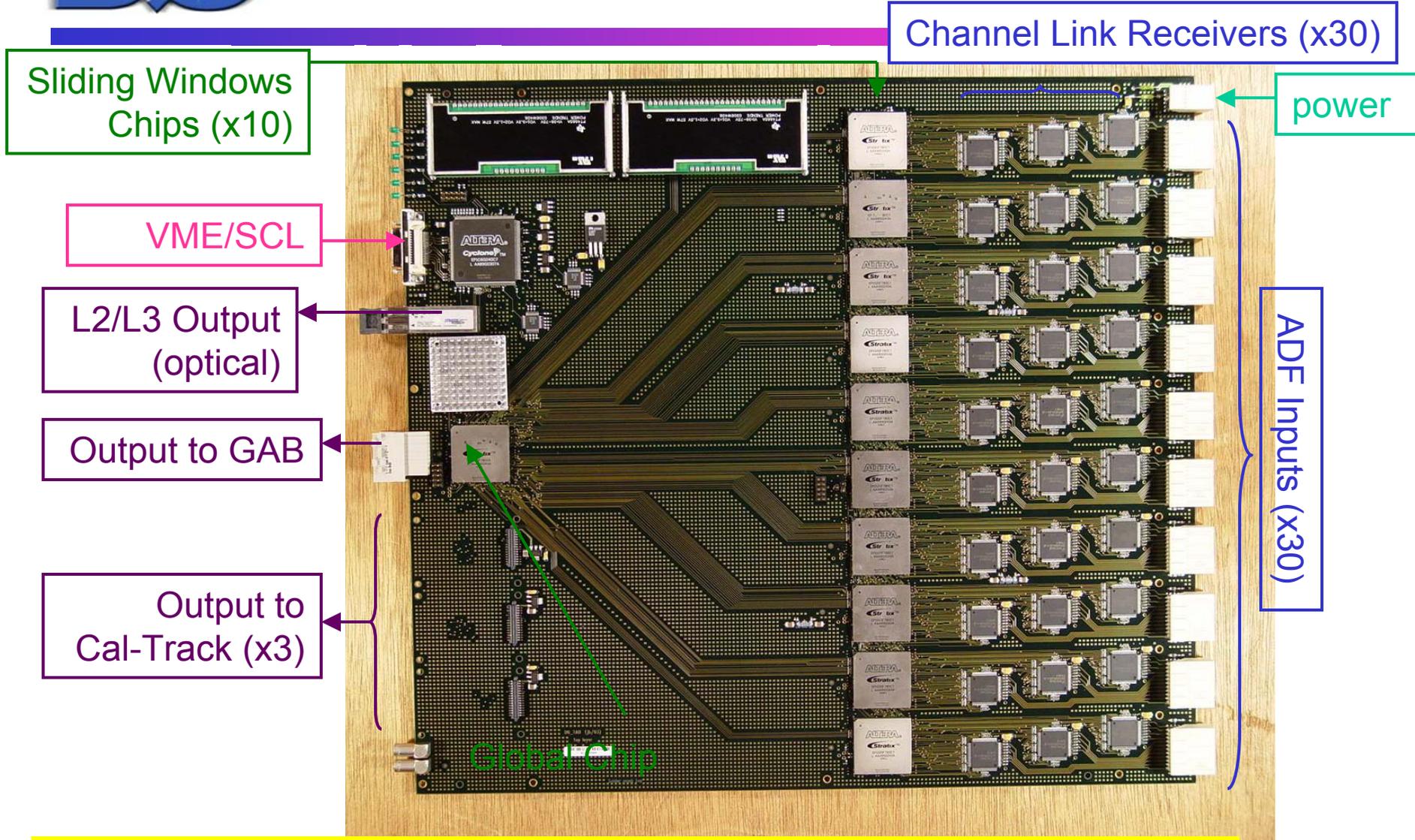
Analog Splitter (Saclay & MSU)

- Analog splitter: allows in-situ test of digital filtering with real signals
 - ◆ Designed and tested at Saclay
 - ◆ Installed in DØ L1Cal trigger (run IIa) during Jan 03 shutdown
 - ◆ Run IIa data with splitter studied for noise effects





TAB Prototype (Nevis)



Assembled Prototype being tested at Nevis - going well

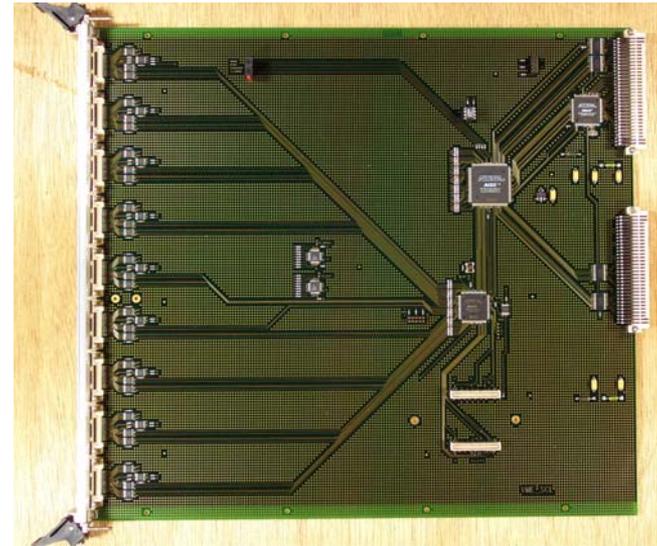
July 2003



VME/SCL and GAB

VME/SCL Prototype at Nevis: May 12

- ◆ main VME & SCL functionality tested & working
- Will be brought to FNAL in July to begin L1 Cal integration tests



GAB Design completed
Layout is underway



L1Cal prototype integration tests (Nevis, MSU, Saclay)

- Major milestone for L1cal
- Scheduled July-October at DØ
- Special test area on sidewalk beside MCH1 (with MCH1 power & ground)
- Includes
 - ◆ VME/SCL board
 - ◆ TAB board
 - ◆ ADF board
 - ◆ Trigger framework
- All full prototypes, will be added to test one at a time beginning with VME/SCL board in July



Technical progress: L1Cal-Track Trigger

- University of Arizona

- ◆ J. Steinberg
- ◆ D. Tompkins
- ◆ C. Leeman
- ◆ N. Wallace
- ◆ B. Gmyrek
- ◆ K. Johns
- ◆ E. Varnes

- Exploit new L1Cal trigger

- Improve Run IIa ϕ matching granularity x8

- Fake EM rejection is improved by ~x2

- Fake τ rejection is improved by ~x10

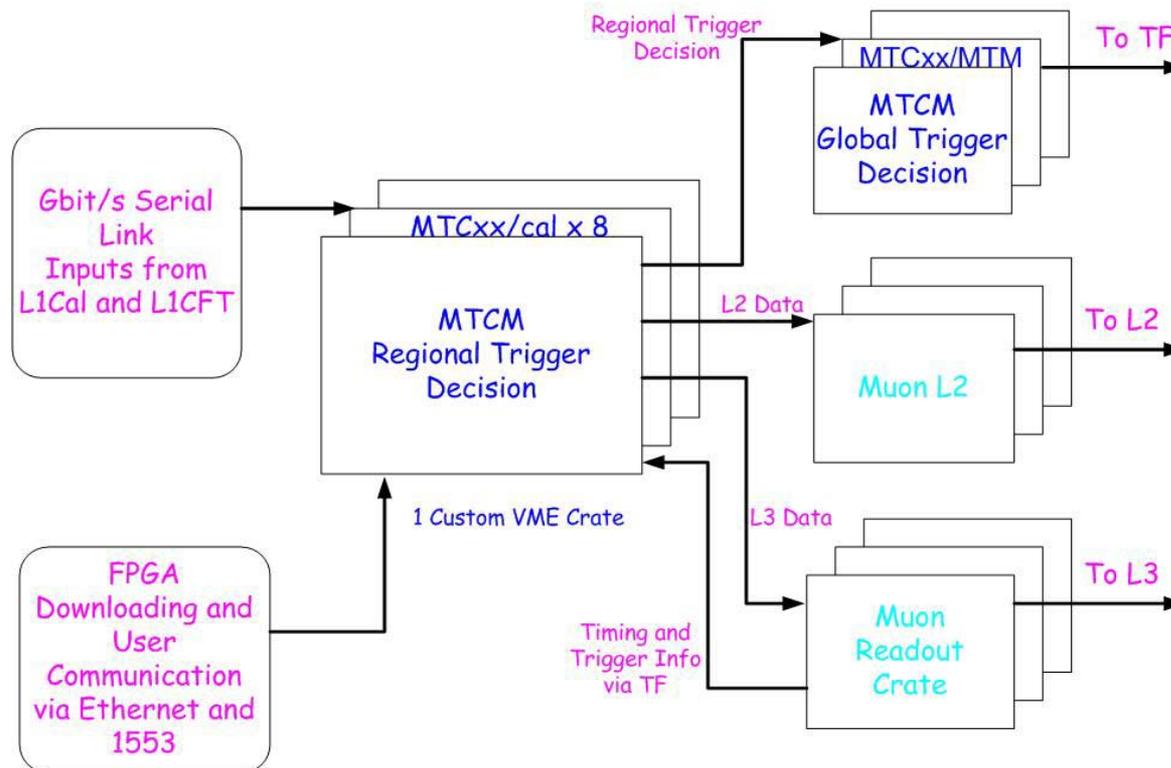




L1CalTrack System

- Uses largely same hardware as existing L1muon
 - ◆ modest cost and effort required

Level 1 Cal-Track Trigger System

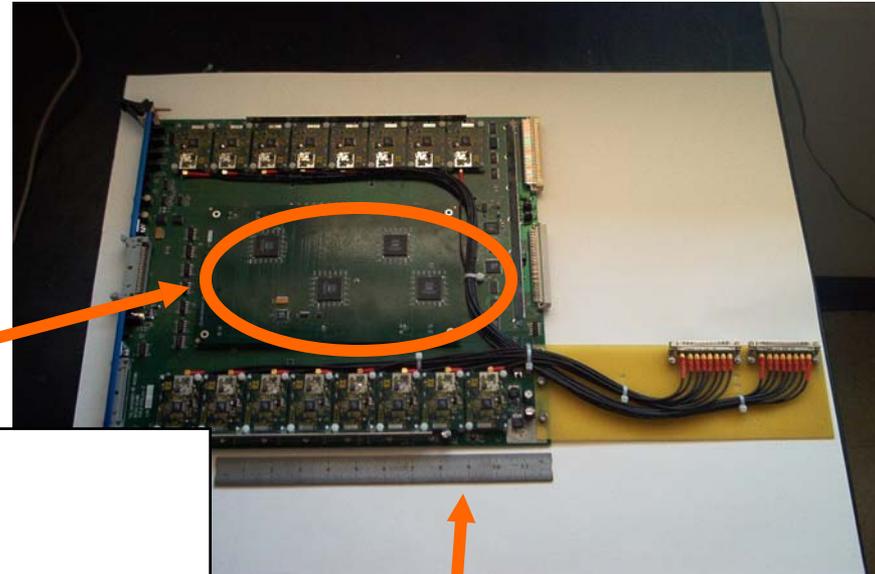




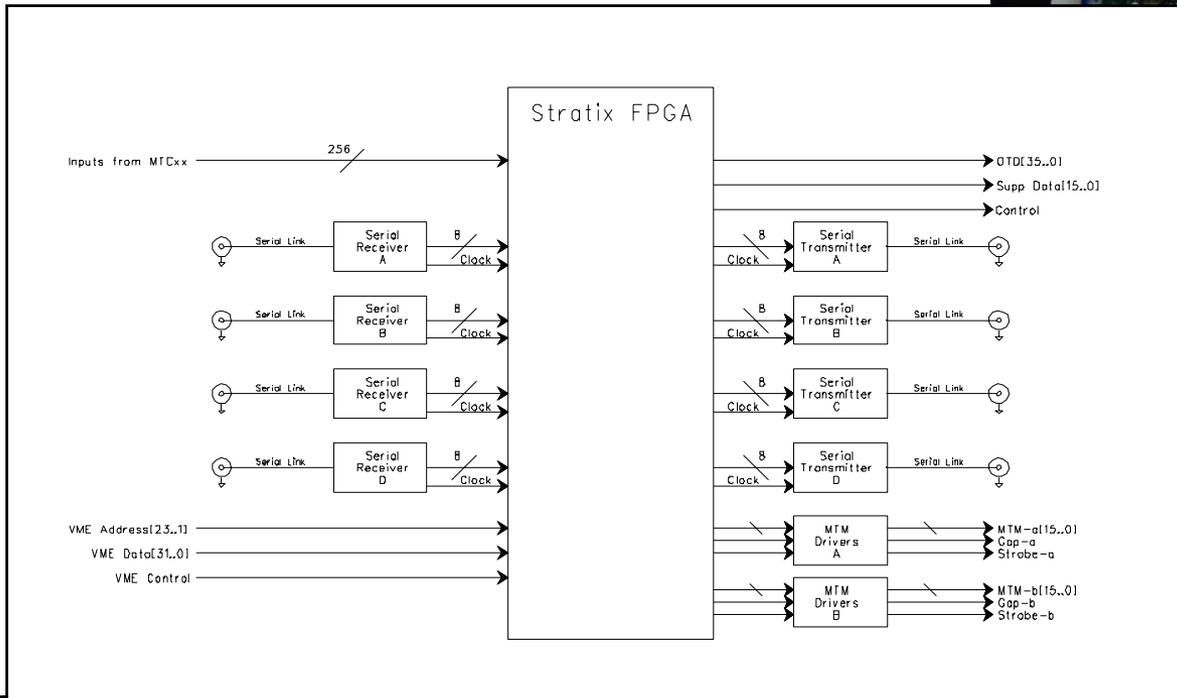
Hardware Progress

- Block diagram of new UFB: only really new board needed for L1 cal-track

Flavor board (daughter)



MTCxx (mother)





Cal-track Hardware Status

- UFB (Universal Flavor Board (daughterboard))
 - ◆ Prototype designed and ready for fabrication
 - ◆ FPGA simulation complete (based on L1Muo CTT.MuScint logic)
- MTCxx (Trigger Card (motherboard))
 - ◆ Design modifications to existing design ~ 75% complete
- MTCM (Crate Manager)
 - ◆ Design modifications to existing design ~ 20% complete



Cal-track Software Status

- L1 Cal-Track Test Software

- ◆ MTT → MTCxx → MTT loop test software is currently being developed
- ◆ The test software uses a new version of the MTT card (MTT == Muon Trigger Test card)

- tsim_l1caltrk

- ◆ Performs calorimeter- CTT track matching in the official DØ trigger simulator
- ◆ Under development

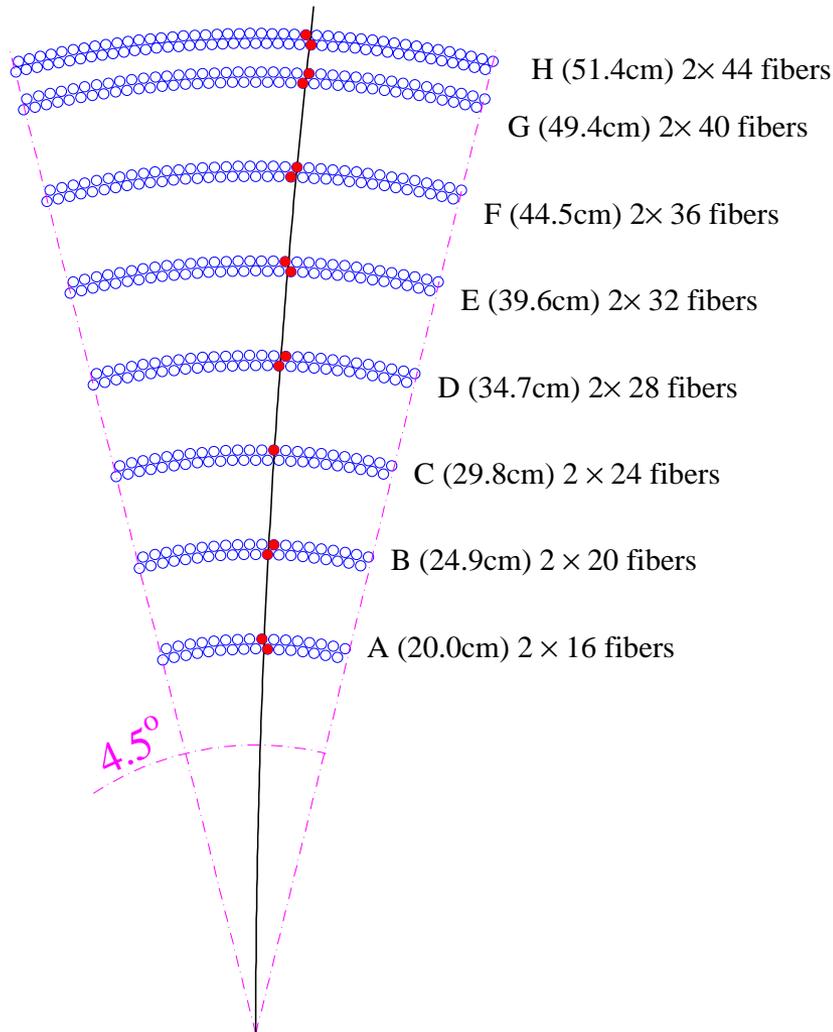


L1CTT Upgrade

- **Boston Univ**
 - ◆ M. Narain
 - ◆ G. Redner
 - ◆ S. Wu
- **Fermilab**
 - ◆ M. Johnson
 - ◆ J. Olson
 - ◆ F. Borcharding
- **Notre Dame**
 - ◆ M. Hildreth
- **Manchester**
 - ◆ L. Han
 - ◆ T. Wyatt
- **Kansas**
 - ◆ G. Wilson
- **Brown**
 - ◆ R. Partridge
- **Indiana**
 - ◆ K. Stevenson



Technical Progress: L1Central Tracking Trigger



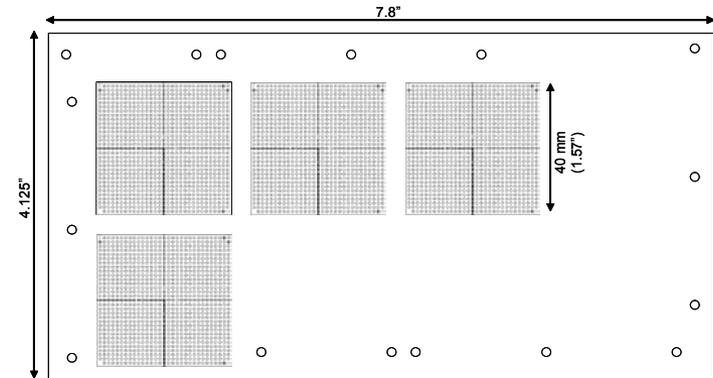
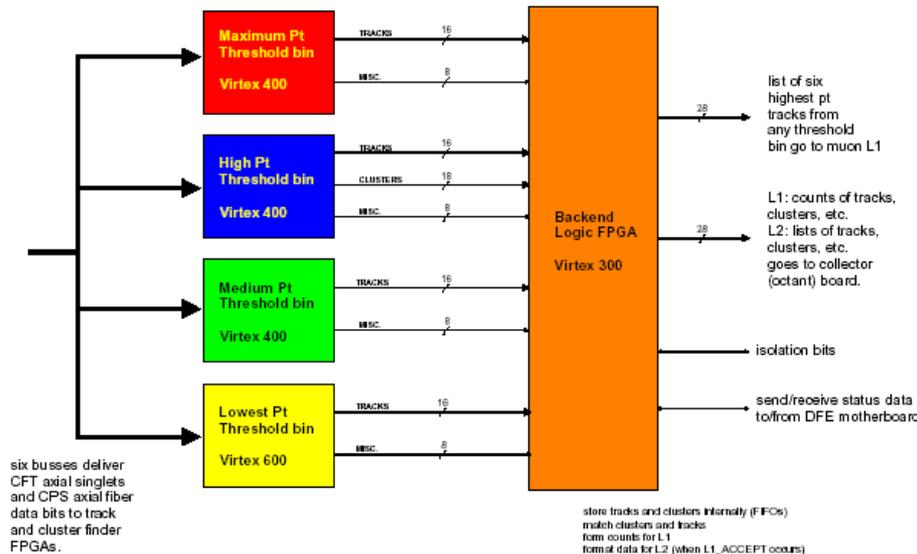
- Tracking trigger rates sensitive to occupancy
- Upgrade strategy:
 - ◆ Narrow tracker roads by using individual fiber hits (singlets) rather than pairing adjacent fibers (doublets)
 - ◆ Cal-track matching



L1 CTT Implementation

- Digital Front End Axial (DFEA) daughter cards get replaced with new layout with larger FPGA's (Xilinx Virtex-II XC2V6000)
 - ◆ Only 80 daughter cards get replaced;
 - ◆ rest of Run IIa system remains intact

CFT/CPS AXIAL Trigger Daughter Board Dataflow



DFEA layout with new FPGA footprints



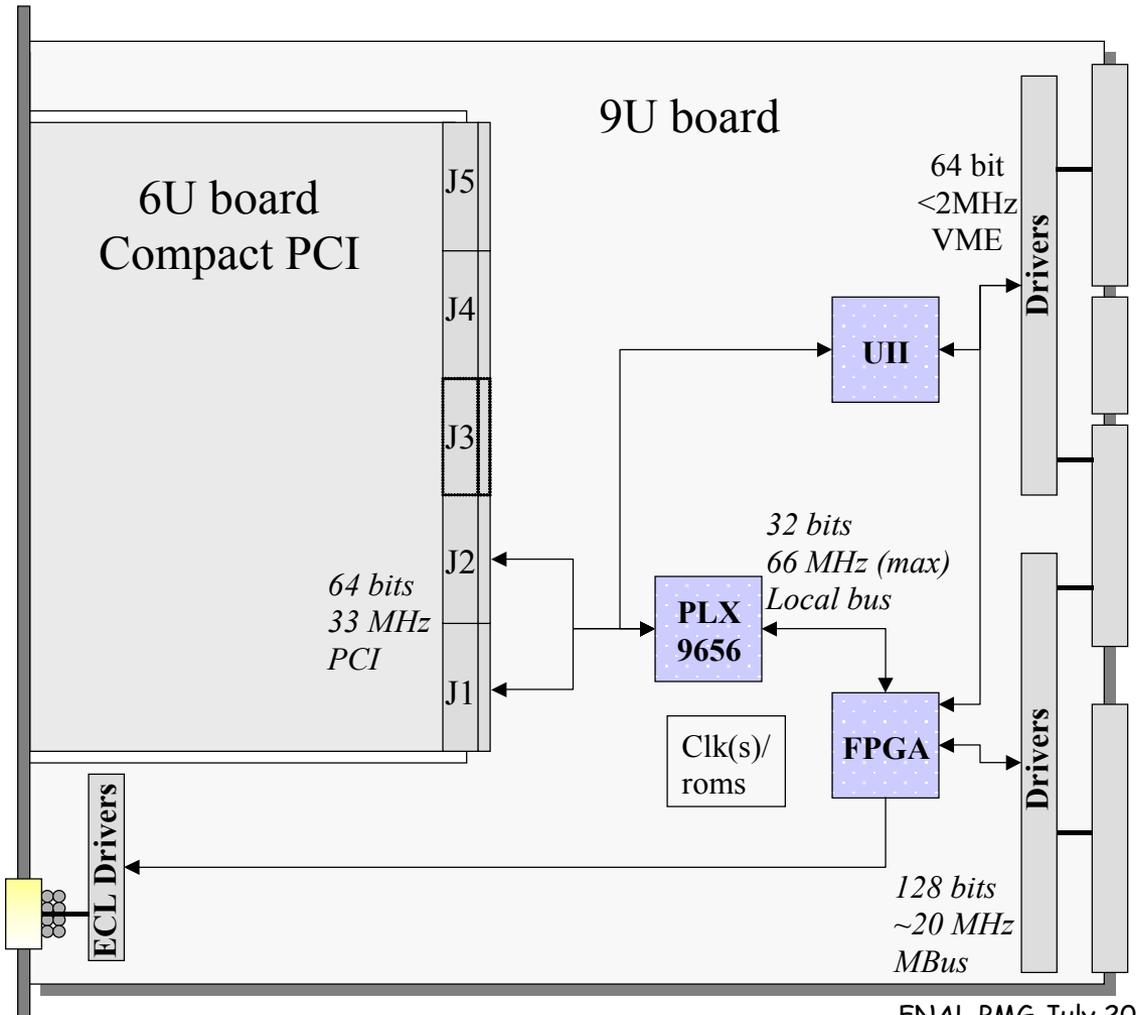
Run IIb L1CTT Progress

- Implemented prototype firmware (Boston U)
 - ◆ Includes equation files from all 4 momentum bins
 - ▲ $p_T > 10$ GeV, $5 < p_T < 10$ GeV, $3 < p_T < 5$ GeV, $1.5 < p_T < 3$ GeV
- Prototype DFEA:
 - ◆ Layout: July, Aug
 - ◆ Fab & assembly: Sept, Oct



L2beta Upgrade

- Run I Ib strategy:
purchase additional,
more powerful
commercial
processors as late as
reasonably possible.

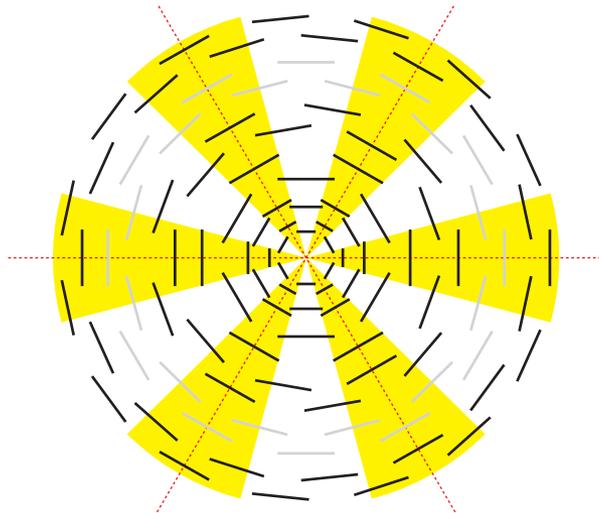


FNAL PMG July 2003



Silicon Track Trigger for Run IIb

- STT upgrade needed to accommodate new SMT geometry
- SMT detector replacement: 6 axial barrel layers
 - ◆ Modest STT upgrade (5-layer readout) requires small quantity of same boards that are used in Run IIa.



Readout layers 0,1,2,3,5

Progress:

- VME Transition Modules procured
 - ◆ Concern about obsolescence
- Original schedule showed other purchases happening now due to expected obsolescence
- Have chosen to hold off, since parts not going obsolete.
- Far from critical path but will push to get started in next few weeks



Status Summary

ID	WBS	Task Name	Duration	Start	2003				2004				2005				
					Qtr 2	Qtr 3	Qtr 4	Qtr 1	Qtr 2	Qtr 3	Qtr 4	Qtr 1	Qtr 2	Qtr 3	Qtr 4		
1	1.2	Run I1b Trigger Upgrade	175.8 w	Thu 11/1/01													31%
2	1.2.1	Level 1 Calorimeter Trigger	168.8 w	Wed 1/2/02													42%
113	1.2.2	Level 1 Calorimeter Track Matchin	101 w	Thu 8/1/02													22%
169	1.2.3	Level 1 Tracking	112.8 w	Thu 11/7/02													78%
228	1.2.9	L1 Trigger Upgrade Production an	0 w	Fri 5/20/05													3/16 5/20
229	1.2.4	Level 2 Beta Processor	61 w	Mon 12/1/03													0%
270	1.2.5	Silicon Track Trigger Upgrade	67.6 w	Fri 8/1/03													0%
354	1.2.8	L2 Trigger Upgrade Production an	0 w	Mon 2/28/05													2/28 2/28
355	1.2.6	Trigger Simulation	115.4 w	Thu 11/1/01													68%
374	1.2.7	Administration	104 w	Mon 2/3/03													20%

- Overall trigger project about 31% complete as of 6/30/03 (not counting installation & commissioning)



Summary

- In the nine months since baselining, the trigger upgrade has been able to make substantial technical progress
 - ◆ Full prototypes in hand for
 - ▲ L1cal ADC/Digital Filter Board
 - ▲ L1cal Trigger Algorithm Board (TAB)
 - ▲ VME/SCL interface for TAB
 - ◆ Prototype design complete for cal-track "Universal Flavor Board", PRR July 30.
 - ◆ Prototype firmware complete for L1CTT
 - ◆ Simulators running
- Lots of progress since last report