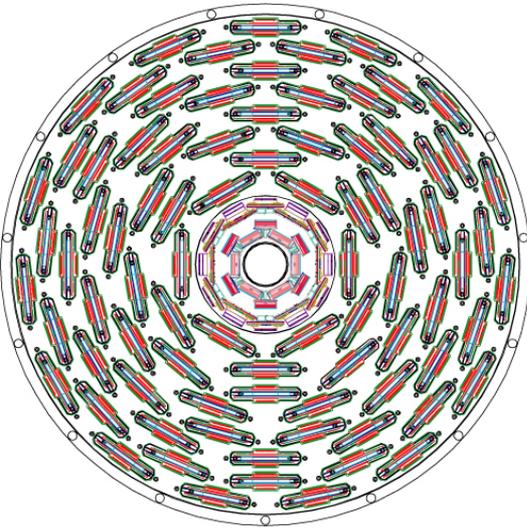
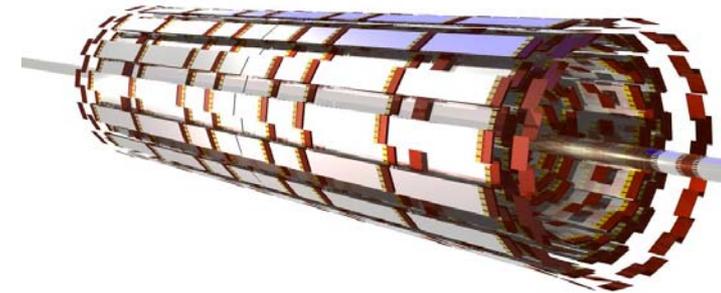


Update on the D0 Run IIb Silicon Upgrade



15 July 03

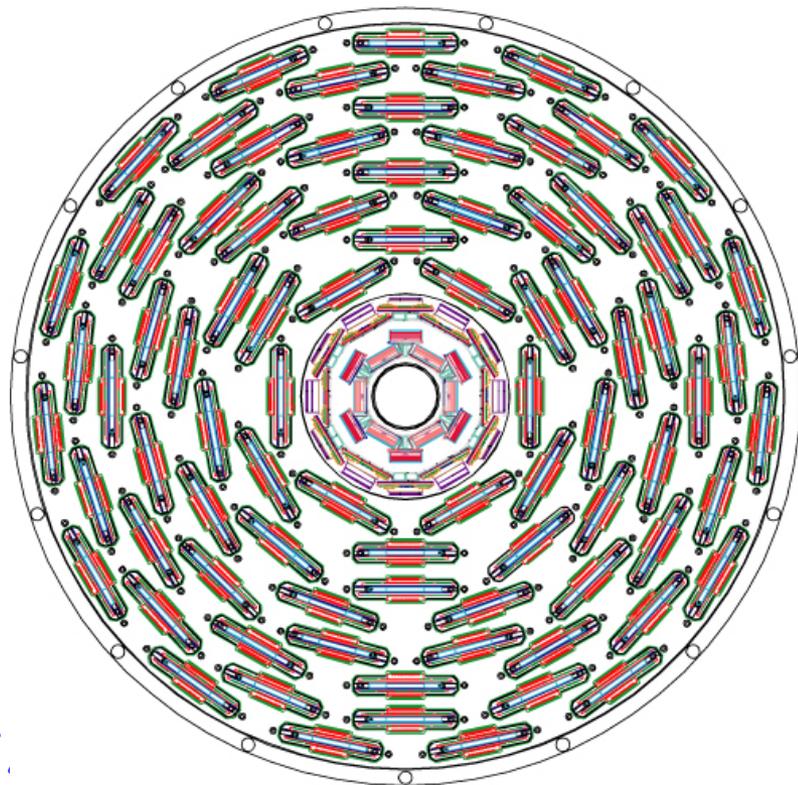


George Ginther
University of Rochester



Detector Design

- Six layer silicon tracker, divided in two radial groups
 - ◆ Inner layers: Layers 0 and 1
 - ▲ $18\text{mm} < R < 39\text{mm}$
 - ▲ Axial readout only
 - ▲ 50/58 μm readout for L0/L1
 - ▲ Assembled into one unit
 - ▲ Mounted on integrated support
 - ◆ Outer layers: Layers 2-5
 - ▲ $53\text{mm} < R < 164\text{mm}$
 - ▲ Axial and stereo readout
 - ▲ 60 μm readout
 - ▲ Stave support structure
- Employ single sided silicon only.
3 sensor types all with axial strips
 - ◆ All sensors intermediate strips





Outer Layer Sensors

- Layers 2 through 5 sensors
 - ◆ 100 prototype sensors ordered from Hamamatsu May 02 and delivered 29 Nov 02
 - ◆ Subset of sensors have undergone full QA program
 - ▲ Very few defects identified
 - All HPK flagged defects confirmed and very few additional defects located
 - ▲ Sensors are of very high quality and satisfy all electrical specifications
 - ◆ Production readiness review 6 Mar 03
 - ◆ Order for full production run of 2735 sensors placed mid April
 - ◆ Anticipate initial delivery of first 130 production sensors later this month



Outer Layer Sensors

- Hamamatsu (HPK) outer layer sensor delivery schedule
 - ◆ 130 pcs during July, 2003
 - ◆ 130 pcs during Aug., 2003
 - ◆ 270 pcs during Sep., 2003
 - ◆ 270 pcs during Oct., 2003
 - ◆ 270 pcs during Nov., 2003
 - ◆ 270 pcs during Dec., 2003
 - ◆ 270 pcs during Jan., 2004
 - ◆ 270 pcs during Feb., 2004
 - ◆ 400 pcs during Mar., 2004
 - ◆ 400 pcs during Apr., 2004
 - ◆ 55 pcs during May, 2004



Inner Layer Sensors

- Layer 1 prototype sensors
 - ◆ 10 prototype Hamamatsu sensors ordered April 02 and delivered 21 Sept 02
 - ◆ Strip leakage current for all 10 sensors at FDV
 - ▲ average strip current of 0.4 nA
 - ▲ 14 strips have a current of 1 nA where specification is < 10 nA
 - ◆ Several sensors irradiated at KSU
 - ▲ Independently verified fluence using foil activation
 - ▲ No breakdown observed to 800V
 - ▲ $I_{leak} \sim 300 \mu A$ at highest fluence
 - ▲ V_{depl} agrees with Hamburg model
 - ▲ Data in agreement with other measurements (Montreal)
 - ▲ No breakdown observed up to $V_{bias} = 800 V$
 - ◆ These sensors are also of very high quality
 - ◆ Ordered remaining 3 prototype sensors Hamamatsu had on hand and these should arrive this month
- Layer 0 prototype sensors
 - ◆ Only ELMA prototype sensors available



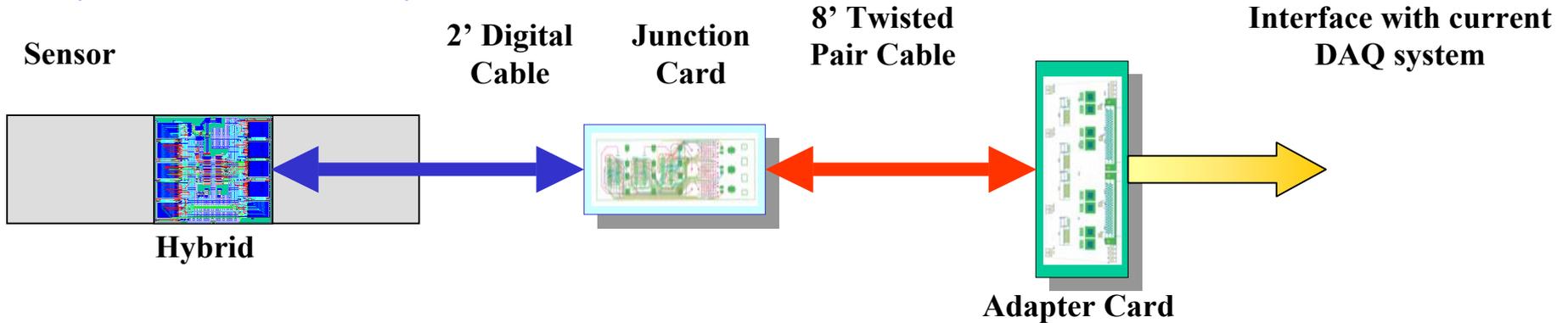
Sensors

- Sensor studies completed
 - ◆ Prototype Hamamatsu sensors are of very high quality
- Production Readiness Review for inner layer sensors scheduled for 8 August
 - ◆ Preparation for order scheduled in parallel with prep for PRR
- Preparation for arrival of production sensors in progress
 - ◆ Certification of remote probing sites
 - ▲ Fermilab
 - ▲ KSU
 - ▲ Stony Brook
 - ▲ Rochester
 - ◆ Procedures and database setup
 - ◆ Visual and mechanical inspection prep

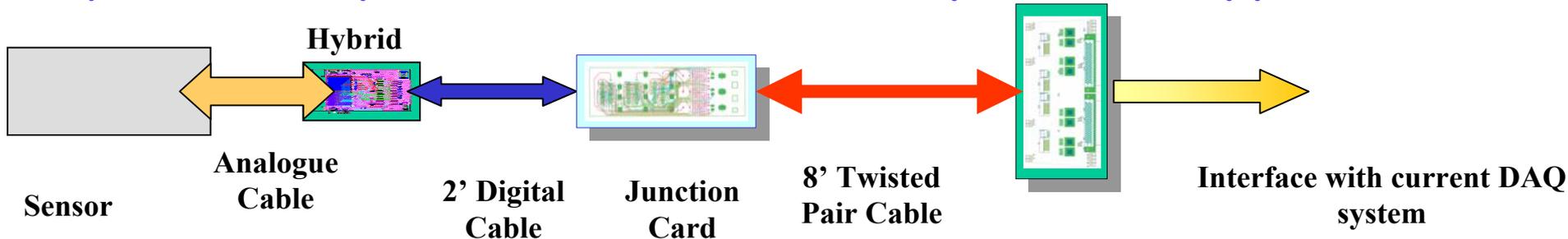


Readout Schematics

Layers 1-5: Hybrids mounted on silicon



Layer 0: Hybrids mounted on independent support

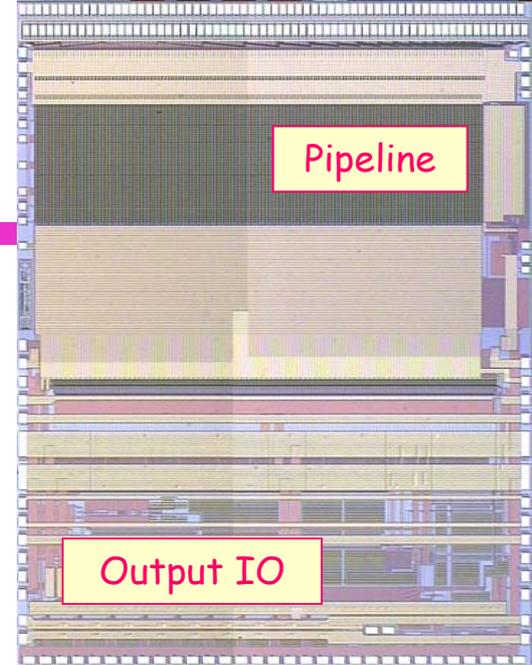


SVX4 chips mounted on hybrids; employed in SVX2 readout mode to facilitate reuse of Run IIa higher level readout infrastructure



SVX4 Chip

- SVX4 readout
 - ◆ 0.25 μm hard hard technology
 - ◆ 128 inputs, 47 pipeline cells
 - ◆ 106 MHz
 - ◆ 53 MHz readout with sparsification
- First full prototype received 11 June 02
 - ◆ A few bugs and features were detected in prototype testing
 - ▲ the MSB of Chip ID not properly available
 - ▲ large pedestal bow across chip
 - ▲ channel to channel variation
 - ▲ pedestal variation with pipeline depth
 - ▲ Redesign of comparator circuitry
 - ▲ Submitted to TSMC April '03
 - ◆ Design modified in response to detected features
- Full preproduction run submitted (to TSMC) April 03 and received 16 May 03
 - ▲ 24 wafers, 454 chips/wafer; yield > 3000 chips for CDF and DØ each

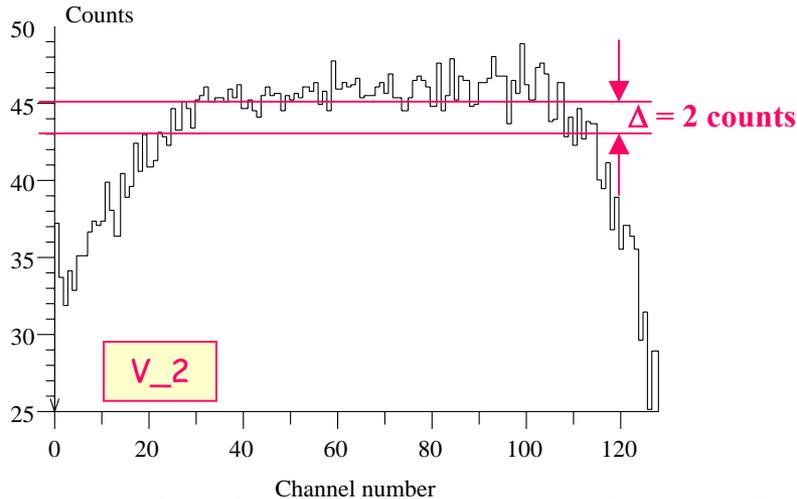




SVX4 Chip

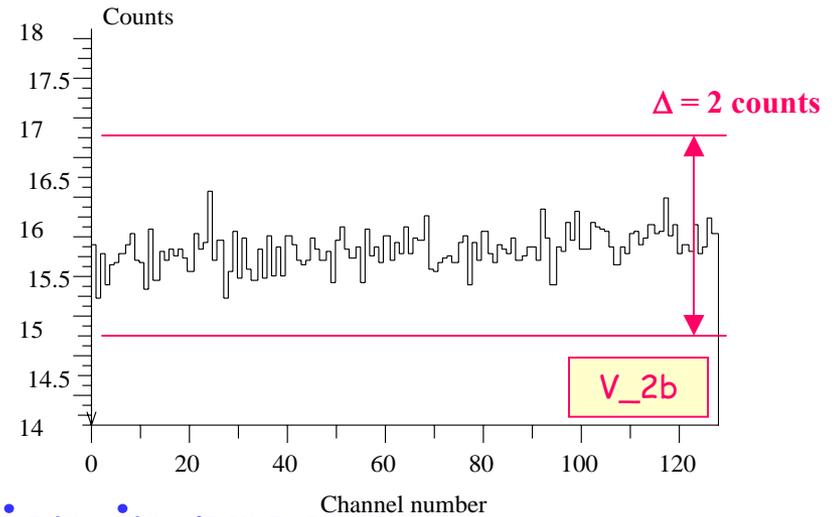
- Previous version of chip

Average



- New version 2b

Average



- Detailed testing and evaluation in progress

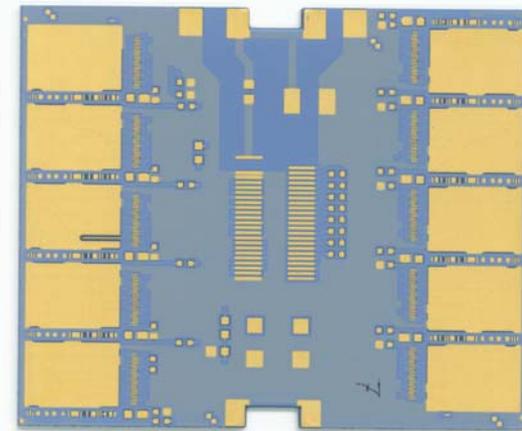
- ◆ Pedestal uniformity across chip much improved
- ◆ Channel-to-channel fluctuations significantly reduced
- ◆ ADC is very linear up to 50 fC
- ◆ Initial test of latest version look very encouraging

- SVX4 release for production scheduled for 25 Sept



Outer Layer Hybrids

- Thick film ceramic hybrids
 - ◆ Beryllia (BeO) substrate
 - ◆ 41.9 mm by 50 mm by 0.380 mm
 - ◆ Supports 10 SVX chips for 1280 channels of readout
 - ◆ Screen printed and fired conductor and dielectric layers (two or three firings per dielectric layer)
 - ▲ 6 layers of conductors insulated via 5 dielectric layers
 - ▲ 8 mil conductor features
 - ▲ Top layer conductors solderable and wirebondable
 - ▲ Dielectric layer must holdoff at least 650V/mil
 - ◆ Dielectric layers printed on backside to control flatness and glue
 - ▲ depth of glue channel in dielectric ~ 0.1 mm
 - ◆ Hybrid flatness and thickness specifications established for ease and reliability of assembly





Proto Outer Layer Hybrids

- Prototype hybrids are electrically functional
- Many failed to satisfy initial mechanical specification
 - ◆ And the trend is a concern

Delivery	Vendor	Quantity	Average		Average		mm
			Thickness	Flatness	Glue Channel	Depth	
	Amitron	Axial 23	0.84	0.19	0.40		mm
11-Nov-02	CPT	Stereo 23	0.92	0.04	0.10		mm
16-Nov-02	CPT	Axial 15	0.94	0.06	0.11		mm
6-Feb-03	CPT	Axial 35	0.90	0.14	0.03		mm
27-Feb-03	CPT	Stereo 27	0.86	0.08	0.05		mm
Original Specification			<0.90	<0.050	>0.075		mm
Revised Specification			<0.950	<0.150	>0.050		mm

- Vendors had issues with yield that impacted delivery schedules and likely have implications for production prices
- These hybrids are now on the critical path

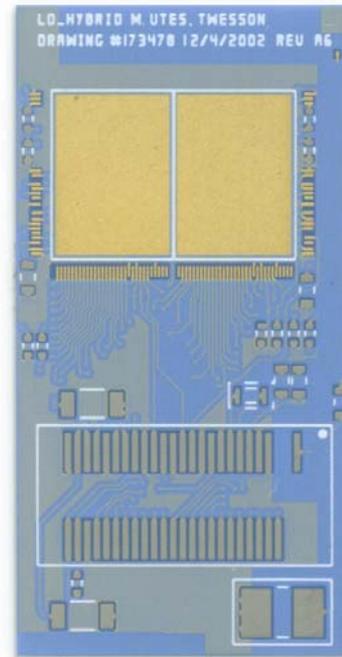


Pre-Pro Outer Layer Hybrids

- Used prototypes to refine specs
 - ◆ Studies of adhesive run-out
 - ◆ Improve manufacturability by relaxing tolerances
- Electrical modifications
 - ◆ AVDD and DVDD tied together
 - ◆ Eliminate bias cap (integrated into SVX chip)
 - ◆ Isolated ground to minimize analog sensitivity to digital signals
 - ◆ Minor improvement to VCAL schematics
- Vendor issues motivated search for additional candidates
 - ◆ Yield issues raise concerns about eventual production costs
 - ◆ Concerns regarding future of one vendor (expert moved too!)
 - ◆ Identified several more potential vendors
 - ◆ Refined artwork to reflect standard pyramid fabrication technique
 - ◆ Axial pre-production ordered from CPT, Halcyon and Scrantom
 - ◆ Stereo pre-production hybrids ordered from Amitron
- Anticipate deliveries in mid-August to mid-September



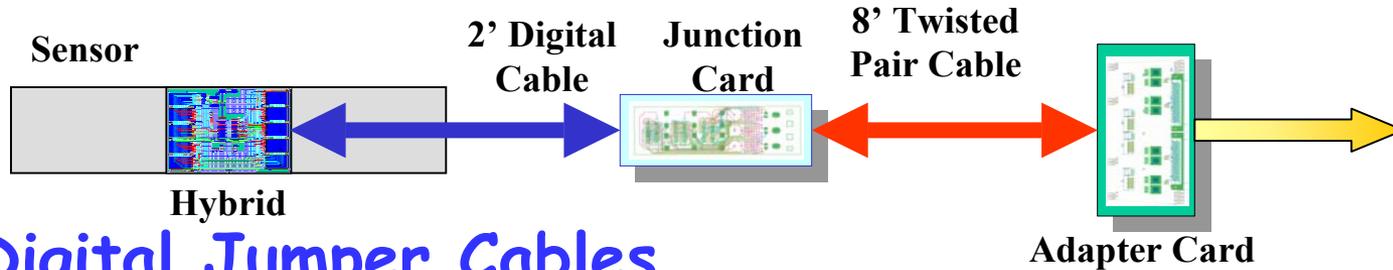
Inner Layer Hybrids



- L1 hybrids (supports 6 SVX chips)
 - ◆ 18 prototype L1 hybrids received from CPT
 - ▲ Functional but had issue with soldering on top layer
 - ◆ Pre-production L1 hybrids
 - ▲ Artwork modifications in progress
 - Isolated grounding scheme
 - Topside pad for grounding to support structure
- L0 hybrids (supports 2 SVX chips)
 - ◆ 22 prototype L0 hybrids received from Amitron
 - ▲ Fabricated ~10 weeks after artwork release
 - ▲ Meet mechanical specs, functional but suffered crack during dicing
 - ▲ 5 hybrids stuffed with latest SVX4 chips for testing
 - ◆ Pre-production L0 hybrids
 - ▲ Artwork modifications in progress
 - Isolated grounding scheme
 - Bottomside pad for grounding to support structure
- Anticipate pre-production orders of L0 and L1 this month



More on Readout

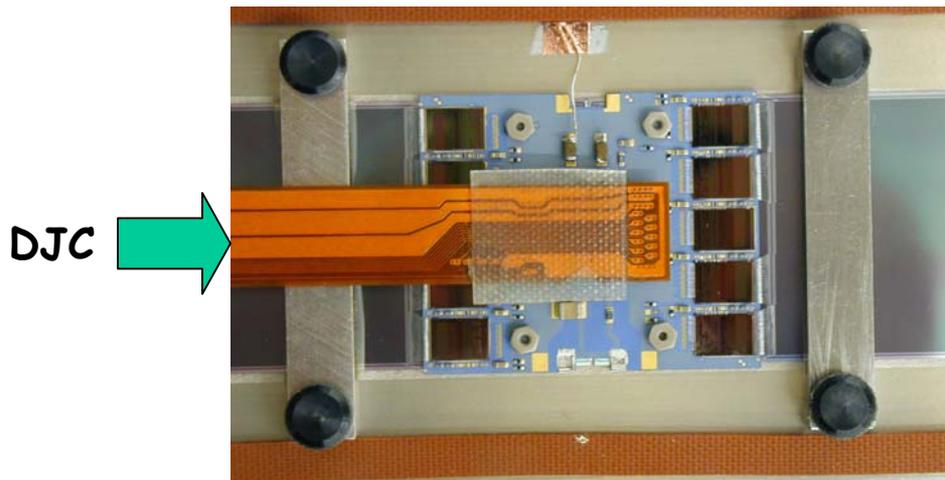
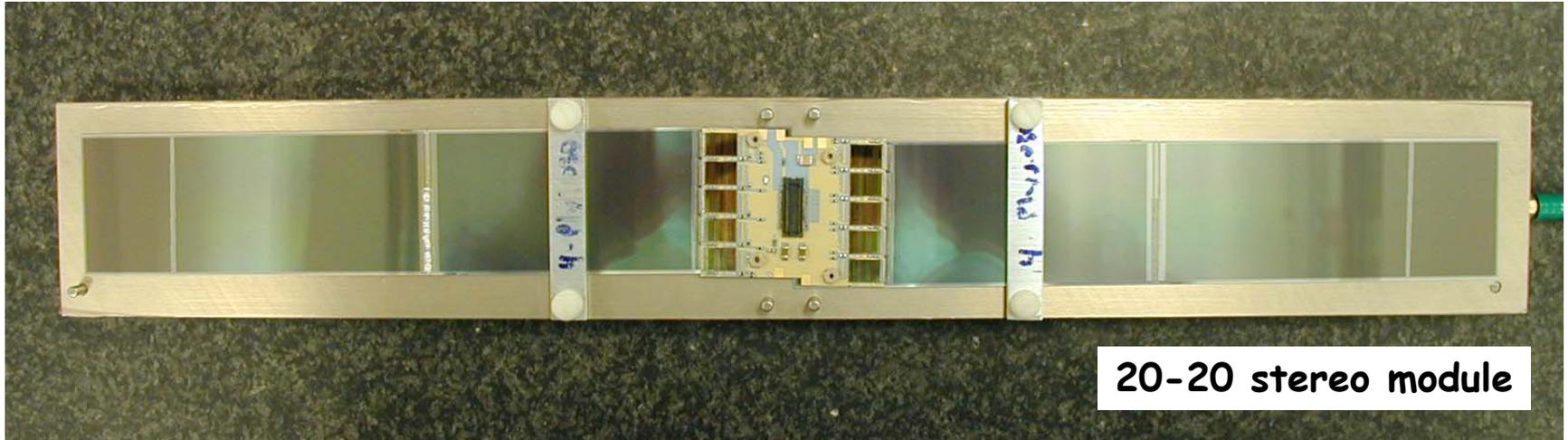


- **Digital Jumper Cables**
 - ◆ 450 test stand cables ordered
 - ▲ 300 received from Century
 - In process of assembly and testing
- **Junction Cards (no active elements)**
 - ◆ Design revised to facilitate installation
 - ◆ Prototype design under review, delivery mid-August
- **Twisted Pair cables**
 - ◆ 16 second prototypes arrived 2 July
- **Adapter Card**
 - ◆ voltage regulation and signal translation
 - ◆ Thermal analysis complete
 - ◆ Second prototype expected early August



Outer Layer Readout Modules

- Prototypes of all four outer layer readout module types have been fabricated using prototype fixturing

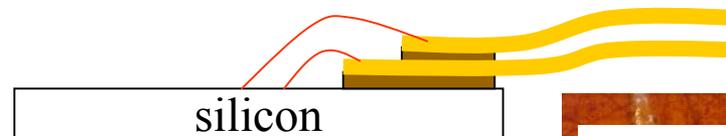


Close up of axial module in vicinity of hybrid
Note attached Digital Jumper Cable

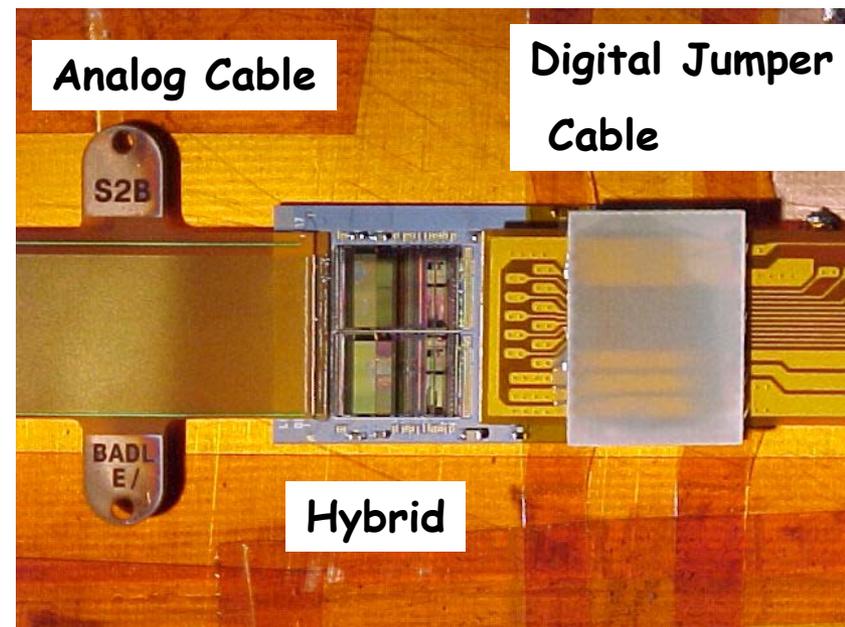


Inner Layer Readout Modules

- Prototypes of Layer 0 and Layer 1 readout module have been fabricated using prototype fixturing
- Layer 0 module has sensor connected to hybrid via analog cable (space and thermal constraints)
 - ◆ Increased capacitance leads to reduced signal to noise
 - ◆ Low mass fine pitch (91 μm) flex cable
 - ◆ Two cables offset by 50 μm



- ◆ Up to 463 mm long
- ◆ 40 prototype cables delivered
 - ▲ Mechanically and electrically high quality cables
- ◆ Currently evaluating lamination of cables
 - ▲ Bonding spacer
 - ▲ Cable spacer to reduce capacitance





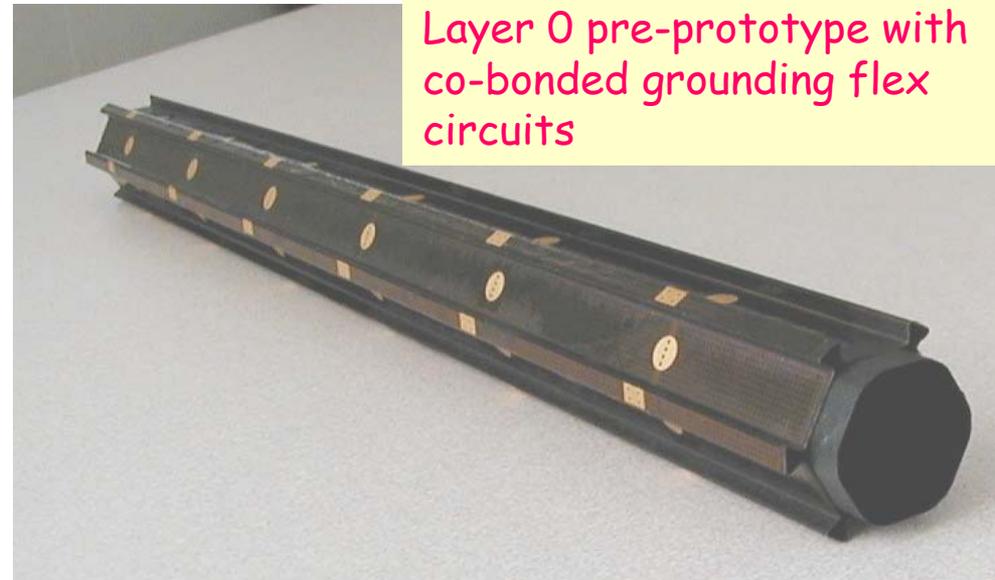
Inner Layer Support Structures

- Carbon fiber support structures
 - ◆ All mechanical and thermal FEA analyses complete
 - ◆ Prototype fabrication tooling complete
 - ◆ Pre-prototype structures fabricated and under tests
 - ◆ Grounding of structures to electrical components being carefully reviewed and studied
 - ▲ Flex circuits to be co-bonded to prototype structures (for grounding) currently on order
 - ◆ Expect prototype support structures late summer

L1 Support Structure Assembly



Layer 0 pre-prototype with co-bonded grounding flex circuits





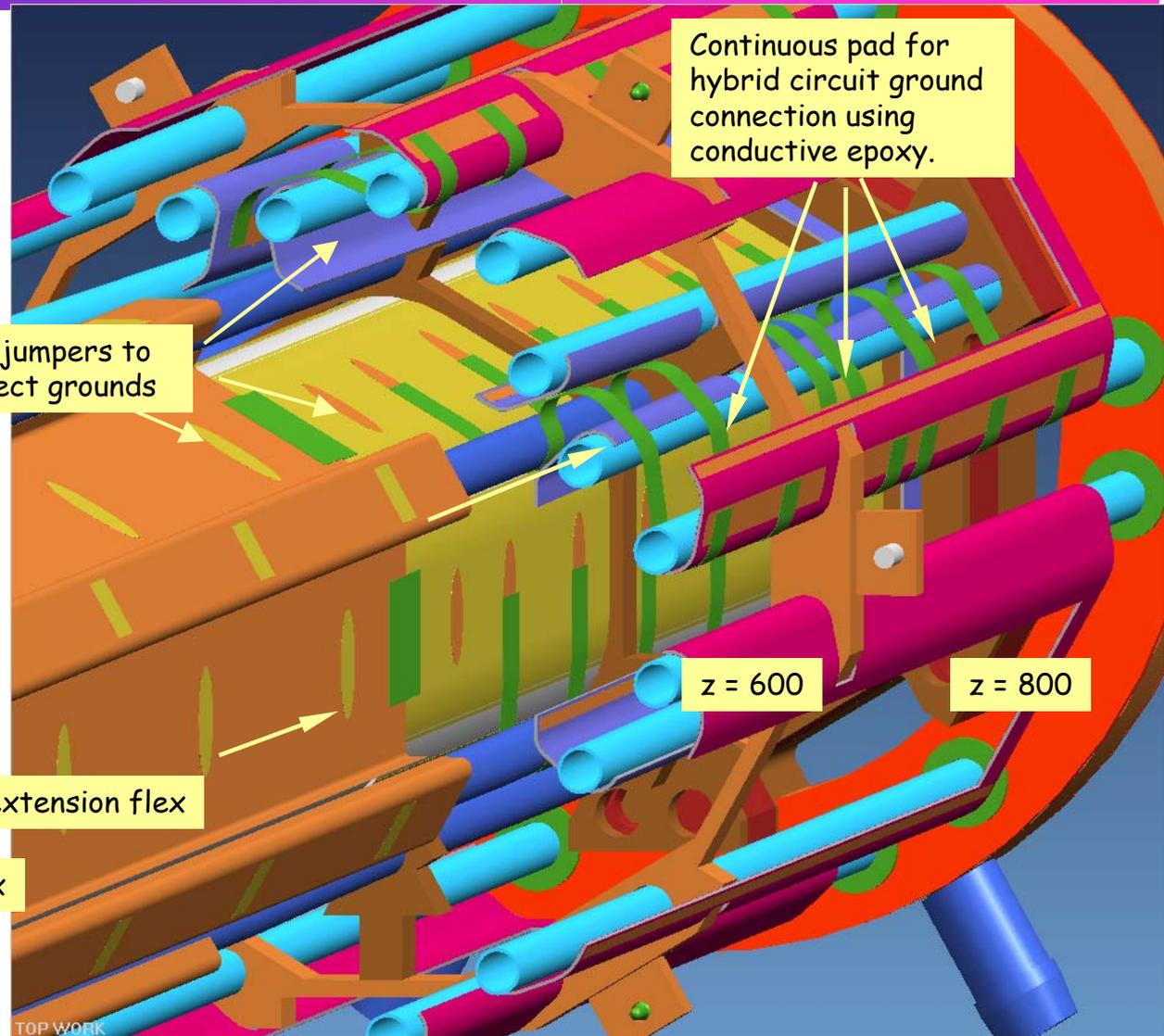
Grounding Scheme

- Increased capacitance of LO due to analog cable requires care in grounding to minimize signal to noise
 - ◆ Goal is $S/N > 10$ after irradiation
 - ◆ Currently have $S/N \sim 12$ before installation on support structure
- 114+ flexible printed circuits will be implemented to address grounding for Layer 0

LOB support grounding flex

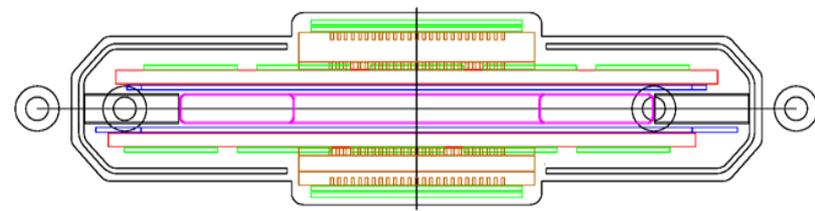
LO support extension flex

LOA support grounding flex





Staves



- Basic building block of the outer layers is a stave
 - ◆ Two-layer structure of silicon sensors
 - ◆ One layer of axial only, and one layer of stereo only readout
 - ▲ stereo angle obtained by rotating the sensor
 - ◆ Layers separated by a "core" with positioning and reference pins and PEEK cooling tubes
 - ◆ C-shells at edge of stave provide stiffness
 - ◆ Total of 168 staves
- Pre-production mechanical stave fabricated
 - ◆ Production procedures under development
- Staves are positioned and supported in carbon fiber bulkheads at $z = 0$ and $z = 605$ mm
 - ◆ Locating features on stave provide the alignment
 - ◆ Bearings are being placed on prototype bulkheads



QA and Testing

- Components are rigorously tested in burn-in stands
 - ◆ Two hybrid burn-in test stands, 16 channels each
 - ◆ Two module burn-in test stands, 32 modules each
 - ▲ with associated cooling
 - ◆ Setup of burn-in stands complete at SiDet and passed Safety Inspection for 24/7 running
 - ◆ A hybrid is currently initial phase of long-term burn in test
 - ◆ Debugging and laser setup stations also operational
- Full system tests using D0 readout configuration
 - ◆ "1%" test - up to 8 readout channels
 - ▲ Readout hardware installed and being debugged
 - ▲ Final low voltage power supply installation in progress (to provide tests of long distance remote sensing)
 - ◆ "10%" test - to perform full sector test
 - ▲ System currently being setup in the Lab C cleanroom



Monitoring and Software

- **Temperature Monitoring**
 - ◆ Prototype flex circuits ordered
 - ◆ Readout system being tested
- **Radiation Monitoring**
 - ◆ Diodes diced for testing
 - ◆ Prototype components ordered and/or fabricated
- **Production Database**
 - ◆ Adopted ATLAS database design
 - ◆ Supported by D0 online support group
 - ◆ Development underway
- **Software**
 - ◆ Address scheme determined
 - ◆ Unpacker and packer written and under test



Silicon Status

Component	Vendor	Design	First Prototype		Second Prototype		Final Order
			Ordered	Delivered	Ordered	Delivered	
L0 Sensors	ELMA	✓	✓	✓			
	HPK	✓					
L1 Sensors	ELMA	✓	✓	✓			
	HPK	✓	✓	✓			
L2 Sensors	HPK	✓	✓	✓		✓	
Analogue Cable	Dycx	✓	✓	✓	✓	✓	
L0 Hybrid	Amitr.	✓	✓	✓	✓		
L1 Hybrid		✓	✓	✓			
L2A Hybrid	CPT	✓	✓	✓	✓		
	others	✓	✓	✓	✓		
L2S Hybrid		✓	✓	✓	✓		
Digital Cable	Honey	✓	✓	✓	✓	✓	
	Basic	✓	✓	✓	✓	✓	
Junction Card		✓	✓	✓			
Twisted Pr. Cable		✓	✓	✓	✓	✓	
Adapter Card		✓	✓	✓	✓		
Purple Card		✓	✓	✓	✓	✓	✓
Test Stand Elctr.		✓	✓	✓			✓

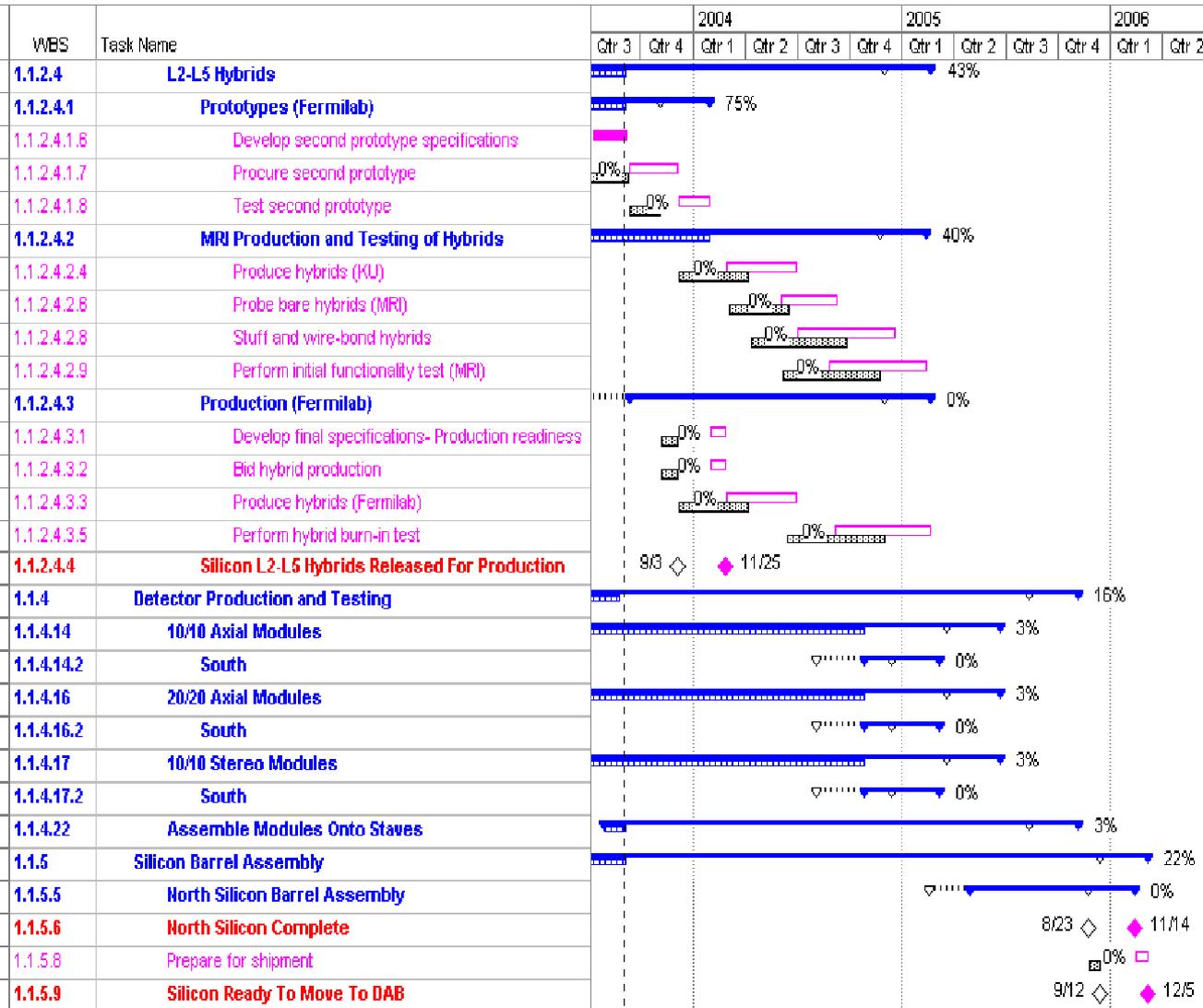


Production Readiness Reviews

- **Inner Layer Sensors** **8 Aug**
 - ◆ Difficulties arranging schedule for return of committee and appropriate D0 experts during summer
- **Inner Layer Support Structures** **early Sept**
 - ◆ Prototyping delayed by grounding improvements
- **Stave Design** **mid Sept**
 - ◆ Mechanical pre-production stave produced
 - ◆ Evaluation in progress
- **Low Voltage Power Distribution** **late Sept**
 - ◆ Distribution design nearly complete, power supply under test
 - ◆ Power supplies outside collision hall, requires long sense lines
 - ◆ Installation at 1% test stand in progress to facilitate tests
- **20 cm Gang Production** **late Sept**
 - ◆ Fixturing and procedures developed
 - ◆ Additional experience fabricating pre-production modules anticipated in the near future



Critical Path



SVX4 chip development drove the critical path in the past



L2-L5 hybrids



L2-L5 Module Assembly



Stave Assembly



Barrel Assembly



Critical Path

- Forecast for Silicon Ready to Move 5 Dec 05
- Corresponding Director's Milestone 25 May 06
- While the L2-L5 hybrids are currently on the critical path, other creatures lurk nearby
 - ◆ a one week delay in the SVX4 schedule returns the SVX4 to the critical path
 - ◆ the L0 hybrid is also hanging close to critical path
 - ◆ (and the L1 hybrid is pushing a Director's milestone)
 - ◆ all will continue to need diligent monitoring
- Because of the multiple items near critical path and the aggressive nature of the schedule, it is a real challenge to regain ground on slips that have already occurred (especially during the R&D and prototyping phase of this project)
- Continued vigilance is required



Conclusions

- Excellent progress on prototyping and pre-production of the D0 Run IIb Silicon Upgrade
 - ◆ Prototypes of all components of the design in hand
 - ◆ Pre-production for most parts in progress
 - ◆ Remaining technical challenges are being addressed
 - ◆ Have started placing production orders
- A strong, knowledgeable, experienced and very dedicated team is working hard (in a rather challenging climate) to produce the upgraded silicon detector that D0 needs to significantly enhance its performance throughout Run IIb