

## **Hybrid production, assembly, and testing QC/QA**

The hybrids are electrical circuits that provide a platform for the SVX4 readout chips, which are coupled via analog cables (L0) to the sensor strips. The hybrid circuits distribute power and control signals to the SVX4 chips and return the digitized data from the digital bus lines from the D0 data acquisition system through an Molex connector mounted to the hybrid, which connects to the external electronics system with a digital jumper cable. There are two SVX4 chips per hybrid and a total of 48 hybrids needed for the detector.

The hybrids consist of several parts, which are assembled to form the final readout unit. The hybrid substrate is a printed circuit on beryllia ceramic. Mounted on this are passive components, custom integrated circuit die called the SVX4 chip, and a connector which allows the digital jumper cables to be attached to the circuit (Molex receptacle). There will be 125 hybrids that will need to be assembled and tested.

The sequence for the production, assembly, and testing of the hybrids includes the following steps:

1. Bare hybrid production (vendor)
2. Bare hybrid wiping (Fermilab)
3. Bare hybrid mechanical inspection (KU).
4. Bare hybrid electrical testing (either Univ. of Kansas (KU) or California State Univ. at Fresno (CSUF))
5. Hybrid assembly including stuffing and wirebonding (vendor)
6. Initial Functionality test (KU or CSUF)
7. Burn-in (KU)

A database tracks both the progress and quality of the hybrids throughout this process. The database is accessible over the web for all institutions to track progress: xxx. In addition, both KU and CSUF have web sites:  
[http://kuhep7.phsx.ukans.edu/hep/l\\_zero/Home%20Page%20for%20L0%20Silicon%20Detector.html](http://kuhep7.phsx.ukans.edu/hep/l_zero/Home%20Page%20for%20L0%20Silicon%20Detector.html) and  
xxx at Fresno.

A paper traveler will accompany the hybrid as shown in Appendix I. There are repair loops that may be needed at various stages of the process. Each of these steps is described in more detail below along with the quality control steps taken.

### ***Bare hybrid production***

The hybrid is to be constructed of alternating thick film layers of gold and dielectric built up on a beryllia substrate. There are six conductor layers and five dielectric layers on the top side. 125 of the hybrid circuits will be procured through Amitron Thick Film Technologies, North Andover, MA 978 686-0622. The vendor must meet the following specifications:

- The gold on the top layer for wire bonding must be compatible with aluminum-wedge bonding.
- The plating on the top for the solder pads must be compatible with using solder paste with reflow temperatures of 205 to 220 °C (for example a Sn62Pb36/Ag2 solder paste by Qualitek such as Delta 792). A plating metal such as Dupont 4596 is recommended.
- The hybrid must be flat to within 0.1mm. (Layers of dielectric may be added to the backside of the substrate in order to meet this specification.)
- Total thickness of the finished hybrid must not exceed 1.0mm.
- Thickness of the metal trace layers is to be 7 to 9 um.
- Ground and power plane layer thickness is to be 4 to 6 um.
- Dielectric layer thickness is to be 40 to 60 um.
- The dielectric strength is to be 650V/mil or higher.
- Laser cutting of the final outline should be accurate to +/- 0.05mm
- Continuity testing of all pads will be performed at the production vendor, with a dual flying head probe test.

#### *Bare hybrid receiving at Fermilab*

Bare hybrid substrates will be received at FNAL. A technician will be assigned to receive all hybrids at SiDet. Here, each hybrid will be assigned a unique number (301-426) and a traveler will be started for each one. The hybrids will be entered into the D0 database as well as the SiDet beryllium tracking spreadsheet. The hybrids will then be cleaned according to prescribed procedures and adhering to the associated JHA (Job Hazard Analysis). After this EH&S will be notified to take wipes of the hybrids for verification that they are not contaminated (beryllium). The results of these wipes are typically available is 1 week. If the wipes come back clean then EH&S approval will be entered into the D0 database and the SiDet beryllium tracking spreadsheet (name and date of approval). If any contamination is found the cleaning and wipes will be redone until the contamination is below the FNAL regulations. Once the hybrid substrates are certified as non-contaminated, there will be 10 hybrids kept at FNAL, 10 hybrids shipped to KU for mechanical testing and the rest shipped to CSUF to prepare for build. The hybrids kept at Fermilab will be assembled in house and used for initial electrical testing.

#### *Bare hybrid mechanical testing at KU*

There will be 10 hybrids fully tested. The primary measurement will be the flatness of the substrates. This measurement will be done on a CMM for each substrate and is expected to take about 5 minutes per part. The outside profile will be checked on a fraction of the parts using a machined gauge or a caliper. They will then undergo a more rigorous inspection using a CMM. Mechanical certification (yes/no) will be entered in the D0 database for each substrate at this point. These 10 parts will remain at KU for full electrical testing.

### *Bare hybrid electrical testing*

There are several initial tests. These tests include: a visual inspection, short to ground tests, continuity tests, and pad-to-pad short tests. All hybrids will undergo a visual inspection and a short to ground test. The 10 hybrids remaining at KU for mechanical tests will also be fully probed for continuity and pad-to-pad shorts. Depending on time constraints a few of the hybrids at Fresno will also be fully probed.

During the visual inspection, the quality of the visible top and bottom layers will be examined using a microscope. The size and appearance of the solder pads, AVX connector attachment pads, and SVX4 die pads will be examined.

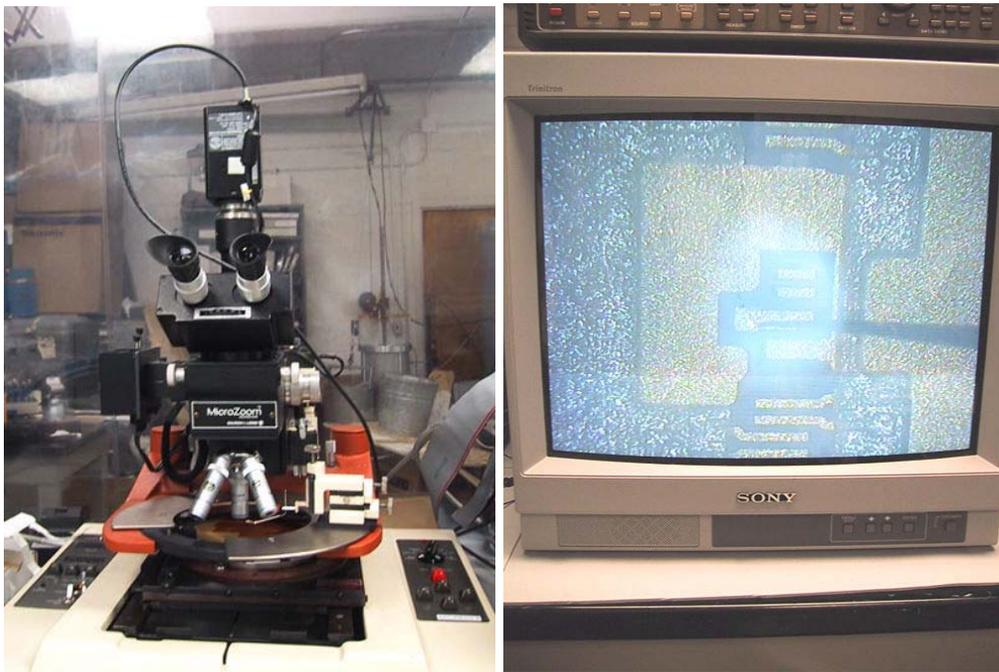


Figure 1. Rucker and Kolls 683A Semiautomatic wafer prober and display of L1 bare hybrid being tested at KU.

Both KU and CSUF have probe stations for conducting the electrical tests on bare hybrids. Figure 1 shows the KU probe station. These probe stations are controlled through a LabView program and allow an Excel spreadsheet describing the measurements of each hybrid to be written out. With the probe station the continuity and short tests are performed. The hybrid is aligned on the probe station and the testing procedures given on the KU hybrid testing web page are followed. The resistance of each pad to ground is measured and written out. Values below 300 Ohms are considered to be shorted and are flagged and that hybrid is retested manually for those pads. If the result is verified, the hybrid fails the test. For the continuity tests, values of the resistance less than 10 Ohms are required. Typical values of these resistances are less than 4 Ohms. Defects found in these tests are also verified manually before the hybrid is

failed. Any open or short is considered to fail the hybrid. Failed hybrids are gathered and either sent back to the vendor or sent to Fermilab to be used as mechanical prototypes according to the purchasing agreements. Hybrid substrates which pass these electrical tests will be combined with other components and documentation into build kits for delivery to the hybrid assembly (stuffing) vendor.

### ***Hybrid assembly***

The assembly (stuffing) of the hybrid includes the attachment of the passive components, SVX4 chips (die), and connector. This work will be done at NXGen and we anticipate only one production run with all of the parts. The assembly must proceed in the following order: placement of the passive components (including Molex connector) with solder, attachment of the SVX4 die with epoxy followed by connection of the hybrid to each SVX4 die with aluminum wedge bonding. All bare hybrid substrates and components are catalogued by CSUF and shipped directly from there to the assembly vendor.

Quality control adds a few more steps to the above. High yield and low volume characterize our project in comparison to how typical assembly vendors operate, which is high volume with less need for high yield. In validating our vendors we present to them the procedures outlined below. In addition to other documentation the vendor will record the identification number and location of each die for each hybrid, as well as data concerning the assembly of the batch of circuits in general, such as oven temperatures and wire bond adhesion measurements. One major request of the vendor is to check each hybrid with a simple ohmmeter continuity test to inspect for shorts to ground across the readout lines. This test occurs after the placement of passive components, where solder can sometimes cause shorts across components that are hard much harder to trouble shoot after full assembly. We anticipate that 105 hybrids will be put in one lot for the stuffing run. The vendor should verify on a pilot run of 5 hybrids that the oven temperatures are correct for the surface mount. We also request several pull tests on these 5 hybrids with the results reported before the batch of 100 is run for stuffing and wirebonding.

Finally we have tight requirements on shipping. The wire bonds are quite delicate and we do not encapsulate them, as is standard practice in industry, due to the potential need for rework after assembly. The shipping containers will each contain one or two assembled hybrids and will be designed for easy access and loading, with special attention given to protecting the delicate wire bonds.

Table 1: Hybrid Assembly Process at Vendor

<b>processing steps</b>	<b>description</b>	<b>documentation</b>
Audit of kits to supplied BoM	Must supply Bill of Materials (BoM). Version numbers should be obvious on parts, and BoM should also have a version number. Vendor will verify all counts.	BoM, drawings, gerber files, shipping instructions, specifications
Visual inspection of hybrid circuits		
Wire Bond Pull tests	Test wire bonding on unused part of circuit (test one or two circuit boards from lot) Results will be included in run card documentation.	
<i>Surface mount (SMT)</i>		
apply solder paste w/screen	Vendor will make screen for solder paste using Gerber files produced from the CAD program. Specified solder paste is Sn62/Pb36/Ag2.	Gerber file
pick and place (automated)	Pick and Place machine uses Gerber file for part placement and denoting fiducial markers for the automated visual alignment. Machine also verifies value of each component placed (resistor or capacitor).	gerber file
put through oven	appropriate temperature profile is documented in run card. Reflow maximum temperature is 205 to 200 °C for approximately 20 seconds.	specifications
SMT visual inspection		
continuity test	test for shorts to ground of cable out pads. If short found send to rework technician to remove and hand replace component.	supply test board
<i>Die attach</i>		
visual inspection of die		
application of epoxy	Use conductive epoxy	specifications
hand placement of die	Die (chip) attachment is done by hand due to the close separation and need for documentation of position	
bake out epoxy	Specify oven temperature and duration	

<i>Wire Bonding</i>	must supply printed map of wire bonds- drawings color is useful	
Clean bond pads	Ar plasma	
	wire bonding	
	visual inspection	
Packing	place in shipping containers supplied with kit (much care with open wire bonds!!)	detailed instructions
Shipping		

Table 4 lists the process control at the vendor.

### *Initial Functionality Testing*

After CSUF receives the hybrids from the assembly vendor, they will ship 50 of them to KU and keep 55 of them at CSUF for functionality tests. CSUF and KU are responsible for all interaction with the vendors, for the performance of the initial functionality tests, and for minor repairs on the stuffed hybrids. These tests will use the SASEQ teststands described in the Run2b Silicon TDR. All test results will be entered into the database. The following steps will be performed on the stuffed hybrids. All tests will take place in a clean room environment.

The visual inspection is done using a high-powered microscope. The purpose is to obtain quick feedback for the stuffing vendors, including wire bonder general problems (too-long tails for example) and to attempt to ameliorate any problems before electrical tests. Typical ``repairs" at this point may include manually straightening out crushed bonds, identify missing or broken wire bonds for repair in-house, locating SVX4 chips with obvious defects, and also to blow off or pick off debris from previous handling. A K&S manual wire bonder is available at both university hybrid testing sites for these quick repairs.

After the visual inspection, there will be a static electrical test to check for power shorts and to verify the connection of the platinum temperature measuring resistor. Hybrids with shorts will be set aside for possible debugging. The functional electronic readout tests are performed using 1 SASEQ stands at each university. This is the basic test of download and readout. We require 100 successful downloads, and error free readout of 10,000 calibration and pedestal events. In addition one cycle (requiring about 15 minutes per hybrid) of the standard burn-in test as described below is performed.

Download failures, are if possible, localized to a single chip using a manual probe station in conjunction with an oscilloscope and logic analyzer, and defective SVX4 chips marked for replacement. Hybrids with problems are scanned at high magnification (50-250X) to

search for chip and other defects. For the Run2a hybrids, in about 50% of the download and readout failures cases, a SVX2 chip flaw was visible. For the Run2a production:

- Debugging success was anecdotally stated to be >70%, meaning that at least 70% of download and readout failures, when localizable to a single chip, could be recovered.
- About 30% of the hybrids with shorts were recovered, in some cases by burning off debris at "high" current (less than 1A in order not to melt wire bonds), or by manipulation of hybrid tails.

The initial yield of working hybrids that were stuffed for Run2a was 70% and varied significantly between different hybrid types and batches. This yield implied that it was cost effective to ship the stuffed and wirebonded hybrids to universities for the initial functionality test. The university collaborators would then debug the non-functional hybrids. The eventual yield for working hybrids that were stuffed was around 90%. The plans for testing are being prepared assuming yields such as those found in Run2a for the stuffing and wirebonding vendors.

#### *Burn-in Tests for hybrids at KU*

The burn-in test is a part of the standard testing procedure during module production. It is the primary Quality Assurance testing suite used to certify and "rate" hybrid quality. It will be performed first on the stuffed hybrids after they pass the initial functionality test. At this point the goal of the test is to select good hybrids for module assembly. The idea of the initial burn-in test is to run every component for a period of 48 hours at elevated temperature and monitor its performance. In particular, measure pedestals, total noise, random noise and gain and examine occupancy in the sparsification mode. Other parameters that will be monitored include temperature and chip current. Typical problems that are revealed by the burn-in test are SVX chip failures, broken and shorted bonds, grounding problems, noisy strips, etc. Students at KU will perform the tests and then the lead physicist will grade the hybrids according to the number of dead and noisy channels after the burn-in test. The burn-in station is capable of running 6 hybrids at a time. Each week, KU can burn-in 18 hybrids. KU will ship the working hybrids to FNAL each week.

The different tests performed during burn-in are the following:

- o Temperature sensor test: performed at room temperature, before the SVX chip is powered.
- o Data integrity check: tests the stability of the SVX chip downloading and the correctness of the individual chip identification number (ID) and channel numbers in the SVX data.
- o Long burn-in test consists of a number of runs with an idle interval between them in which the chips remain powered. In each run, the SVX chips are tested in "read all" and "read neighbor" modes. In "read all" mode, chip pedestals are read out to evaluate the noise in each SVX channel and then chip calibration is performed. In sparsification ("read neighbor") mode, where only the channels whose response exceeds the preset threshold and their immediate neighbors have to be read out, the frequency of false readouts is studied.

For a detailed description of the tests performed during burn-in in Run2A, see d0note 3841. We plan to run the same tests during Run2b.

### *Schedule*

Currently, expected delivery of bare hybrids from Amitron is late July, 2004. The schedule assumes 2 weeks for the hybrid wipe tests at FNAL. Hybrids should be shipped to both KU and CSUF 2 weeks after delivery to Fermilab. The anticipated build date at NXGen thus starts 4 weeks after receipt of bare hybrids. Before starting the build, preliminary tests at FNAL and KU should be available. We assume that the stuffing vendor will take 4 weeks upon receipt of the package. Assuming that functional testing takes 2 weeks after that, the first available burned-in hybrids will be available for module builds 10-12 weeks after delivery of bare hybrids. Burn-in at KU is assumed to take 5-6 weeks if there are no significant repairs needed.

## Hybrid Traveler

**Hybrid #** \_\_\_\_\_

**Build Kit #** \_\_\_\_\_

Procedure	Name	Date	Comments
Received at Fermilab			
Be wipe OK			
Mechanical meas.			
Bare hybrid probe			
Shipment to Stuffing Vendor			
Short test at stuffing vendor			
Wirebond pull test			
Shipment from Stuffing Vendor			
Received at CSUF			
Shipped for I.F.T			
Initial Functionality Test (IFT)			
Shipped from IFT			
Received at Fermilab			
Fermilab Initial Test			
Burn-in			
Certify & Rate			

SVX4 chips used: