Layer 0 Silicon Detector Electronics for the D-Zero Experiment

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1. INTRODUCTION

A new inner layer silicon detector is being constructed for the D0 experiment at Fermilab. [1] This detector is designed to fit inside the existing Run2a detector and will utilize much of the existing infrastructure as well as the new electronics and readout designed for the cancelled Run2b silicon replacement. The current D0 Silicon Tracking detector consist of 12 disks positioned between six 4-layer barrel structures. Figure 1 shows an end view of the current detector with the new Layer 0 superimposed in the center.

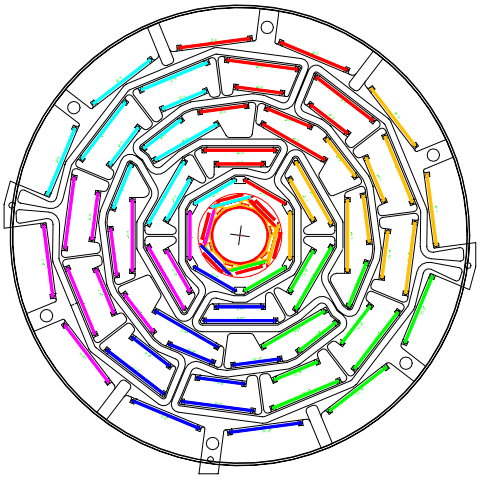

Figure 1: South End View with Layer 0 superimposed in center.

Layer 0 must be able to slide over a beam pipe and associated mounting flanges that have a diameter of 30.48 mm. The detector is also required to maintain ~1 mm separation from the beam pipe to limit capacitive pickup of noise. The new detector must also clear the inner most layer of the current detector constraining the overall diameter to 44.04 mm. Given the tight mechanical constraints the detector is designed to maximize acceptance (98.5%) and readout segmentation. Hybrids are located outside of the active volume and are connected to the sensors with fine pitch analog cables. Z segmentation is limited to eight sensors of 7 and 12 cm lengths by the radial buildup of the cable bundles. This arrangement provides better segmentation near Z=0 and equalizes the load capacitance by having lower sensor capacitance on the strings with longest analog cables. Figure 2 is an enlarged end view of Layer 0 illustrating sensor positions.

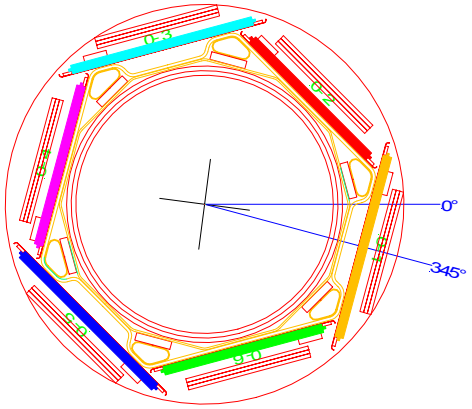

Figure 2: Layer 0

2. INSTRUMENTATION

Layer 0 SVX4-based instrumentation is designed to operate within the constraints of the currently installed SVX2 data acquisition system. Newly designed components consist of silicon sensors, pitch adapters, analog cables, hybrids, digital jumper cables, junction cards, twisted pair cables, and Adapter cards.

2.1 Sensors, Pitch adapter

Layer 0 is composed of 48 silicon sensors manufactured by Hamamatsu. Inner radius positions utilize 71μm pitch sensors while 81μm pitch sensors are used at larger radius positions. Two lengths of sensors will be used, 70 mm and 120 mm. A single cable pitch is accomplished by utilizing ceramic pitch adapters mounted on the sensors that also carry decoupling capacitors.

A number of Run2b studies have established that low coherent noise can be achieved by good low inductance ground connections to the support structure. [2] This is accomplished by co-curing mesh ground planes onto the carbon fiber support structure and utilizing low inductance flex circuits which carry bias and ground from the bottom to the top of the sensors.

2.2 Analog Cables, Hybrids, SVX4

The analog cables are flexible circuits manufactured by Dyconex. The cable lengths vary, with the longest at 34.3 cm, and have a capacitance of .35 pF/cm. Table 1 shows the calculated electrical parameters at various Z locations. The signal/noise is roughly equal at each Z location with adequate signal available for tracks incident at the extreme edges of the detector for reliable readout and reconstruction.

	Z1	Z2	Z3	Z4
Detector length (cm)	7	7	12	12
Strip pitch (microns)	71	71	81	81
Active width (mm)	18.18	18.18	20.74	20.74
Radius (inner)	16.10	17.60	16.10	17.60
Max angle (radians)	0.51	0.48	0.57	0.53
Analog cable length (cm)	34.3	31.7	24.1	16.5
Total capacitance (pf)	20.4	19.5	22.8	20.2
Total noise(electrons)	1419	1378	1528	1407
S/N (normal inceidence)	16.2	16.7	15.1	16.3
S/N (edge)	7.3	8.1	7.0	8.2

Table 1. Electrical parameters of the Layer 0 detector.

The SVX4 [3] chip is a 0.25 μm silicon readout chip originally developed for the Run2b upgrades. These chips use a protocol similar to the currently installed SVX2 chips but operate with a single 2.5V supply rather than the three 3.3 – 5V supplies needed for the SVX2.

2.3 Digital Jumper cables, Junction Cards, Twisted Pair Cables

The chips are placed on a BeO ceramic hybrid. Each hybrid holds two SVX4 chips. Grounding of the SVX2 reference to the support structure is through vias plated through the hybrid to contacts on the co-cured flex circuit on the supports.
Digital signals from the hybrid are carried to the end of the support structure using a kapton flex digital jumper cable, coupled to twisted pair cable using a junction card located on the existing silicon support structure, and then interfaced to the existing readout using active circuitry on the adapter card mounted on the wall of the D0 calorimeter.

2.4 Adapter Cards, Isolated LV System

Layer 0 is a continuous conductor between the North and South ends of the detector and the potential exists for a serious ground loop encircling the D0 calorimeter. In addition to interfacing the 5V single ended SVX2 control signals to 2.5 differential signals needed for SVX4 the adapter card is also designed to isolate the Layer 0 detector from the rest of D0. Isolation is provided by utilizing the high impedance of the differential signals provided to the SVX4. In addition, a separate isolated 2.5 V supply drives the SVX4 chips. The isolation requirement is greater than 10 Ohms. Results on prototype adapter cards will be presented.

4. Summary

The Layer 0 detector is currently being constructed for installation in D0 during the summer of 2005. Prototypes, based on initial RunIIb upgrade plans, of all components have been received and tested. Grounding issues, to prevent system noise, has been investigated as well has response characteristics of the new SVX4 readout chip. Test results of the system will be presented.

REFERENCES

[1] D0 Collaboration, “D0 Layer 0 Conceptual Design Report,” October 28,2003.
[2] K. Hanagaki, Nucl. Inst. And Meth. A511 (2003) 121.
[3] L. Christofek, K. Hanagaki, M. Jun, D. Kau, P. Rapidis, M. Utes, “SVX4 User’s Manual,”D0 Note 004251.