

Identified High Risk Items for Silicon

SVX4: WBS 1.1.2.1

The SVX4 chip is the chip used to readout the silicon sensors. It essentially consists of an analogue front-end (FE) and a digital back-end (BE). The FE has been tested through a test submission to the wafer manufacturing plant, TSMC, in May 2001. The full chip with integrated FE and BE was submitted to TSMC early April 2002. Extensive simulations were run on the design to assure that the chip will perform as specified. The chip is designed in the 0.25 micron technology using industry standards. Because we use an industry standard process, manufacturing risks are minimized.

Risk Assignment:

0.8

Schedule risks:

Schedule risk is mitigated by including a second prototype chip submission to occur in November 2002. If the test chips from the April 2002 submission perform according to the specifications, the late Oct 2002 submission could produce production chips, which can be used in the final detector. The final chip submission is scheduled to occur mid-April 2003. Therefore a schedule contingency of 5 months exists. If a third prototype run is necessary to obtain a working chip, then the schedule-end date slips by 6 months.

Cost risk:

Two different cost risks have been identified: additional electrical engineering and production yield. The uncertainty in additional engineering needed to bring the chip within specifications is addressed by adding a 100% contingency to the cost estimate for the engineering at LBL. The uncertainty in the yield is addressed in three ways. First, a large set of spares is ordered. Secondly, a 50% yield for the wafer production is assumed, which is believed to be conservative. Thirdly, a 30% cost contingency is assigned to the cost associated with the production chips. It should be noted that this production run may not be needed in case the second prototype chip run yields acceptable chips.

Procurement risk:

Procurement risks are mitigated by using industry standard design rules.

Sensors for Layers 2 – 5: WBS 1.1.1.4

The major component of the detector is sensors for Layers 2-5. The delivery of these items drives our scheduled end-date. We have chosen single-sided sensors in order to reduce the technical risk in producing these items. This technology has been proven for over 10 years. The vendor we have chosen has an excellent reputation for delivering quality sensors very similar to the sensors we plan on using, on budget and on schedule for many other high energy physics experiments.

Risk Assignment:

0.6

Schedule risks:

Schedule risk is mitigated by including two sets of extra time for delivery of the sensors. First, the time allocated for sensor production has a time contingency of 6 weeks. That is, based on the promised production rate of the vendor, sensor production can be completed six weeks prior to the end date in the schedule. Secondly, the schedule assumes production not only of the sensors needed for the detector, but includes 20% spares. This corresponds to an additional 7 weeks of contingency. In addition, two months of float have been added into the schedule at the end. We have done an additional risk analysis on a disaster scenario outside of our schedule contingency. If a production batch at the company were to fail, containing about 300 sensors, the delay would be two months to the schedule end-date.

Cost risk:

We have existing quotes for these items so we have assigned a 30% contingency to the costs. We are currently negotiating to receive a reduced cost on these devices with the company as well.

Procurement risk:

We are using a proven vendor. If necessary, we can contract a second vendor.

Hybrids for Layers 2 – 5: WBS 1.1.2.4

We will be using a technology for hybrids that was successfully implemented by CDF for the Run2a silicon detector. The D0 hybrids will have 10 SVX4 chips to be readout. This requires having fully debugged SVX4 chips when they are mounted onto the hybrid in order to allow a sufficient yield for hybrid production. Most of the technical risks of the hybrids are thus tied to those of the chip. Multiple vendors are currently providing prototypes that will allow us to both test the hybrids and the vendor delivery schedules within the next few months.

Risk Assignment:

0.5

Schedule risks:

Schedule risk is mitigated through the inclusion of a second prototype run to occur concurrently with a second prototype chip submission. If there is no 3^d prototype chip run and a 3^d prototype hybrid run (not included in the present schedule) is necessary it has no impact on the schedule end date.

Cost risk:

Currently quotes are available for prototype hybrids including the bare hybrids, components, and stuffing and wirebonding. Even with the quotes for prototypes, we have assumed a 50% contingency on the cost. Also included in the cost estimate are funds for two sets of prototype runs before the production run.

Procurement risk:

Procurement risks are mitigated by using two separate vendors both for the bare hybrids and for stuffing and wirebonding the hybrids.

Analog Cables: WBS 1.1.2.5

An analog cable carries the charge from the silicon strips of the innermost layer, Layer 0, to the SVX4 readout chip on the Layer 0 hybrids. There are 288 of these cables needed with various lengths, the longest being 40 cm long. The pitch, trace width and length for these cables makes them difficult to fabricate. An R&D program started with these cables last year. We currently have two potential vendors for producing these cables. The first prototypes received from one company had problems with open traces and problems with wirebonding. A second set of prototypes of these cables is currently being tested and we are procuring a first set of prototypes from the second vendor. The risks associated with these cables include: having higher noise because the trace width and pitch cannot be controlled successfully resulting in a larger trace capacitance; having a large fraction of non-working channels due to production problems; coherent noise associated with the layout of these cables in the mechanical structure. We are working with the vendors to help mitigate the first two risks. The coherent noise problem are being addressed by performing a series of tests on the bench to optimize the layout of these cables.

Risk Assignment:

0.4

Schedule risks:

Production is scheduled for January, 2003 for these cables and it is a four month process. There is a one year available float for having these cables completed without affecting the end-date of the project.

Cost risk:

We assume that we will have at least 3 more prototype runs in the cost estimate. Also, there is a 50% contingency assigned in both prototyping and production although we have quotes for production cables.

Procurement risk:

Procurement risks are mitigated by using two different vendors. If necessary, we have a third vendor, which CDF is researching, to provide their analog cables.

Layer Zero Support Structure: WBS 1.1.3.2.1.1.2

The layer 0 support structure will be built out of carbon fiber with cooling channels embedded. The structure has to support the sensors to high mechanical accuracy and allow cooling of the hybrids mounted on the end of the structure. The University of Washington has the primary responsibility for engineering this structure. Their mechanical engineers have worked extensively with carbon fiber structure for aerospace industry. There are challenges both in the design and the production of this structure. Currently a full length prototype structure has been assembled. Many finite-element and other simulations have been performed to test the design. These simulations have been cross-checked using data from cooling, thermal, and mechanical tests to show their correctness. Further simulations and tests will be done as the prototyping and production process continues.

Risk Assignment:

0.3

Schedule risks:

Because the end-date in the schedule is driven by the assembly of the outer layers, there is significant float in the schedule for assembly of the Layer 0 support structure. The structure is scheduled to be ready in June 2003, but modules don't need to be mounted on it until March of 2004 so a float of 8 months exists.

Cost risk:

The cost risk associated with this item is having to add additional mechanical engineering resources. We have added a 60% contingency to the cost estimate for the this engineering.

Procurement risk:

These items are being built by D0 collaborators. Currently a prototype module exists. If necessary, Fermilab can help to build this device in Lab 3.

Adapter Cards: WBS 1.1.2.13

The adapter cards contain the active elements that allow signals to be sent to the SVX4 chip, and signals processed coming from the SVX4 chips. They provide the power regulation as well as the impedance matching. For the Run2a silicon detector, the interface boards performed a similar function. We have chosen to use the same electrical engineering team at Kansas State University to build these cards that designed and built the interface boards for Run2a. Their team has extensive experience with the types of problems that may be encountered. However, extensive prototyping and testing will be needed as soon as the SVX4 chip is available. Therefore, the risks associated with this item follow those of the SVX4 chip.

Risk Assignment:

0.5

Schedule risks:

Although the production cards are not needed until the detector is mounted into the D0 experiment during the scheduled shutdown, extensive testing is needed to ensure reliable operation of these boards. There are 2 prototype rounds in the schedule with the production starting in late October, 2003. If a third round of prototyping is required, it has no effect on the scheduled end-date.

Cost risk:

The main cost risk is for additional electrical engineering. Two rounds of design have been costed with a 50% contingency.

Procurement risk:

Many companies can produce these boards and few problems are anticipated.