‘Status and Scope DØ Run 2b Silicon Tracker’

Fermilab PAC Meeting
April 12, 2001

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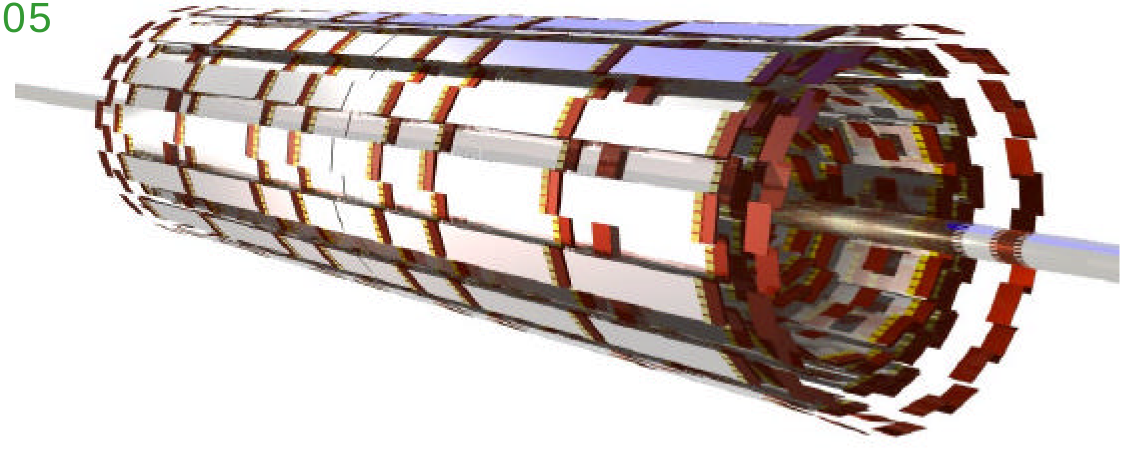
For the Run 2b Silicon Group

Outline

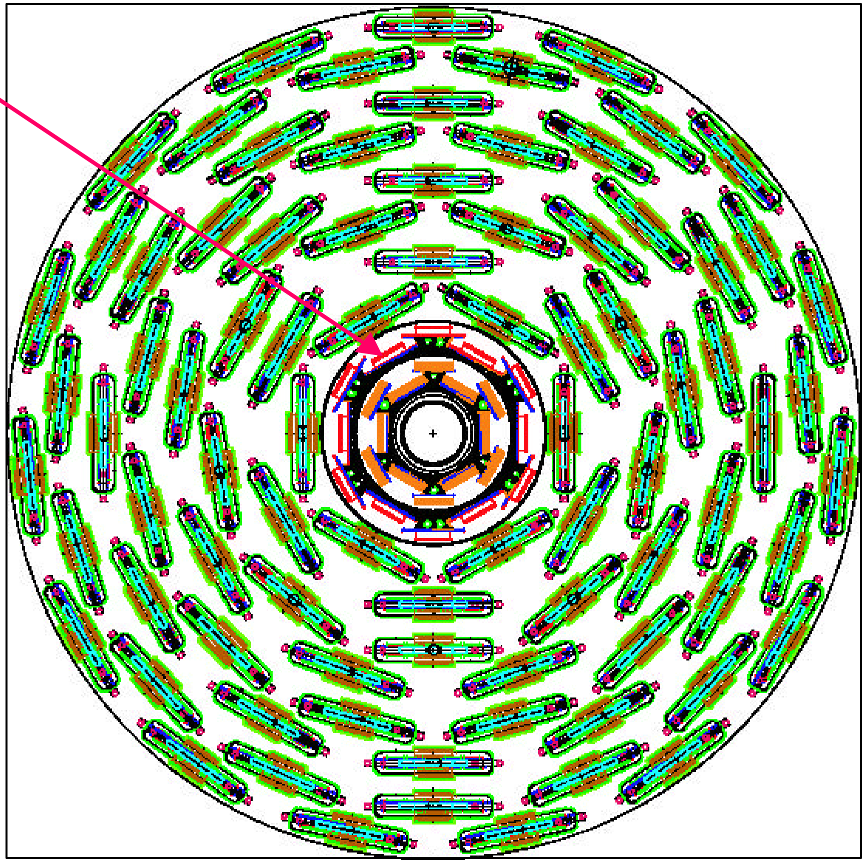
- Brief reminder of design
  - No change in overall layout of the detector
  - Changes in sub-components
    - » Advancement of design
      - cooling layer 0 hybrids
    - » Better performance
      - details of stave design
    - » Easier design
      - Eliminated fingers on hybrid
- Schedule
  - Completion May-June ‘05
- Scope



Picture based on Geant Model

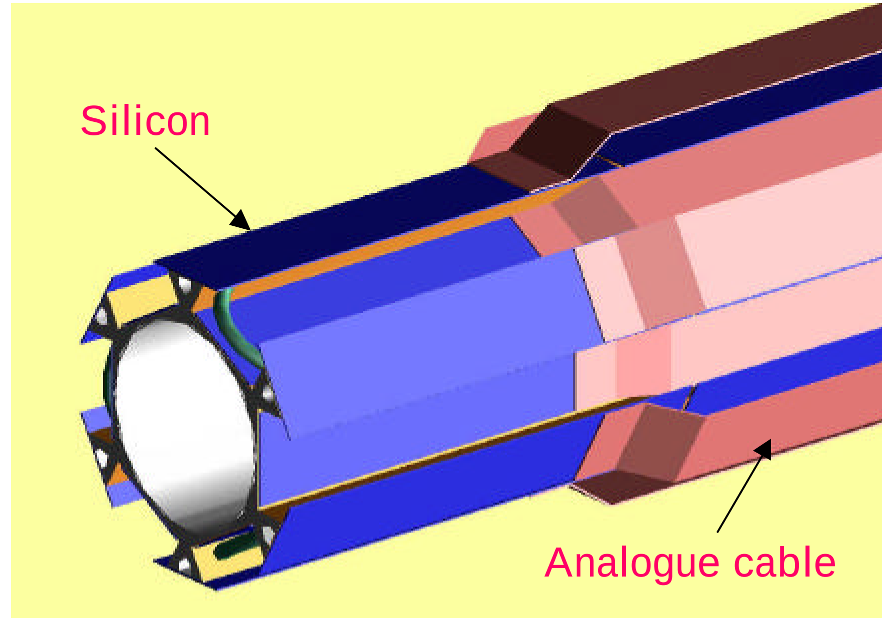
Basic Layout

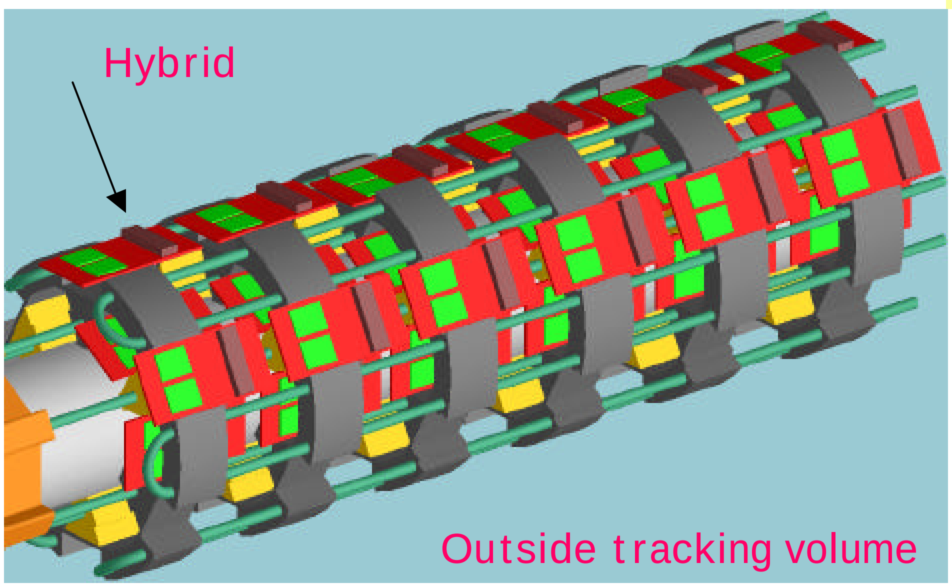
- Six layer silicon tracker, divided in two radial groups
  - Inner layers: Layers 0 and 1
    - » Axial readout only
    - » Mounted on integrated support
    - » Assembled into one unit
    - » Designed for V_{bias} up to 700 V
  - Outer layers: Layers 2-5
    - » Axial and stereo readout
    - » Stave support structure
    - » Designed for V_{bias} up to 300 V
- Employ single sided silicon only, 3 sensor types
  - 2-chip wide for Layer 0
  - 3-chip wide for Layer 1
  - 5-chip wide for Layers 2-5
- No element supported from the beampipe
- Drilled Be Beampipe with ID of 0.96”, 500μm wall thickness



Layer 0

- Support Structure
  - 12-fold castellated geometry
  - carbon fiber support
  - possible use of pyrolitic graphite
  - sensors cooled to T=-10 ^{o}C
  - R_{in} = 18.5 mm

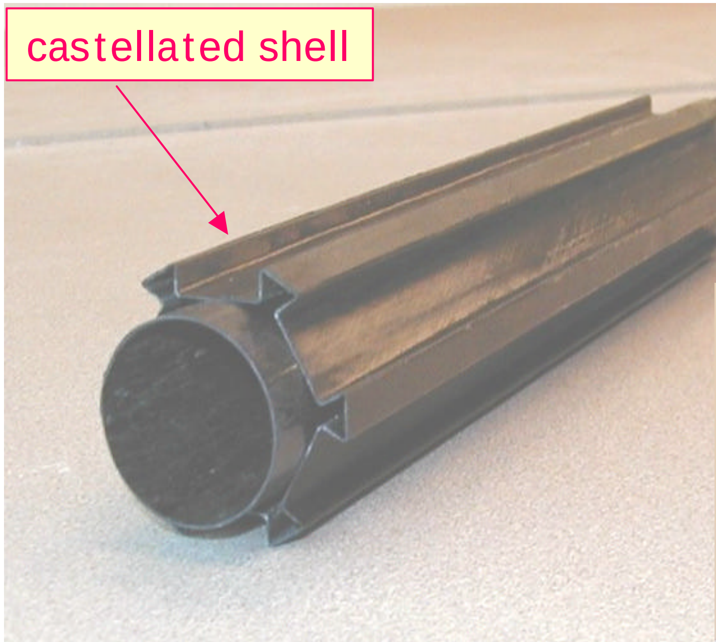


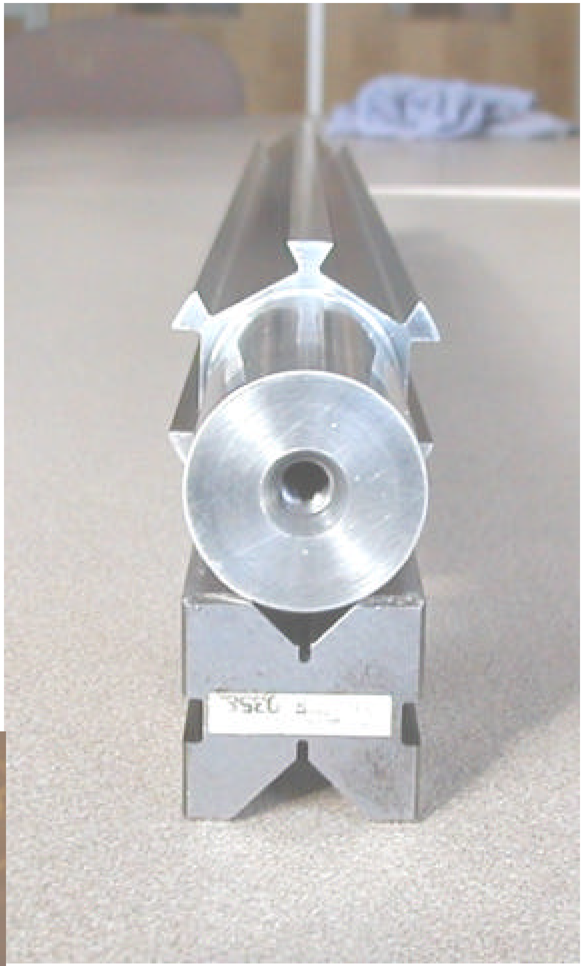


- Assembly
  - 2-chip wide sensors
  - 25 mm pitch, 50 mm readout
  - Analogue cables for readout
  - Hybrids off-board
  - Staggered in z for 6 readouts per end per phi-sector
- Space is extremely tight !

Layer 0 Support Structure

- Prototype support structure made by University of Washington
  - Castellated mandrel
    - Stacking sequences
      - Cylindrical Shell: 3 ply 0º, 90º, 0º laminate
      - Castellated Shell: 6 ply $[0^{\circ}, +20^{\circ}, -20^{\circ}]_s$ laminate
  - RTV pressure strips, vacuum bag
  - Pressured to 85 psi
  - Cured in autoclave at 275 °F

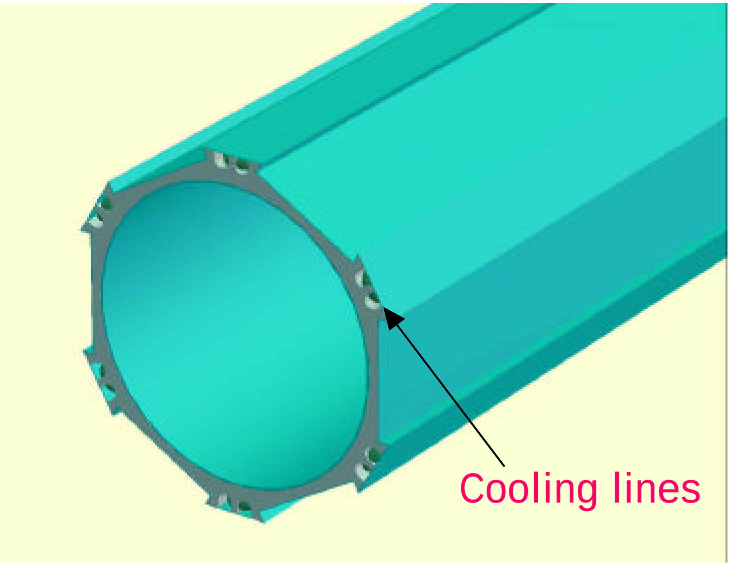


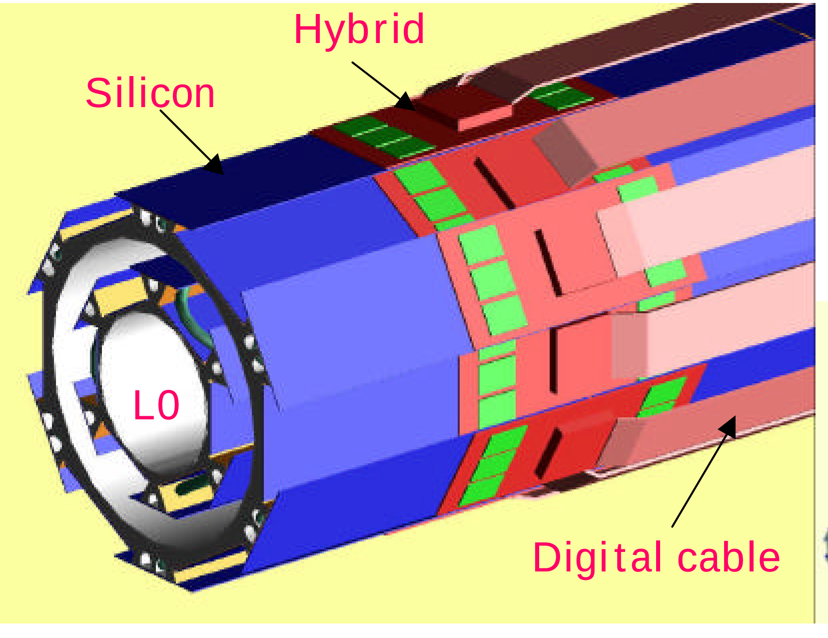


Measurements and comparisons of elastic properties of prepreg. laminates

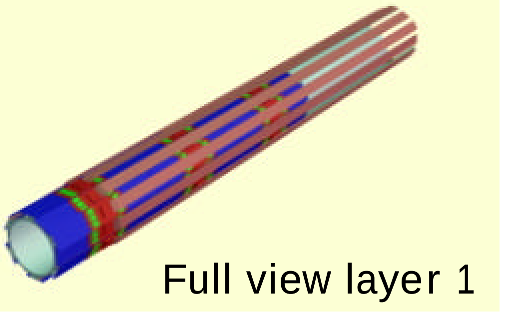
Layer 1

- Support Structure
  - 12-fold crenellated geometry
  - carbon fiber support
  - Integrated cooling
  - R_{in} = 34.8 mm



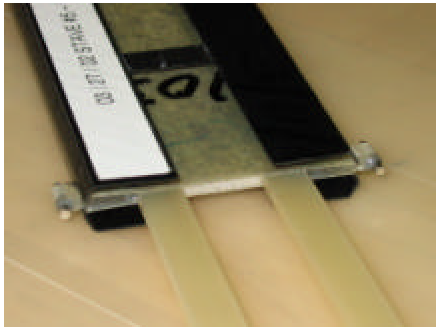


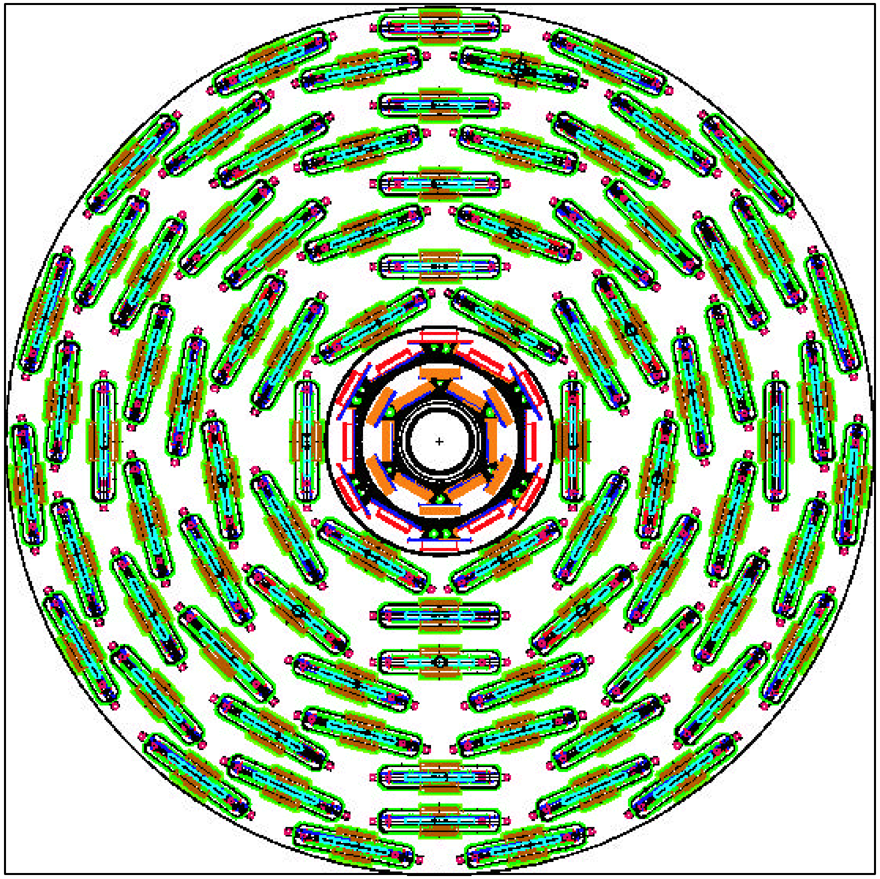
- Assembly
  - 3-chip wide sensors,
    58 μm pitch, axial readout
  - Hybrids on-board
  - 6-chip double-ended hybrid readout



Layers 2-5

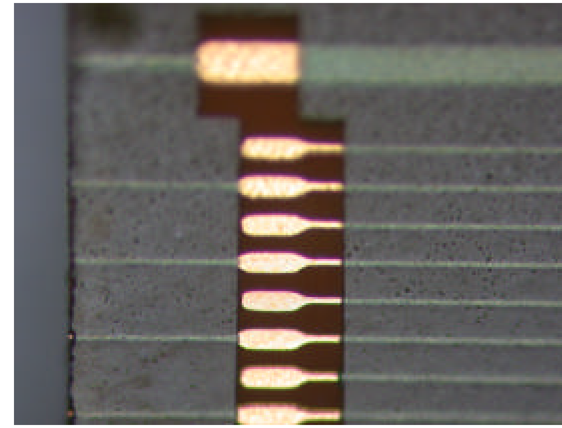
- 12, 18, 24 and 30-fold geometry
- All layers:
  - 5-chip wide sensors, 30 μm pitch, 60 μm readout
  - Hybrids on-board
  - 10-chip hybrid readout
  - Stereo and axial readout
  - Stereo angle obtained by rotating sensor
- Support
  - Modules are assembled into staves
  - Staves are positioned with carbon-fiber bulkheads
- Steady progress on stave design

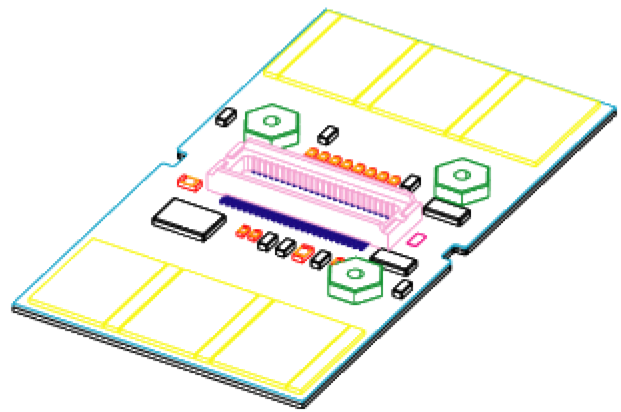


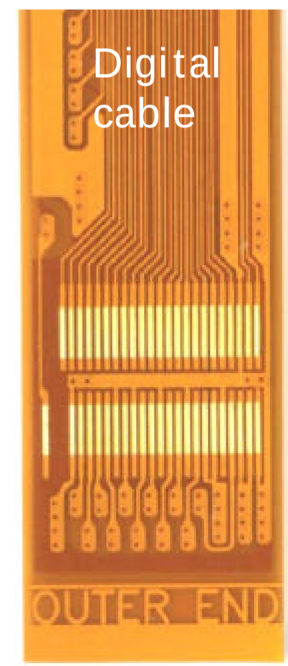


Silicon Readout

- SVX4
  - Submitted (finally) to TSMC on March 28
  - SVX4 Test cards to qualify chip, design finished
- Analogue cable
  - Low mass, fine pitch cables to bring analogue signals outside of tracking volume
  - Technically challenging
    - **Trace width ~ 10 mm, pitch 100 mm**
    - **C ~ 0.4 pF/cm**
  - Two vendors
    - Dyconex (2nd prototype)
    - Compunetics
- Hybrids
  - Common technology with CDF
  - First hybrids delivered
- Digital Cable
  - Two vendors: Honeywell, Basic Electronics
- Adapter Cards
  - Design nearing completion







Progress

Component	Vendor	Design	First Prototype		Second Prototype	
			Ordered	Delivered	Ordered	Delivered
L0 Sensors	ELMA	✓	✓	✓		
	HPK	✓				
L1 Sensors	ELMA	✓	✓			
	HPK	✓	✓			
L2 Sensors		✓				
Analogue Cable	Dycx	✓	✓	✓	✓	✓
	Comp	✓	✓			
L0 Hybrid						
L1 Hybrid		✓	✓			
L2A Hybrid		✓				
L2S Hybrid		✓				
Digital Cable	Honey	✓	✓	✓		
	Basic	✓				
Junction Card		✓	✓	✓		
Twisted Pr. Cable		✓	✓	✓		
Adapter Card						

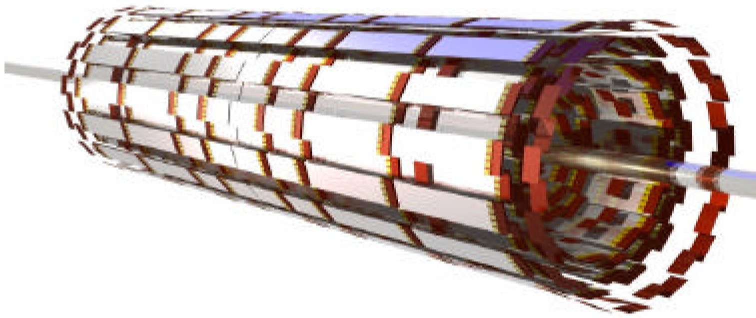
- Expect to have full scale prototype of all elements by this fall

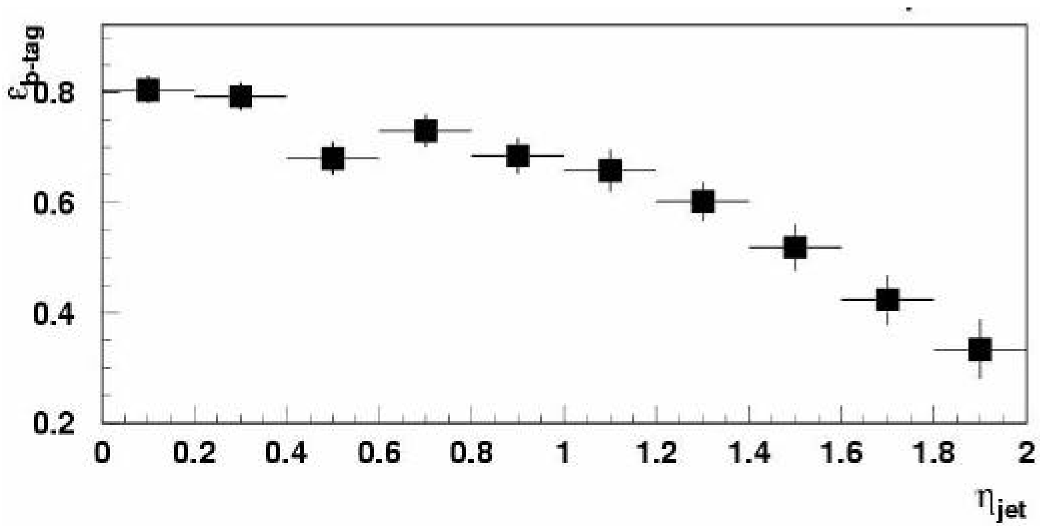
Alternate Designs with Reduced Scope

- Given that many elements are already in prototype stage, reduced scope obtained by omitting various element
- No re-optimization considered
  Would set project back by at least 6-9 months
  - Variation of radii, width of sensors
  - different type of sensors
  - …
- Options considered for reduced scope
  - Omission of Layer 4
  - Omission of Layer 1
  - Omission of sensors at large |z|
- Folding in realism

Reference: TDR Design

- Fiber tracker has full coverage up to $|\eta| < \sim 1.6$
- Require silicon stand-alone tracking for $|\eta| > \sim 1.6$
- Studies based on full Geant simulation
  - b-tag: signed impact parameter, $E_b > 20$ GeV
    - » Track selection
      - within cone $\Delta R < 0.5$ of b-jet
      - $p_T > 0.5$ GeV/c, good χ^2, hits in silicon ≥ 2
    - » Impact parameter significance
      - 2 tracks: $d_0/\sigma(d_0) > 3$
      - 3 tracks: $d_0/\sigma(d_0) > 2$



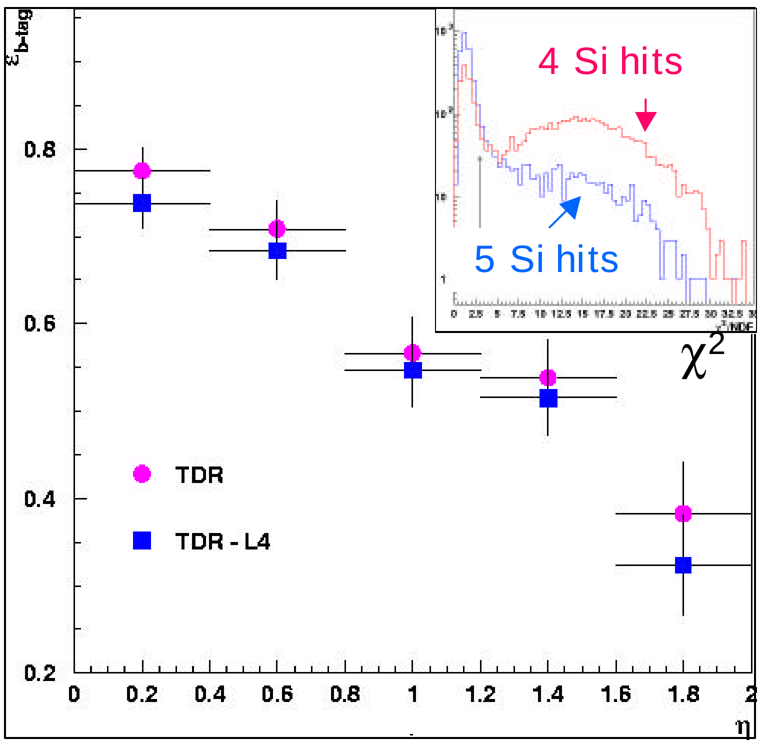


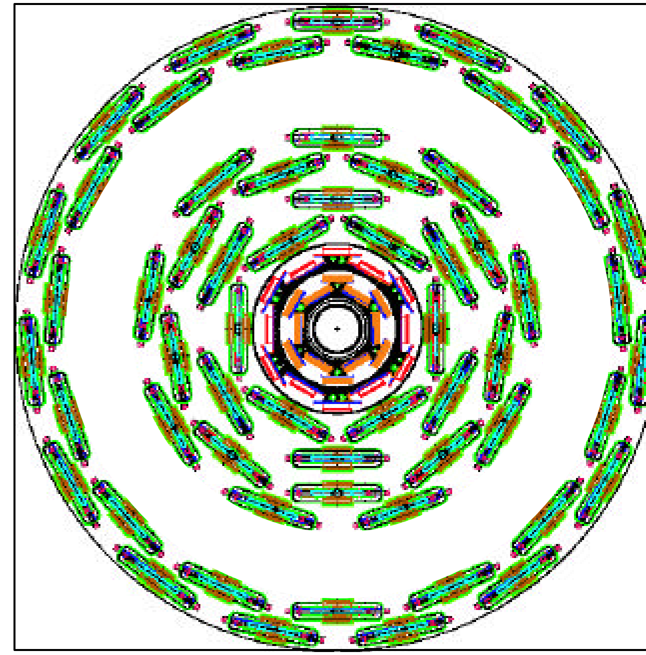
	TDR
$P(n_b \geq 1)$	76%
$P(n_b \geq 2)$	29%
Mistag Rate	< 1.5 %

Based on WH-events, with b's falling within acceptance

Omission of Layer 4

- Consider CFT+SMT tracking
  - One stereo measurement less
  - Tracking efficiency and b-tagging eff. degraded
  - But double number of tracks with poor quality (pattern recognition)



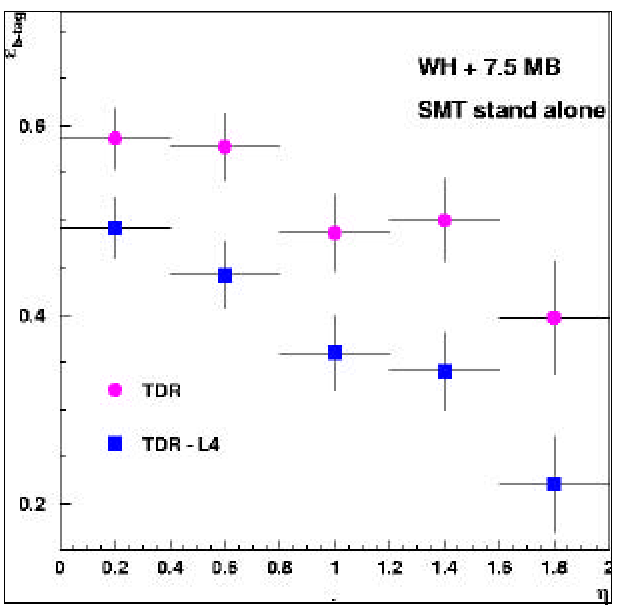


	TDR - L4	Rel. ε Loss
$P(n_b \geq 1)$	73%	3.2%
$P(n_b \geq 2)$	26%	10.3%
Mistag Rate	< 1.5 %	

In addition lose 2% in lepton id.

Omission of Layer 4

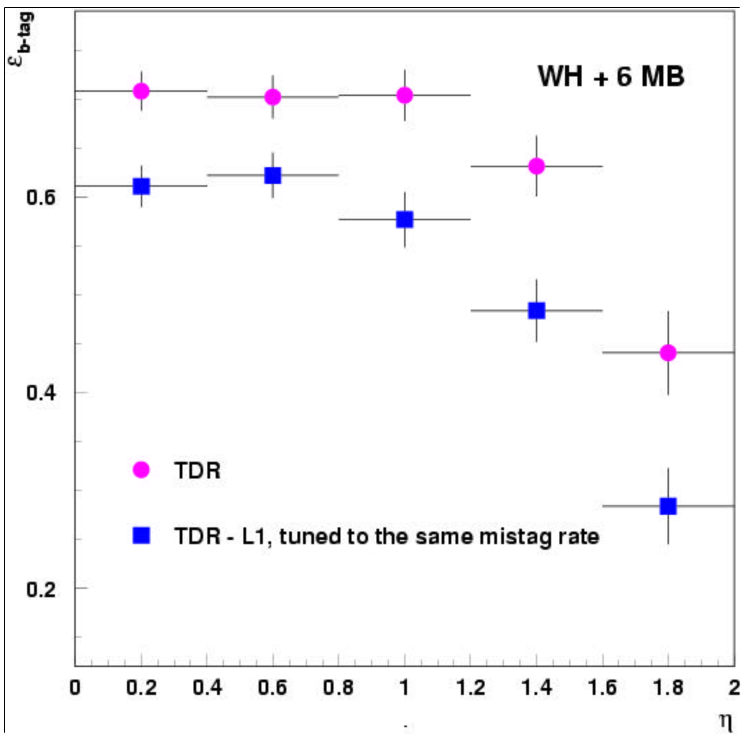
- Consider Silicon Stand-Alone tracking
  - Important in forward region with no full coverage of CFT
  - Important in lepton identification
  - Important tool for consistency checks
- Tracking efficiency and fake rate
  - Fake rate: factor 10 larger for tracks with 4/5 (TDR-L4) compared to 5/6 hits
  - At same fake rate
    - » Central region reduction of: track finding eff. by 10%, b-tag eff. by 20%
    - » Forward region reduction of: track finding eff. by 22%, b-tag eff. by 40%



	TDR - L4 (SA)	Rel. ε Loss
$P(n_b \geq 1)$	61%	19.3%
$P(n_b \geq 2)$	18%	38.0%

Omission of Layer 1

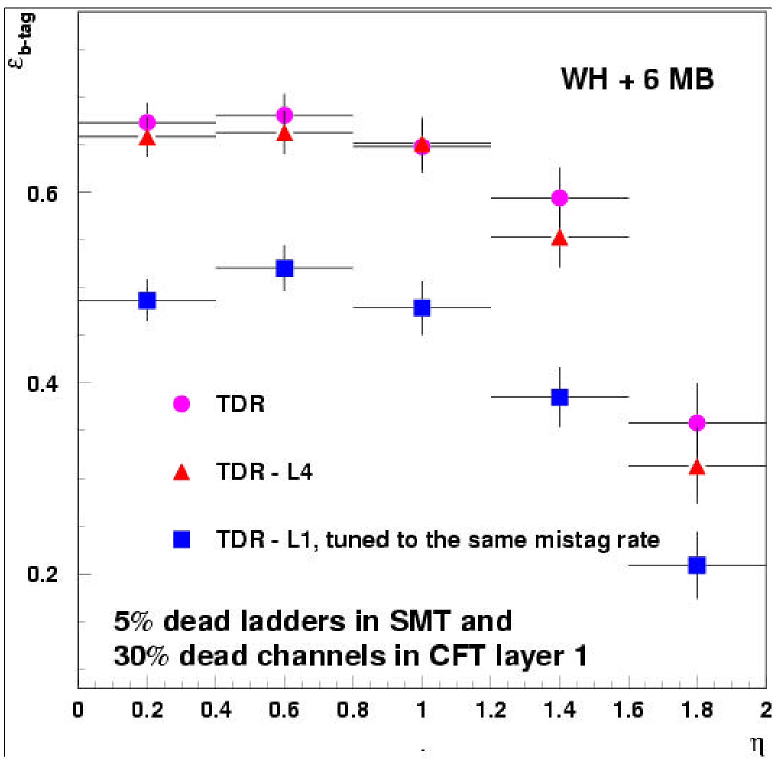
- A priori undesirable
  - Layer 1 also a contingency in case problems encountered with layer 0
    - » Deterioration of impact parameter measurement by ~10% for L2-L3 system
- Mistag rate doubles if layer 1 removed. Compare using same mistag rate

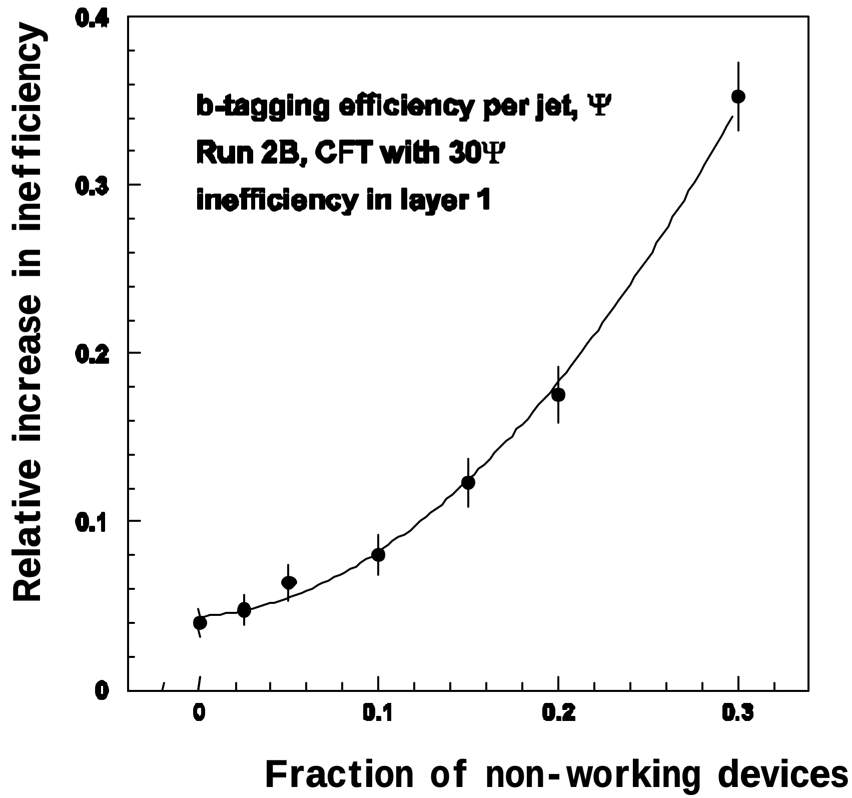


	TDR - L1	Rel. ε Loss
$P(n_b \geq 1)$	66%	12.2%
$P(n_b \geq 2)$	22%	24.0%
Mistag Rate	< 1.5 %	

Folding in Realism

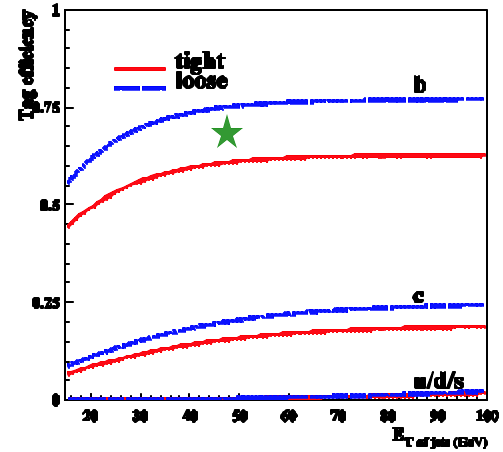
- So far assumed detectors are perfect; reality, however, is different
  - Example: Run2a silicon detector
    - » Barrels / F-disks / H-disks: 93%, 96%, 89% functioning devices
- Assume certain fraction of Si ladders dead, 30% inefficiency in CFT lyr 1
  - effect on b-tagging efficiency





Summary on Scope

- TDR design:
  - b tagging efficiency of ~65%
  - Higgs working group simulations assume even higher b-tag efficiencies
- Omission of any element would significantly affect physics reach and diverge from the basis of justification for Run 2b
  - b-tagging efficiencies would fall below 50%, especially if analyses would require tighter tagging algorithm
  - 20% loss in luminosity on 15 fb^{-1}, 5 GeV reduction in reach on m_H (115-135 GeV)



Alternative Design		D Lumi	D Running time (months)
TDR - L1		-24% (w/o ineff.) -44% (w/ ineff.)	8.6 15.9
TDR - L4	Global Tracking	-12% (w/o ineff.) -14 % (w/ ineff.)	4.4 5.0
	SMT stand-alone	-38%	13.7
TDR - z		-27%	9.7

Assuming 12 fb^{-1} /3yrs

Summary

- Project is well into prototyping phase; significant progress has been made over the last 5 months
- Results from our studies indicate that all baseline elements are necessary to address physics opportunities of Run 2b
- Given the narrow window of opportunity, any reduction in scope would adversely affect the justification for Run 2b
- Project is well positioned to present
  - Current full scale design
  - Schedule
  - Resource estimates
  - Project cost estimate

  to the review committees to get this silicon detector baselined.