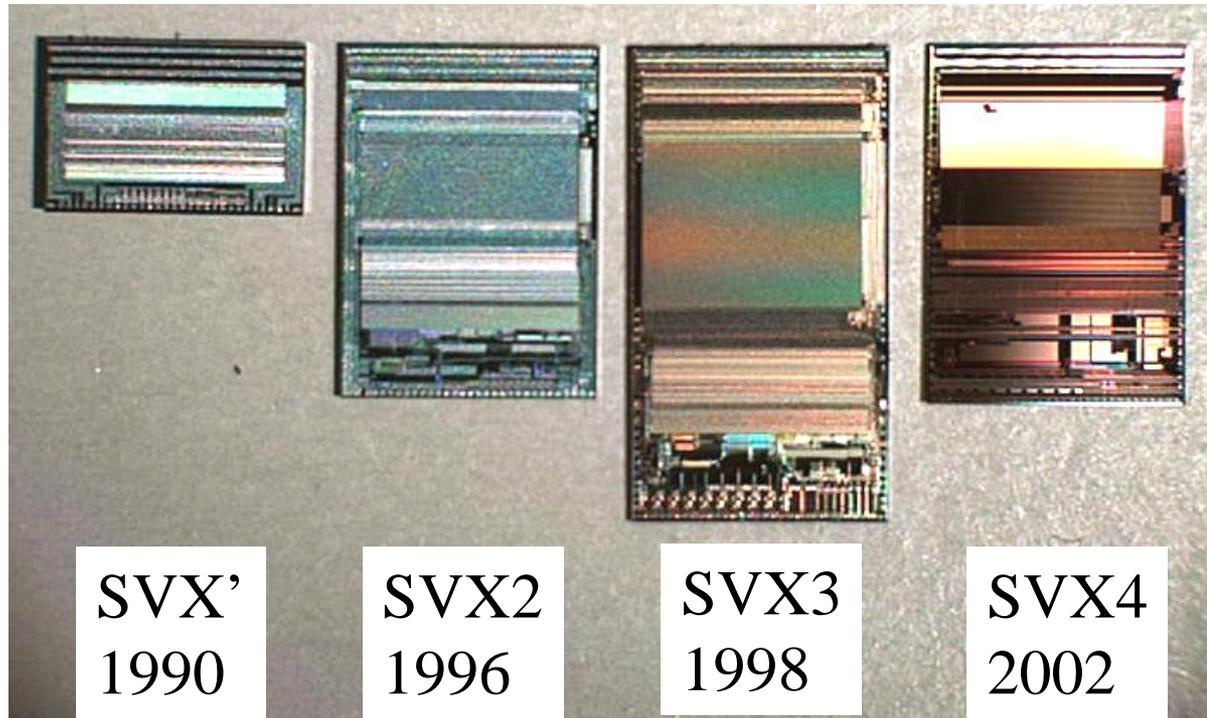


Status of SVX4

Kazu Hanagaki / Fermilab



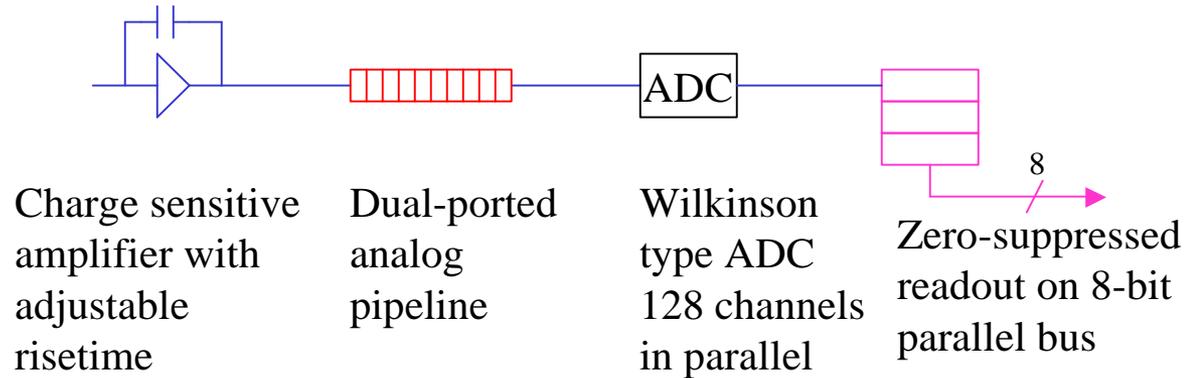
- For technical detail

<http://www-cdf.lbl.gov/users/mweber/svx4>

- Our test result

<http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/readout/svx4/svx4.html>

Introduction



- Functionality is the same as SVX2/3.
← one can choose D0 or CDF mode.

➤ D0 mode: blocking FE clock in digitize/readout → Less worry for the back end activity while sampling data.
➤ CDF mode: while digitize/readout, sampling data is possible. → Deadtime-less operation.

- Rad-hard by 0.25 μ m technology by TSMC.
← up to 15Mrad.
- Real time pedestal subtraction (RTPS) capability.
← reducing common mode noise.

Where we are?

- April 2002: Design submitted for fabrication
- June 10, 2002: Wafers delivered to FNAL
- June 12, 2002: First chip tested at LBNL, basic functionality verified.

Many tests done by lots of people

(? ? , ? ? ? ? , ? ? ? ? ? ,
? ? ? ? , ? ? ? , ? ? , ? ? ? ? ...)

- Most items meet the specification.
- Some problems.
 - D0 operation (i.e. needs FE clock for pipeline cell sampling).
 - Pedestal non-uniformity across the channels;
1) bow or slope, 2) channel to channel variation
 - Pedestal non-uniformity across the pipeline cells.

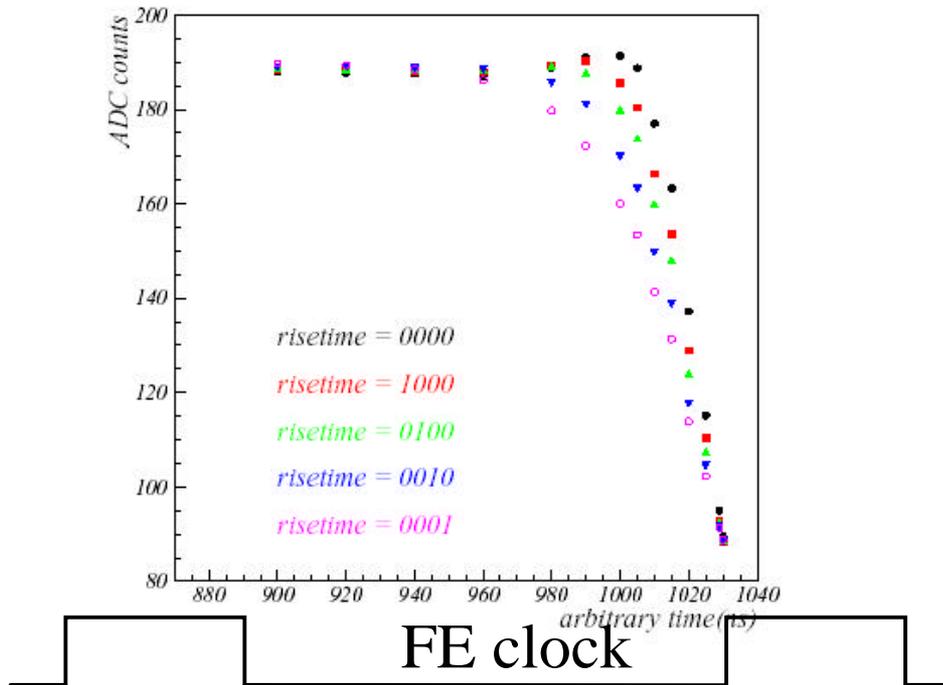
Outline of the rest of talk

- Brief review of tests results.
 - ← not cover all the tests. I just pick up some.
- Major problems.
 - Description
 - How to fix
- Proposals for the next submission.
- Conclusions.

Rise time measurement

- Timing scan of charge injection → looking at ADC.
- Purely front end measurement using preamp output buffer.

Rise time (ns)



BW	10pF	10pF	33pF
0	19.0	20	37.9
1	22.8		45.3
2	27.2		53.1
3		32	
4	35.1		65.4
7		46	
8	48.3		81.5

Design: $25\text{ns} + (\text{BW} \times 4\text{ns})$ for 10pF

Gain measurement

$$\text{Gain} \equiv \frac{\text{external injection charge (=assumed to be known)}}{\text{measured charge by ADC}}$$

#electrons / ADC count

BW	10pF	33pF	40pF
0	679	645	704
6	714		849
15	678	795	1043

Ramp slope
(001)

 MSB LSB

BW	10pF	33pF	56pF	82pF
0	877	923	940	1055
6	936	1009	1142	1450
15	1013	1217	1772	2051

Ramp slope
(100)

Noise

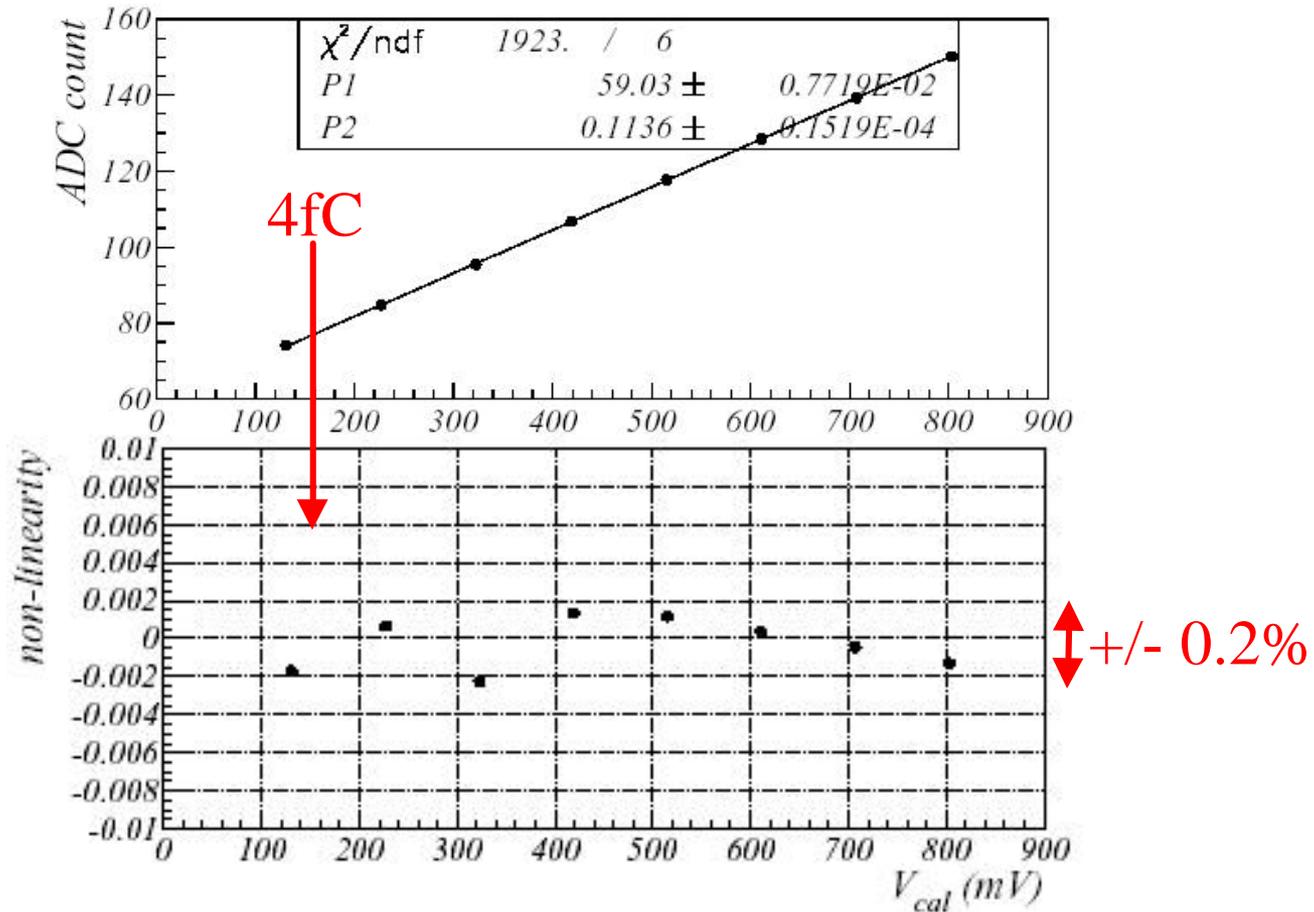
- For **fixed rise time (69ns)** by Tom Zimmerman:
 $ENC \cong 300 + 41C$ (2025e⁻ @40pF)
cf. this was $450 + 43.5C$ for the front end test chip.
- Spec. < 2000e for 40pF @ 100ns rise time.
→ very good noise performance.
- Noise can be measured as RMS of pedestal.
(noise = RMS × gain [#electrons/ADC])

BW=15	Ours	Tom's front end
10pF	993	794
20pF	1315	1034
30pF	1637	1434

← (~500 electrons) of additional setup noise?
(Note this is <0.5ADC counts)

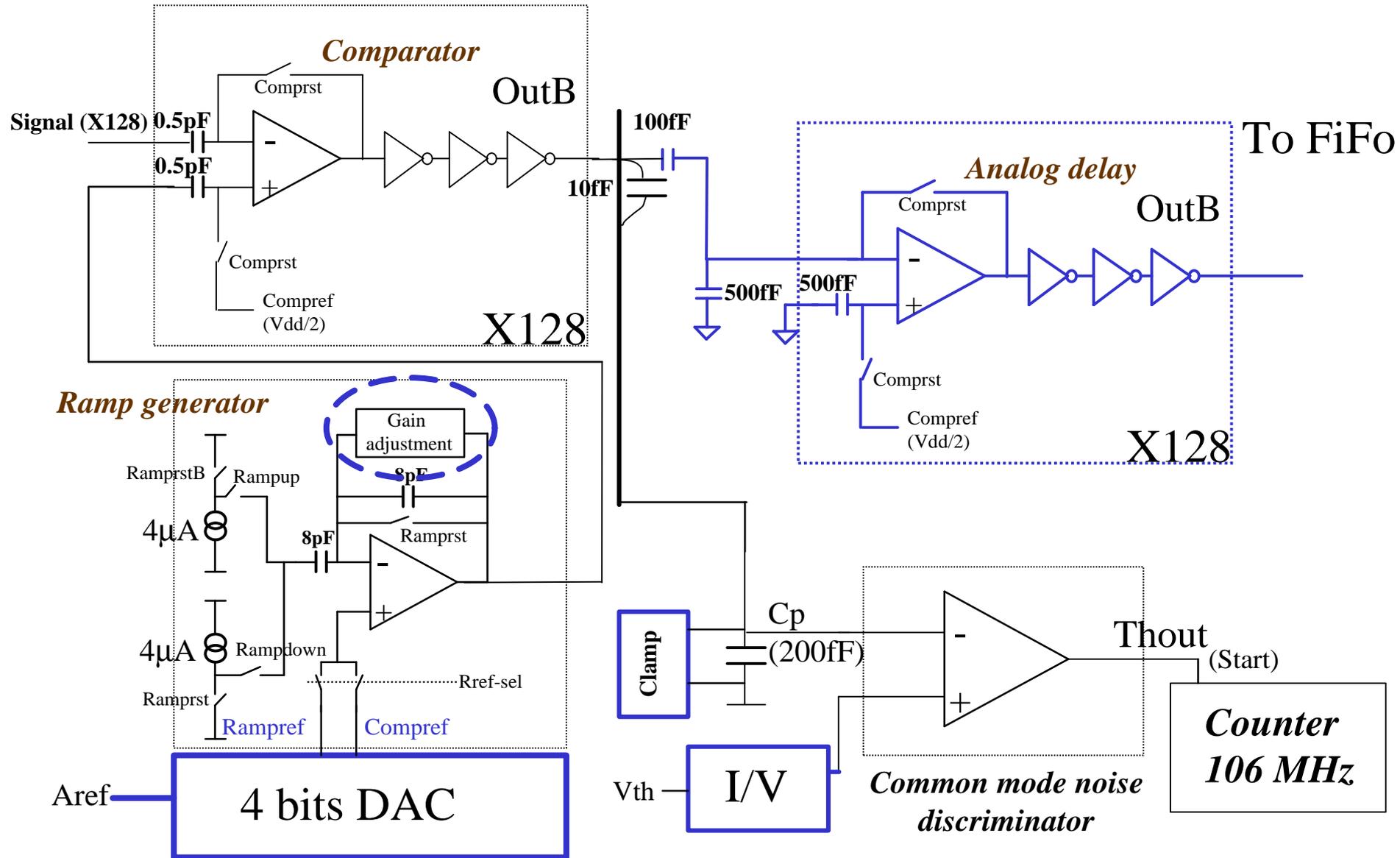
Non-linearity measured by cal_inject

- Non-linearity \equiv ADC(meas) – Expectation(by the fit)

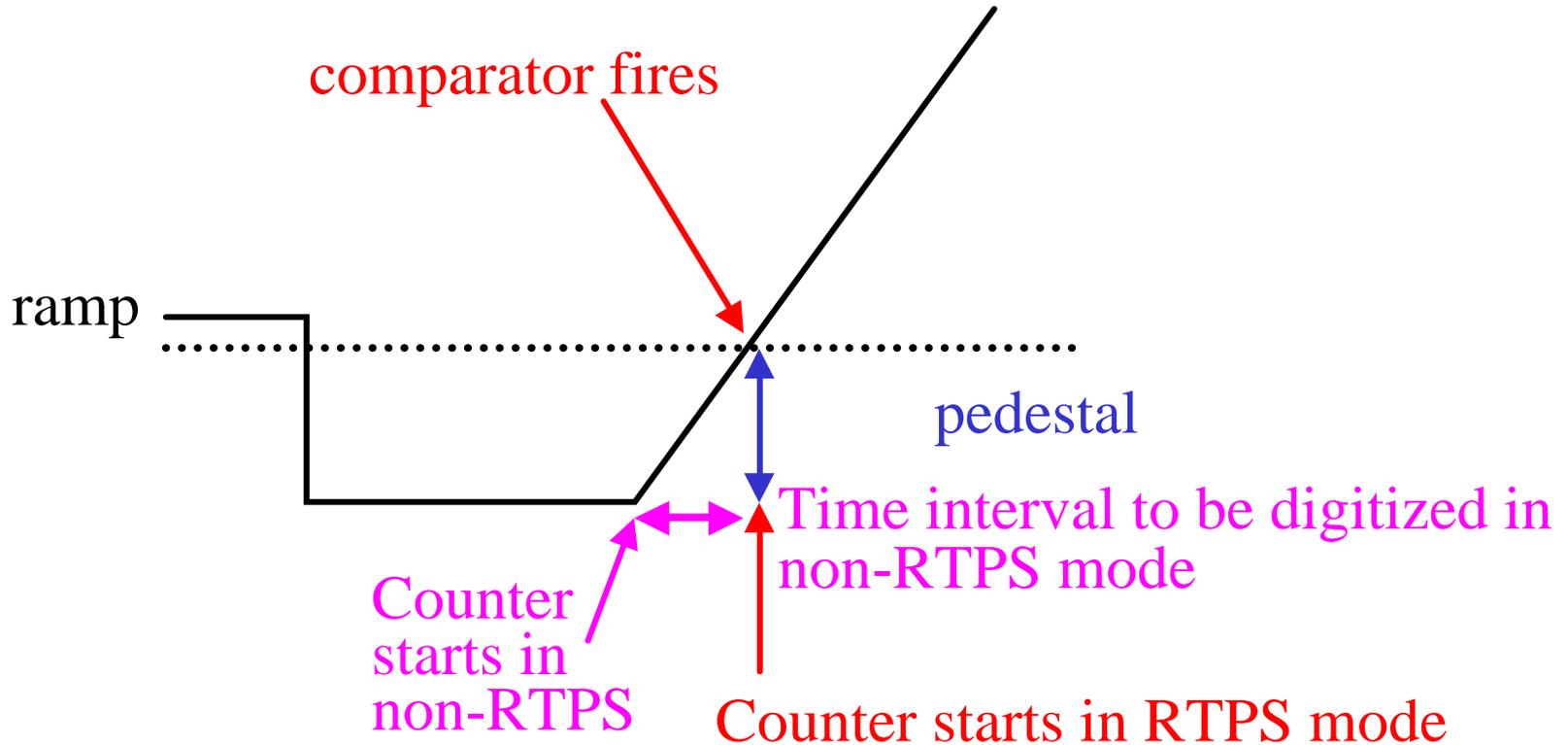


- Note!! This includes not only ADC but also the front-end.

Schematic of ADC



Real Time Pedestal Subtraction (RTPS)



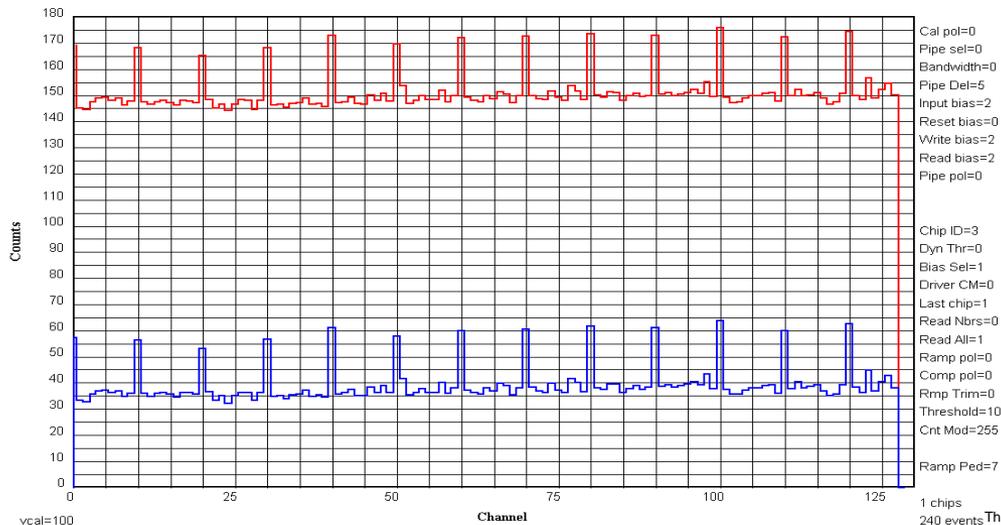
- Democratic vote from all 128 channels when to start the counter.

RTPS (cont'd)

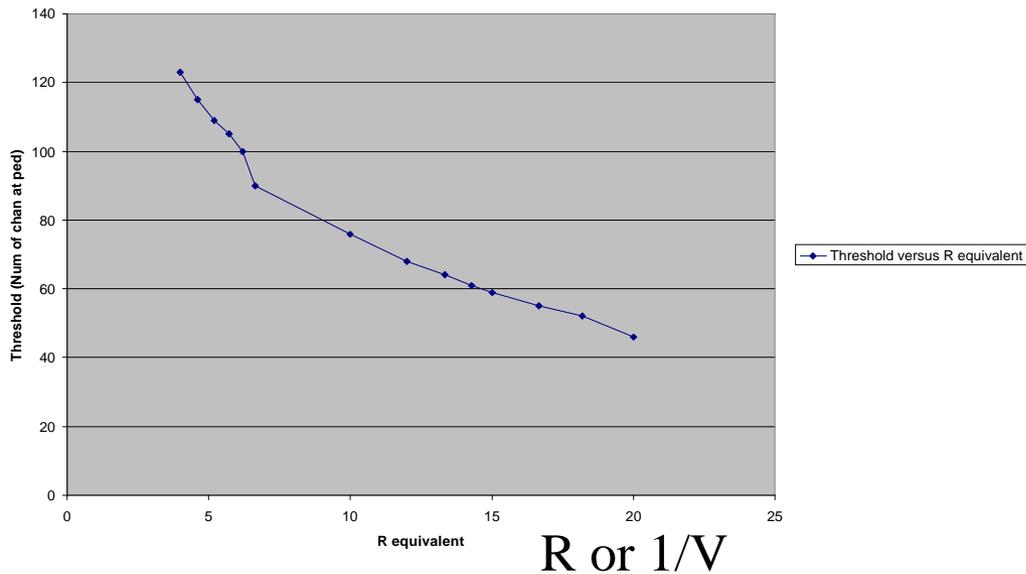
Run: 27333
Plot: 22409

Mean of data, ,

10-10-2002 7:43



Threshold or pedestal



R or 1/V

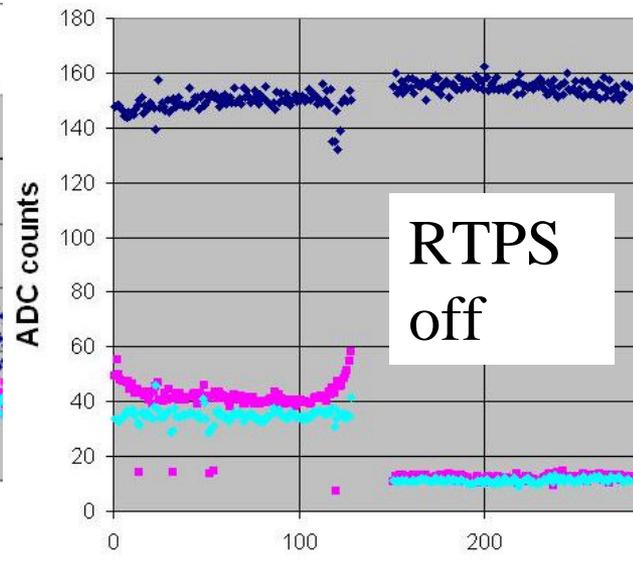
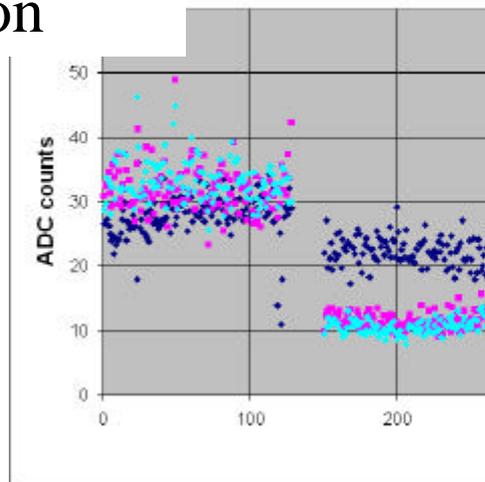
RTPS (cont'd-2)

Cal_inject – pedestal (ADC counts) for L0 prototype

#fire	8	16	32	64	64	80
off	66.0 ± 7.2	65.0 ± 7.2	68.8 ± 7.5	69.1 ± 6.9	73.5 ± 7.4	71.1 ± 6.5
On	65.8 ± 5.9	64.8 ± 6.1	67.8 ± 5.2	68.0 ± 5.2	72.1 ± 5.5	69.4 ± 5.4
occ. (%)	6.3	12.5	25	50	50	62.5

RTPS

on

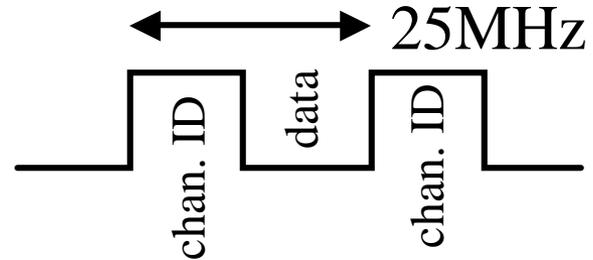


→ common mode noise is really reduced!

Frequency Scan for readout

- Len and Mike worked on the readout frequency scan.

For example,
BE clock = 50MHz

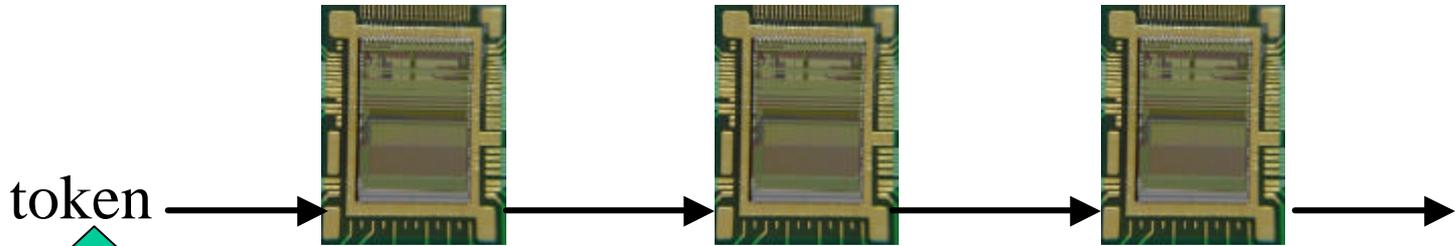


BE clock \ Duty cycle	40%	50%	60%
100MHz	Blue	Blue	Blue
72.4MHz	Blue	Green	Blue
50MHz	Blue	Green	Blue

Usual
operation
range

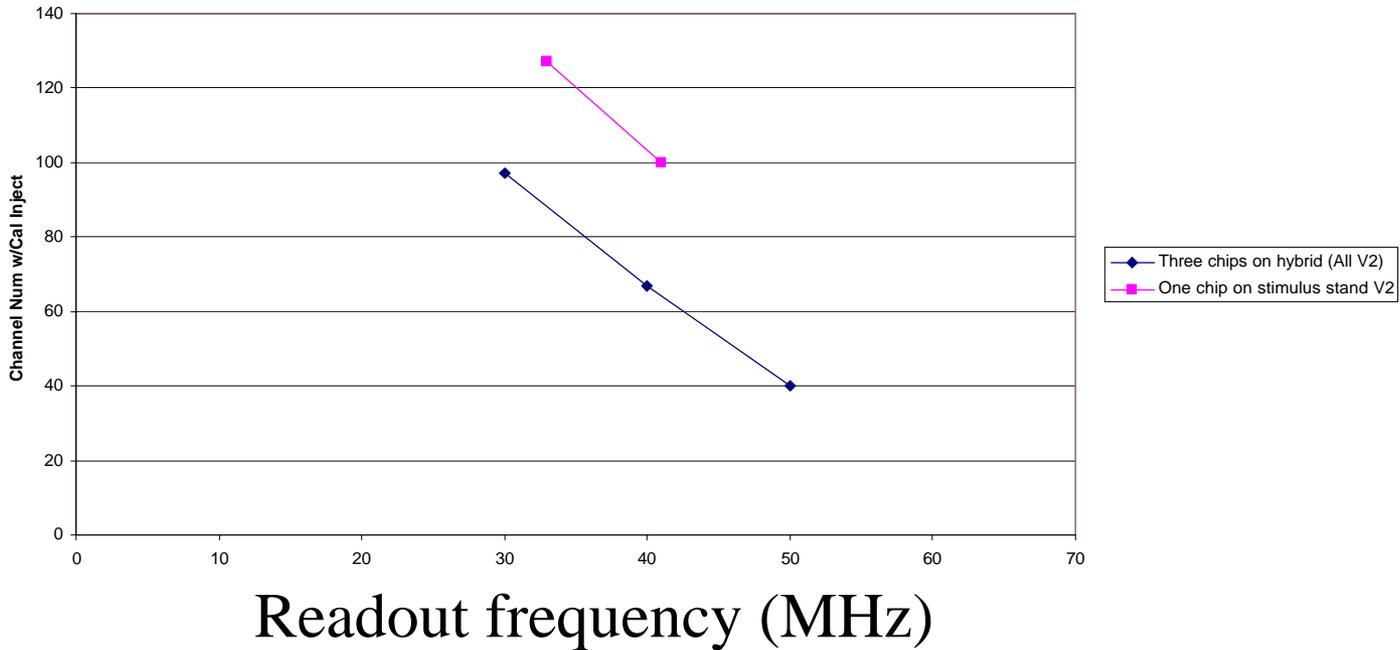
- ✓ confirmed by single chip operation.
- ✓ confirmed by hybrid (4chip).

Double readout



like a pointer which chip (channel) should be read out.

Readout may be finished before token passing through a chip
→ double readout happen (in sparse mode).



Data output driver

- Measured the voltage between bus and bus-bar (differential signal with 100Ω termination).

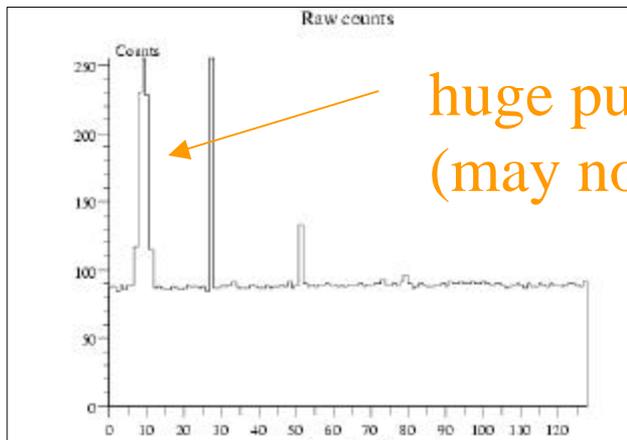
Output driver current

bit	Meas.	design
001	5.6mA	5.6mA
010	9.4mA	9.2mA
100	13.2mA	13.4mA

- Also measured the rise time and fall time to be $\sim 3\text{ns}$.

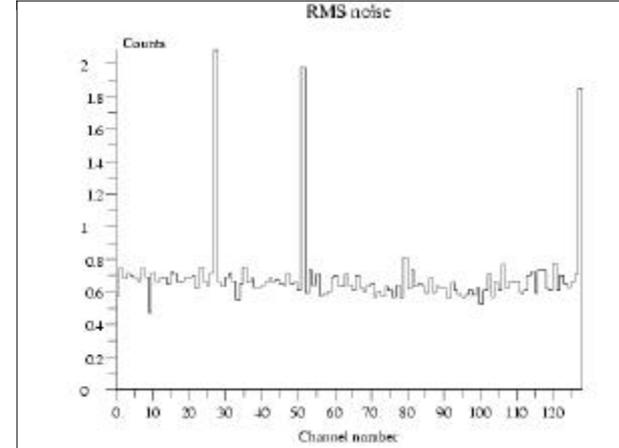
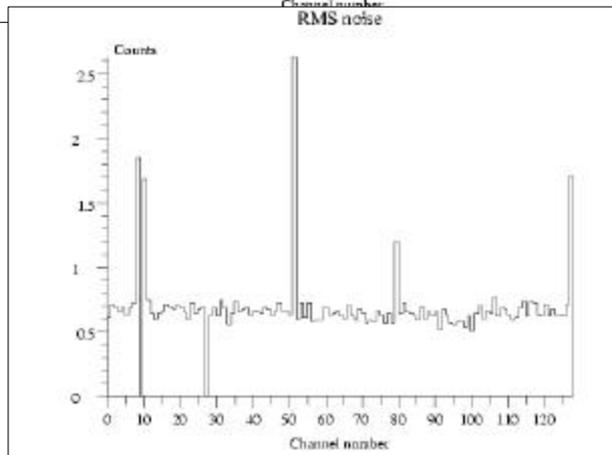
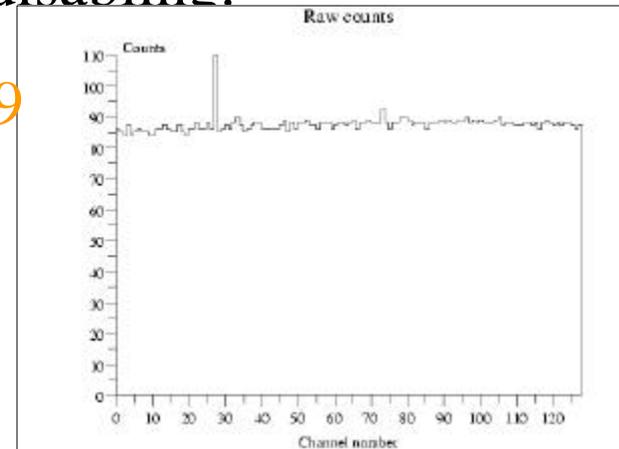
Channel disabling mask

- Functionality to disable individual channel (=preamp is kept resetting) to avoid black hole effect.
- The same bits with cal_inject mask, but another bit determines whether cal_inject or disabling.



huge pulse into ch. 9
(may not be B.H.)

ch.9
disabled



Yield

- 33 chips tested on the hybrid. 30 seems OK.
- 6/8 by individual chip test at stimulus machine.



- $36/41 = 88\%$.



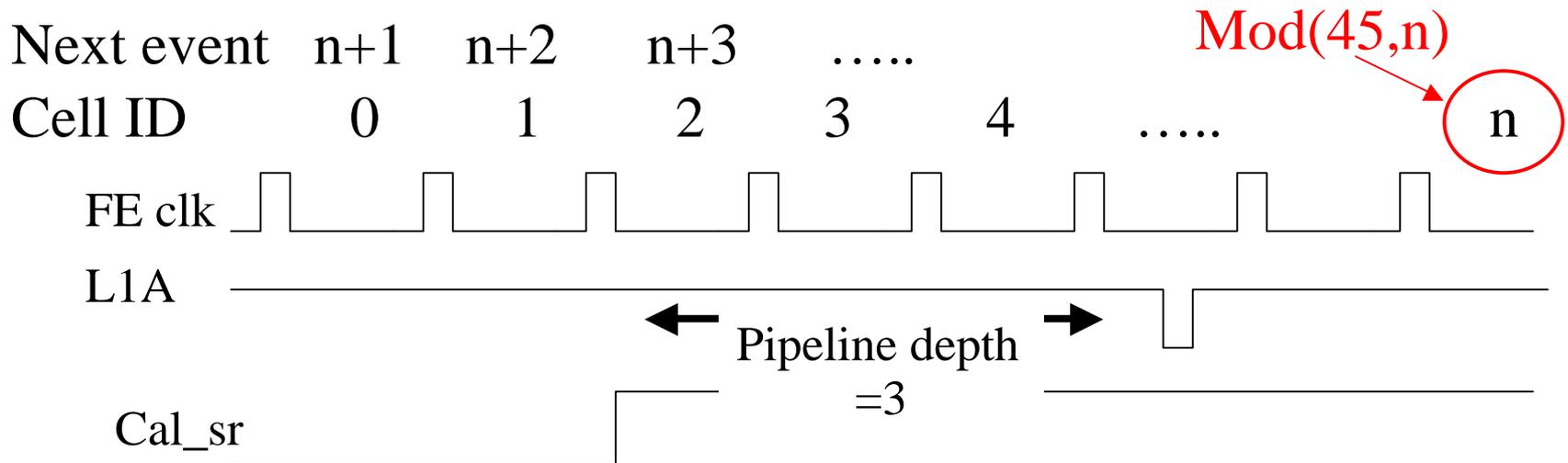
may be different criteria

All channels checked, but not sure for pipeline cells.

Pipeline cell and pipeline-depth (one of init parameter)

Pipeline Cell or Depth?

- Do not mix pipeline depth and actual pipeline cell.
- Only cal_strobe in initialize mode resets the cell back to the first one.



- Pipeline cell dependence has been checked. But did we check the pipeline depth dependence? (= test of data persistence)

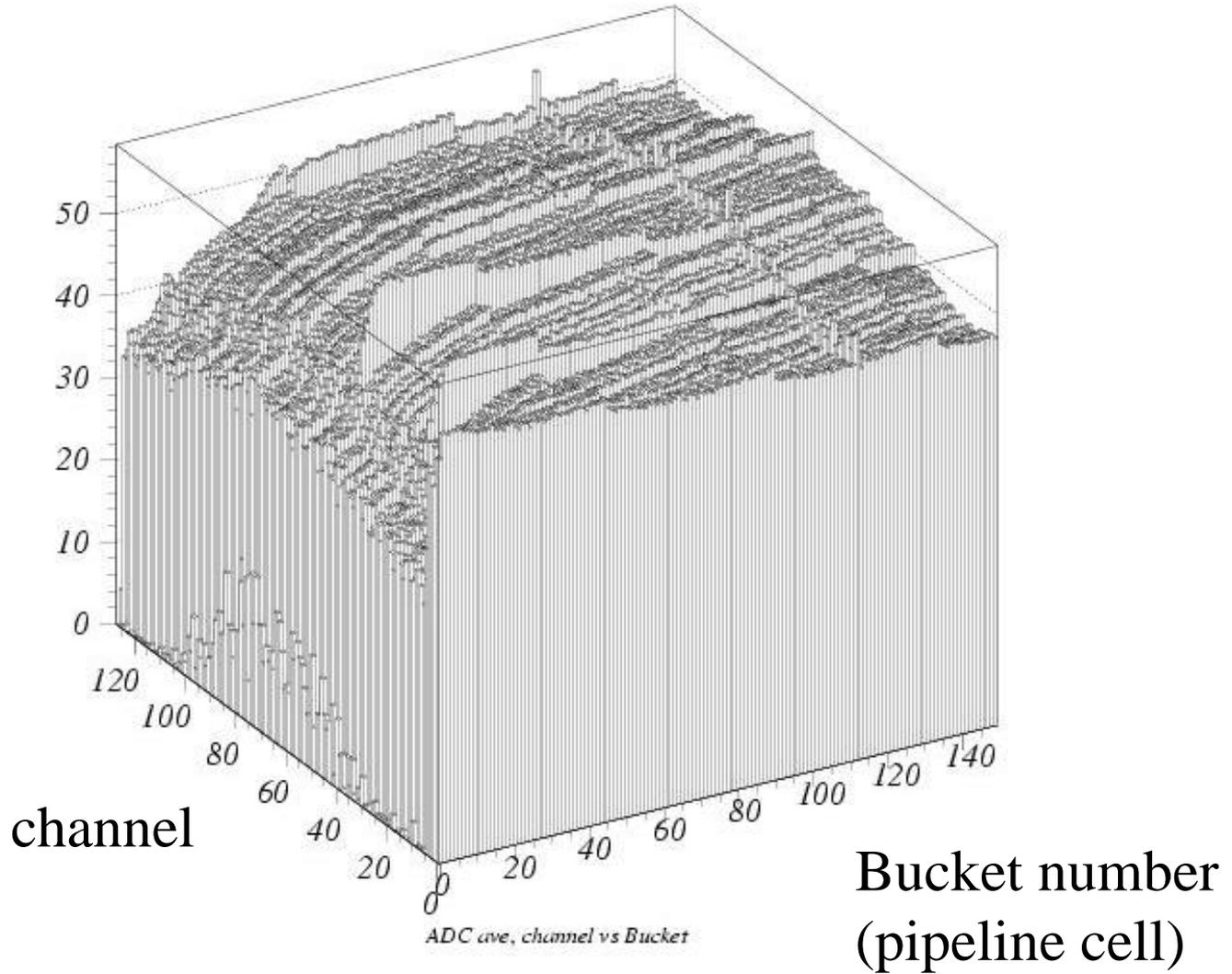
Irradiation tests

- SEU test by 63 MeV protons. Total fluences = $1.4E14$.
 - SEU cross section $2.2E-17$ to $1.6E-16$ cm^2 @95%CL
 - No major change in pedestal, noise, or gain up to $\sim 19\text{Mrad}$
- Co-60 irradiation for CDF hybrid 16-18Mrad.
 - No change of noise.
 - Small pedestal shift and small increase (!) of gain.
- D0 hybrid irradiation at KSU by 16 MeV protons.
 - Survived 25Mrad.
 - No significant change in noise performance.

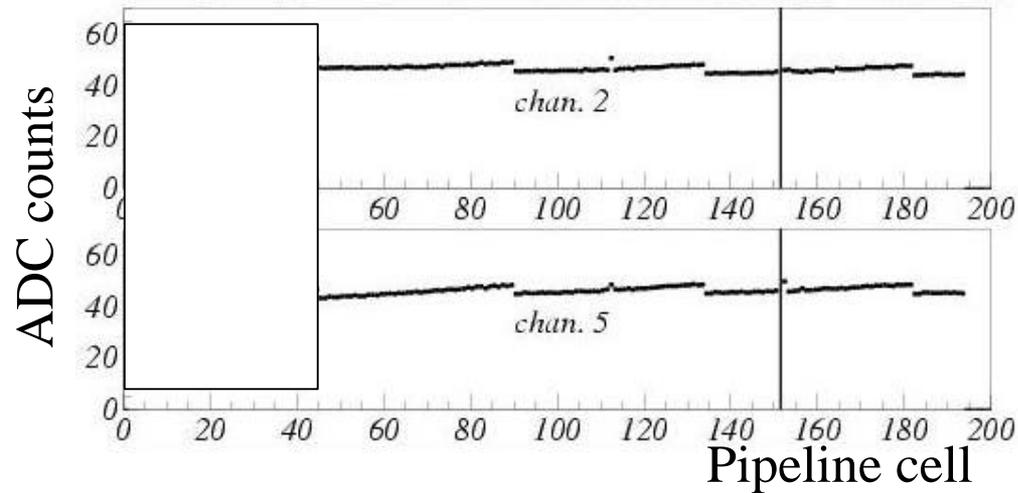
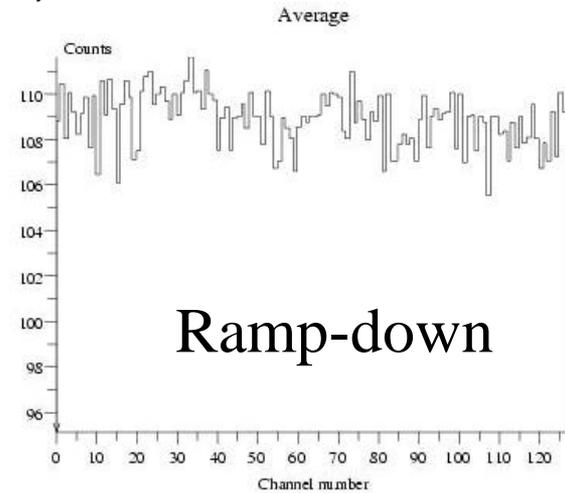
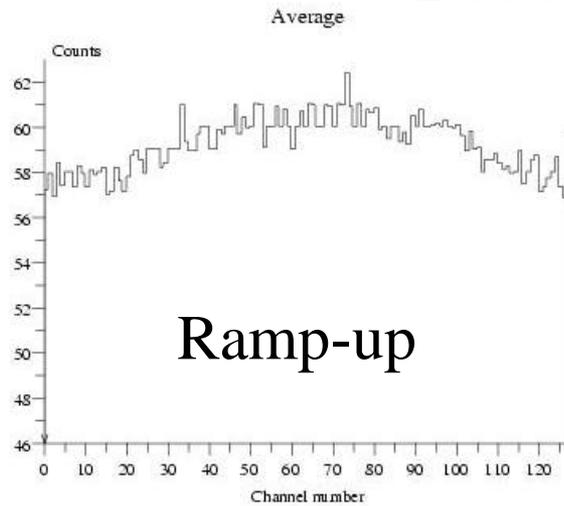
Major problems

- Pipeline cell sampling in digitize mode in default. FE clock is needed to latch it in conjunction with PRD1 (control signal). HOWEVER, D0 mode blocks out FE clock in digitize/readout mode. → does not work in normal procedure.
- Going back and force between acquire and digitize mode.
(acquire) → (starting ADC setup) → (Pipeline sampling) → (digitize)
- Pedestal non-uniformity across channel.
- Pedestal non-uniformity across pipeline cell.

Pedestal

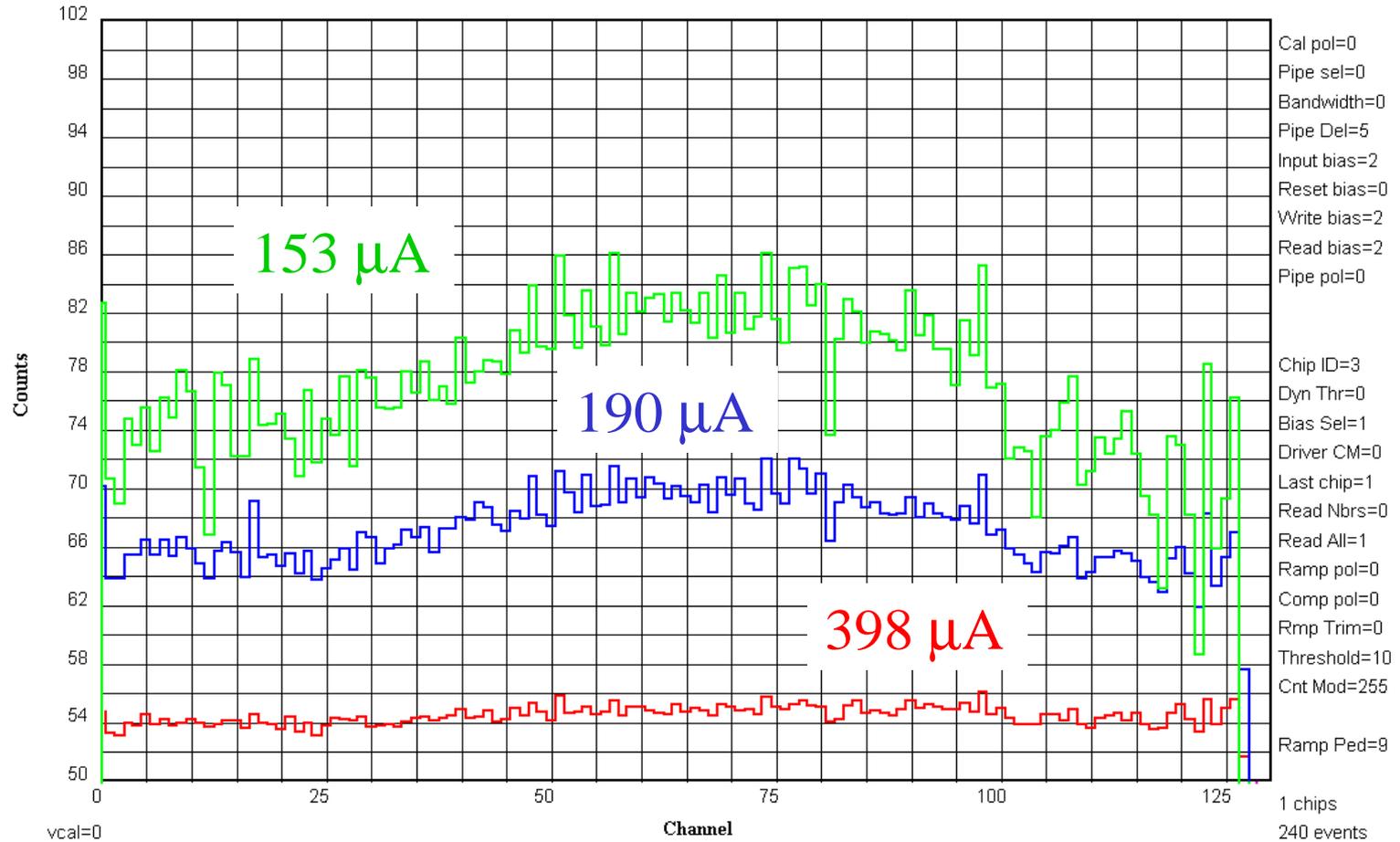


Pedestal (cont'd)

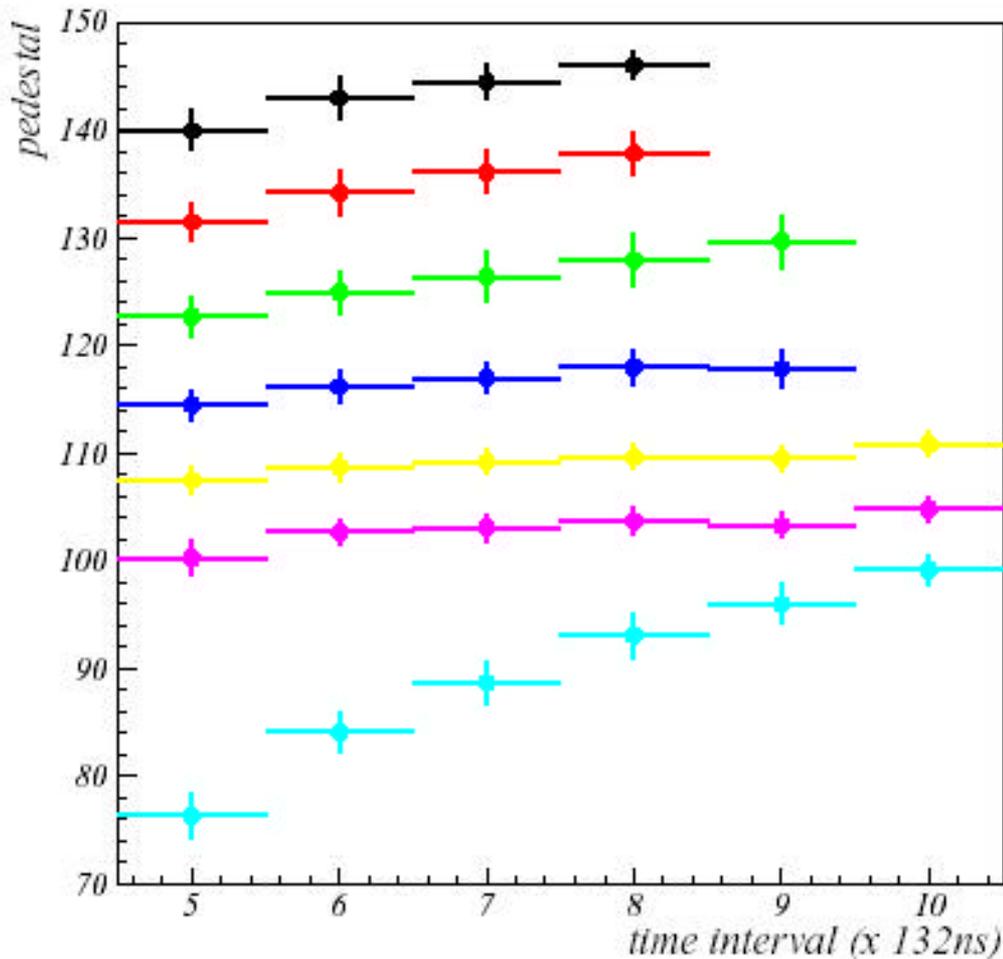


- Channel dependence (and channel to channel variation)
- Pipeline cell dependence

Pedestal Dependence on IQUI (comparator bias current)



Pedestal shift



Between comp_rst and ramp_rst

- The behavior is consistent with the expectation.
- **NOTE!!** What relevant here is the time interval between comp_rst and when comparator fires, i.e. longer is more stable.
- A setting with higher pedestal value has longer time interval internally.
← the dependence is less.

Proposal for Fixing

- For D0 operation issue:
Use readout-bar signal (= either initialize, acquire, or digitize) mode, to control ADC setup lines. This enables us to set up ADC in the end of acquire mode (and of course sampling of pipeline cell).
- For pipeline dependence of pedestal:
Widen front end metal lines. ← It is considered as the thin line causes resistance variation to each cell, and thus the cell dependence.
- For channel dependence of pedestal:
Redesign or modification of comparator (and analog delay).
← It is considered as too slow comparator response causes the channel dependence. (see next page)

Two versions for next submission (finally settled...)

- Version A (minimal changes): fraction 1
 - transistor sizes in comparator bias cell to speed up the comparator (x2)
 - NMOS guard ring in ADC modules
 - Version B (pre-production): fraction 5
 - Redesign comparator, keeping the architecture same as the existing one.
 - Redesign ramp, and ramp pedestal generator.
 - Widen front end metal.
- ↑
will be
submitted
|
-
- Version C (Greatest redesign by Tom Zimmerman)
 - Redesign comparator using different architecture.
 - Many more.

Common Fix List

All Versions:

- 1) add pulldown on D0Mode
- 2) add pullup on USESEU
- 3) pullup bit7 of chipid
- 4) pulldown bit 6&7 of cellid
- 5) hardwire PRIOUT driver strength bits all ON
- 6) change ADC control signal latching scheme from “digitize” to “not(readout)”
- 7) add 2 bits to SR in frontend
- 8) add VCAL switch, VCAL resistor to AVDD only
- 9) change “feclockgating” comprst/rstb driver to 2 parallel paths, with the same strength (E_Inv1*2) as present

Schedule

- Design work has to be finished in a week or two.
- Verification by simulation for a month.
- Next submission will be January 2003.
- Turn around will be two month???
→ next version in hand in March or April 2003 (?).

Conclusions

- Check list going through most of the specification.
 - ➔ The most are within the specification.
 - Low noise: $ENC=300+41C(\text{pF})$ at 69ns rise time
 - Rad-hard: no problems up to 15Mrad or more.
 - Real time pedestal subtraction capability
- Yield: 36/41 (=88%) ← Very preliminary.
- Three major problems, and other several minor problems.
 - ← next submission will address all these issues.
- We are about to next submission (=next January?).

1. Preamp		
Gain	3mV/fC	×
Gain Uniformity	5% or better	×
External load capacitance	10pF to 50pF	×
Risetime 0-90%	adjustable in 60-100ns for any allowed load	×
Risetime adjustment	4bits	×
Noise (ENC)	< 2000e for 40pF load	×
Linearity	Linear response for pulses up to 20fC.	×
	Non-linearity < 0.25mV at output.	×
Dynamic range	>20fC	×
Reset + setting time	< 1 μ s for any initial condition.	×
Calibration injection	40fF internal cap switched to input.	25 fF
2. Pipeline		
Voltage gain	3 to 5.	×
Gain uniformity	5% channel to channel.	×
Risetime 0-90%	10ns to 40ns.	×
Noise (ENC at preamp input)	< 500e	×
Linearity	Linear response up to 20fC at preamp input.	×
Dynamic range	>40fC at preamp input.	×
Reset time	< 20ns for any allowed initial condition.	×
Pedestal uniformity	< 500e at preamp input channel to channel.	×
	< 1000e at preamp input cell to cell.	failed

3. ADC

Ramp rate trim bits	3 bits	×
Ramp pedestal trim bits	4bits	×
Ramp Linearity	0.25% for rates between 0.1 and 1 V/ μ s	×
Counter	8 bit Gray code, 106MHz rate.	×
Differential non-linearity	< 0.5 LSB.	needs to check

4. Data output driver

Current source range	2.5mA to 17.5mA in 2.5mA step	×
Rise and fall times	>2ns and <4ns.	×
Bi-directional	All bus pads are I/O for D0.	×
Single ended use	No additional requirement.	×

5. TN/BN pins

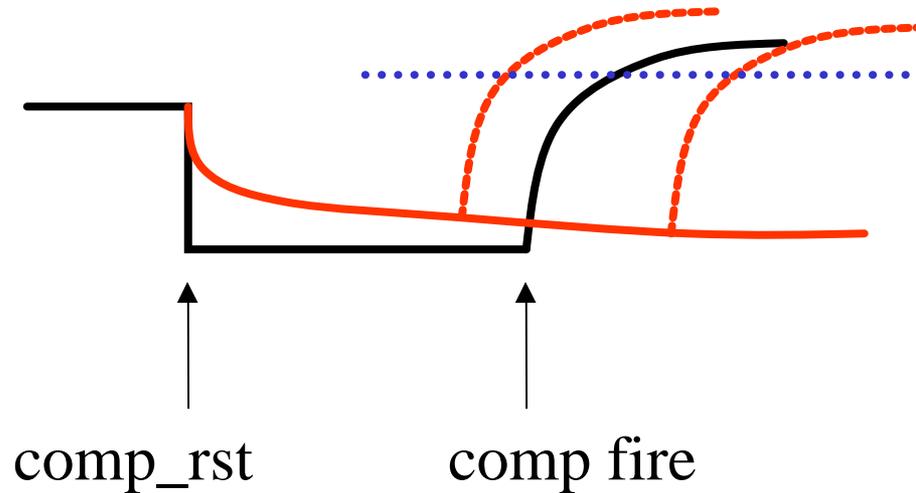
BN/TN modes	Only active in ditigize mode.	??
Priority in/out modes	Configuration registers input/output during initialize mode.	×
	Priority passing during readout mode.	×
	Priority out high during ditigize mode.	×

6. Control functions		
Ramp and Counter Reset	In normal mode Counter Reset is to be tied to Ramp Reset. In Dynamic Pedestal Subtraction mode Counter Reset is internally generated.	×
Preamplifier Reset & FE clock	Preamplifier Reset should always function independently of FE clock state.	×
PRD1		×
D0 mode pad		×

7. Configuration register	
Check if the following parameters affect the ADC counts for cal_inject, as expected.	
Cal_injection mask	×
Preamplifier bandwidth	×
Ramp rate	×
Preamplifier current	×
Pipeline write current	×
Pipeline read current	×
Pipeline depth	×
Driver current	×
Threshold for sparsification	×
Counter modulo	×
Chip ID	×
Dynamic pedestal subtraction	×
Read-neighbor	×
Read channel 63	×
Read channel 127	×
Pedestal adjustment	×
Reversed Polarity	×

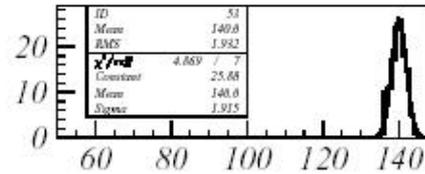
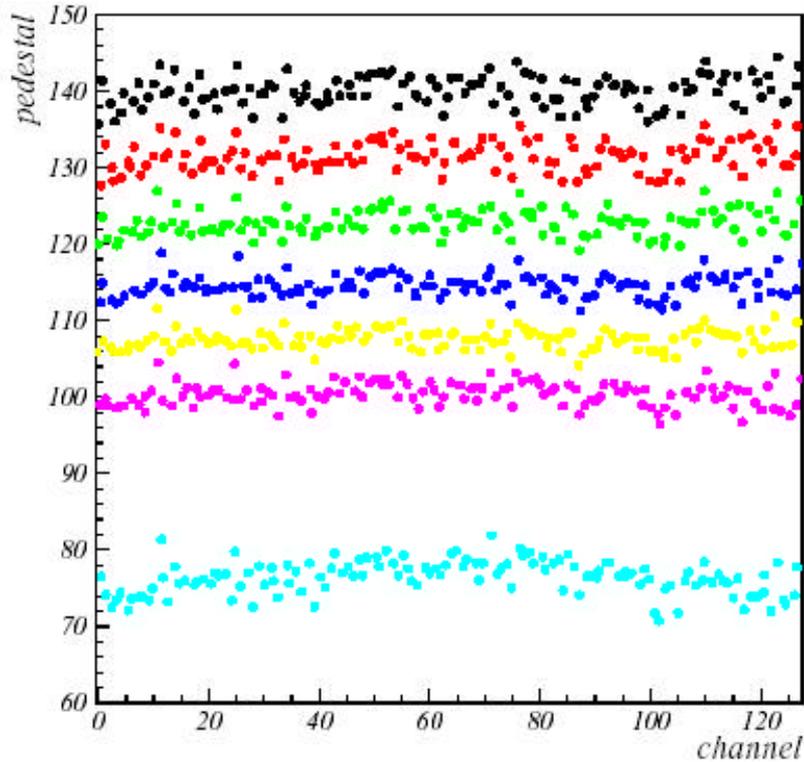
Comparator issue

Signal in the output buffer seems to need some time to be stable.

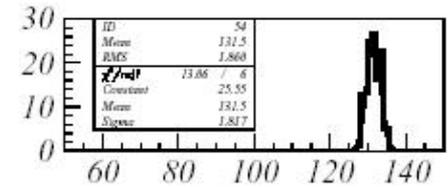


- Internal delay depends on the time interval between `comp_rst` and when the comparator fires.
- Pedestal should depend on this time interval.
- Expect pedestal increase for larger interval.

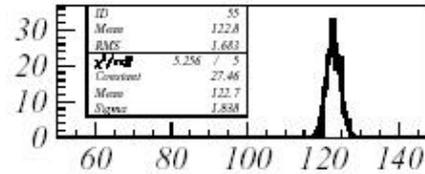
Observation



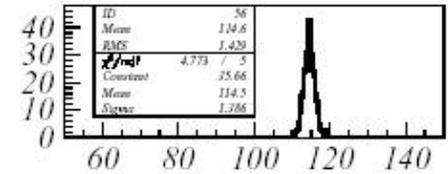
FE 5 Ped 3



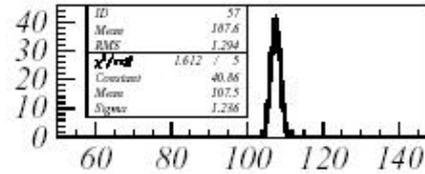
FE 5 Ped 4



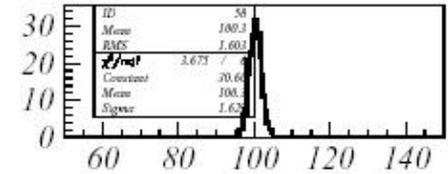
FE 5 Ped 5



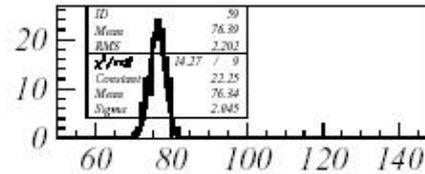
FE 5 Ped 6



FE 5 Ped 7

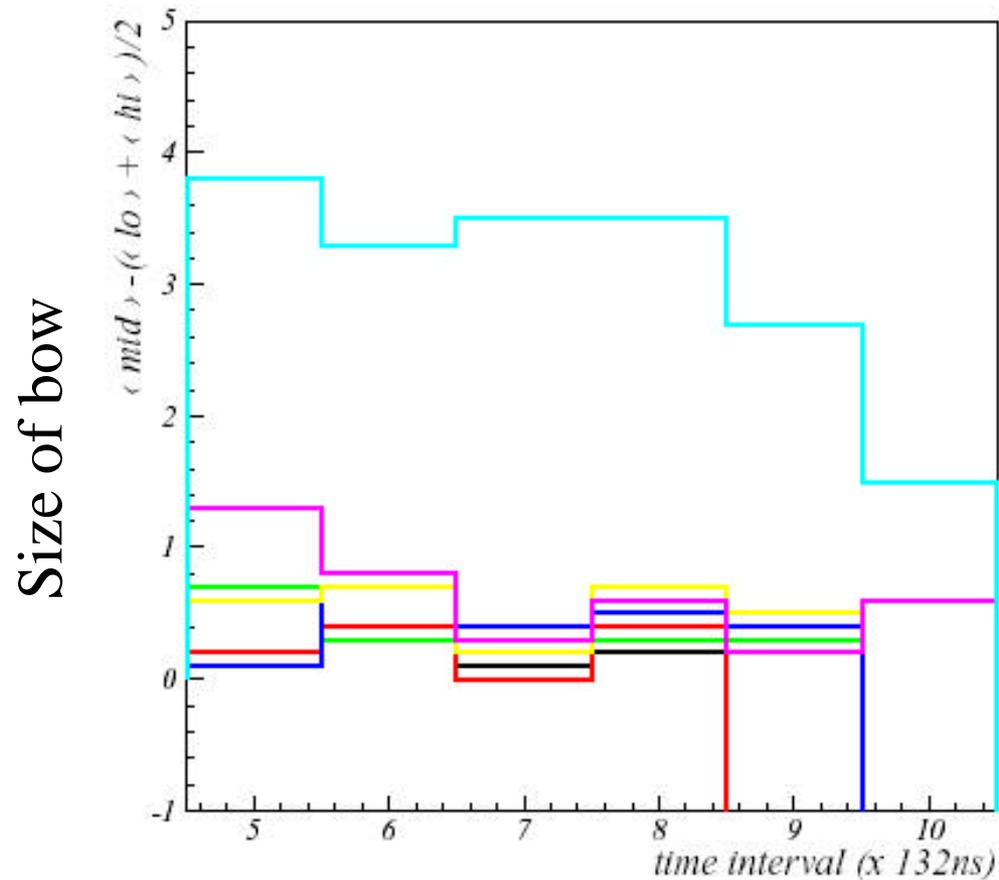


FE 5 Ped 8



FE 5 Ped 9

Size of bow



- The bow disappears after the long time interval. (= after the comparator reaches the saturation point, or stabilization.)