

Purple Card Notes – April 18, 2002

1. Current board size is 6" x 7.75". Mounting holes are provided in each corner.
2. HV bias is designed to be routed along top edge and bottom edge of the card. This provides for easier isolation from other circuitry and minimal interference with card ground plane. However, channel symmetry results in a larger jumper on channel B at the AVX connector.
3. Input power is on a 0.156" dual-row Molex mini-fit jr. connector. CAL_SR A and B come in on separate LEMO connectors. High voltage comes in on panel mount SHV connectors (a bracket for mounting these will be made). SASQ signals are on the 50 pin 3M connector.
4. Jumpers are available on the input side of the fuses to tie the "A" and "B" input power together if only one set of supplies is used or if current requirements do not justify doubling up on the wiring.
5. Regulator/Switch output side LED's have been removed from first draft. This is because of the limited space available on the front face of the board. The LED's on the comparator outputs have been retained to give indication when SVX power is on. Comparators only give a crude indication of the power level (threshold at 80%)

LED's available:

AVDD_A_IN	AVDD_B_IN
DVDD_A_IN	DVDD_B_IN
VCC_A	VCC_B
VA_A_IN	VA_B_IN
LVD_A_OK	LVD_B_OK
AVDD_A_OK	AVDD_B_OK
DVDD_A_OK	DVDD_B_OK
VA_A_OK	VA_B_OK
HDI_EN_A	HDI_EN_B
PWR_EN_A	PWR_EN_B

6. Currently six (6) layers are planned.

Layer 1 (top) – routing
Layer 2 – ground
Layer 3 – power and misc. routing
Layer 4 – power and misc. routing
Layer 5 – ground
Layer 6 (bottom) – routing

It will be difficult to properly impedance control the differential signals from the AVX connector to the transceiver due to the fanout of each component. However, because the AVX connector is so close to the transceiver, I doubt that it will be a problem. It may be best to focus instead on the single ended impedance from the transceiver to the SASQ instead.

7. Power dissipation of the regulators is a concern. If current reaches 1A limit, dissipation could reach 2.65 watts per regulator for $V_{in} = 4.6V$. Package is not optimal for use with a heat sink. Preference would be to enlarge the board and move the regulators to a clear area and use thermal vias to provide for heat-sinking to copper on both sides of the board. Efficacy of this is currently unknown.
8. Terminations resistor packages will be changing to smaller packages – SMSIP for pull-up/pull-down and SM for series termination. This will yield some of the board space required for the above.
9. Assertion of HDI_EN causes the PLD to turn on PWR_EN. PLD then waits TBD seconds for “OK” signals to stabilize before OE and DIR signals respond. If any of the “OK” signals go away, PWR_EN turns off and HDI_EN has to be cleared and reasserted to restart the board. If HDI_EN is cleared, PWR_EN is cleared. There is only one PWR_EN per channel (no sequencing of voltages to SVX).
10. Need values for fuses so we can get them ordered.
11. Need AVX connectors from KU