Summary of Purple Card changes and Modifications.

1. Jumpers J11, J12, and J13 are wired incorrectly. Will be corrected on Rev. 2 (Tim)

2. Add 100k pulldowns on the outputs of all solid-state relays. (Tim)

3. Fix reversed silk on R115 and C96. (Tim)

4. Rewire AVDD, DVDD, and LVD SSR's to correct adjust pin bias problem. Proposal is to use VA (switched by HDI_EN) to turn on regulators via the control input. This eliminates 6 SSR's and some other components. (Tim)

5. Correct power monitor reference voltages R1=R7=R21=8.87k, R13=R19=15.0k. (Tim)

6. Add 5.11k/10.0k voltage divider to VA input to power monitors to correct comparator common mode voltage problem. (Tim)

7. Change U17 and U13 from 74ABT04D to 74HCT14D (or 74HCT04D) to yield higher drive voltage to SSR's. (Tim)

8. Fix soldermask error on regulators. (Tim)

9. Fix clock polarity. Swap from /CLK to CLK on U3A and U6A. (Takes into account bypassing U10 and U12 -- see #13) (Tim)

10. Add 2K pullups/pulldowns on SVXOBDV and /SVXOBDV (input to U6B and U3B) to prevent oscillation in undriven state. Put 3K pullups and pulldowns on unused inputs to U6 and U3 (Tim and Evgeny)

> **(Utes: Although we did see oscillations, we found they also went away when I downloaded the first SVX with the "First Chip" bit, which tells that chip to drive the differential lines during other modes than Readout. Because of this I think we can confidently disregard any additional resistors from the purple card, and you can save the real estate.)**
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> **(Evgeny wrote back that /SVXOBDV of the LVDS drivers U6B and U3B must be connected to a positive potential and SVXOBDV input must be connected to ground via pullup and pulldown resistors so that the proper logic level is maintained on the output.)**
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> **(Message from Utes and Evgeny conflict. Current schematic eliminates pull-up and pull-downs on unused inputs and has SVXOBDV and /SVXOBDV pulled per Evgeny. Needs resolution)**

11. Remove RN2 and RN7. These are now 43 ohms series resistors and are to be completely removed from the design (understanding per Utes). (Tim)

12. Add an adjustable resistor in series with R58, R63, R38 and R43 to provide a 2.5+/-.3V adjustment range for AVDD and DVDD (range per Utes) (Evgeny)

13. Remove lump delay for dvalid (U4 and U7). Take the terminated input signals (CLK, PRI_IN, MODE1, CHMOD, and MODE0) directly to the LVDS chips (U8 and U5) with the same terminations, bypassing the ABT25245 (U10 and U12). U10 and U11 would them be used to drive PRI_OUT and DVALID to the SASQ, with DVAILD being daisy chained through multiple gates and a 0.1" jumper being provided to select the desired delay. (Evgeny)

14. Change resistors R121-R128 to 56 Ohm (now 90) (Evgeny)

15. Put op-amps to drive Vcal signals. Drive is 0 to +2.5V into a 4.5k pullup to 2.5V and a 1.5K pulldown to ground (times 10 chips)

16. Replace R137 and R138 (1 MOhm in HV ground line) with a jumper. (The capability of placing a resistor in this location will be preserved but it will be stuffed with 0 ohms during assembly. FNAL can decide later if the protection resistor is required for 1kV operation) (Andrei)

17. Change to a purple color solder mask if available (Andrei)

18. Design and build 90 degreee holders for purple card testing

19. Resistors R27-R30 and R129-R136 will never be used and can be removed (Evgeny)

20. RN4 and RN9 will never be used and can be removed (Evgeny).