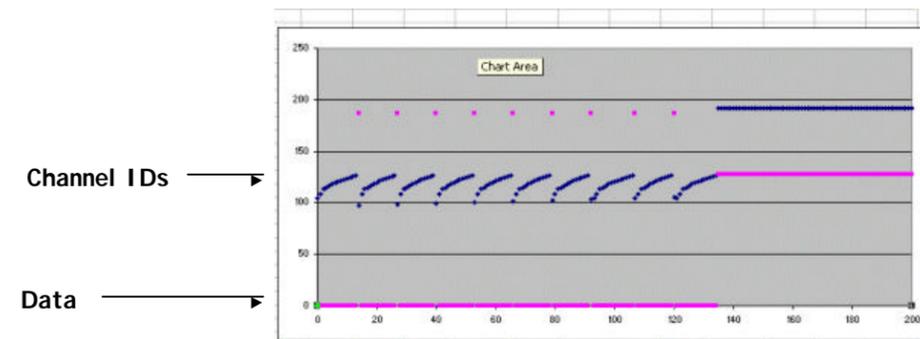




## SVX4 Incomplete Readout

### Symptom:

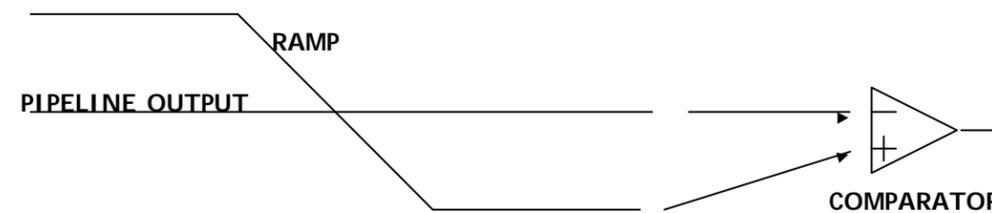
- Only Thirteen to fifteen channels read out in Read-All mode.
- Characteristic display:





## Conditions

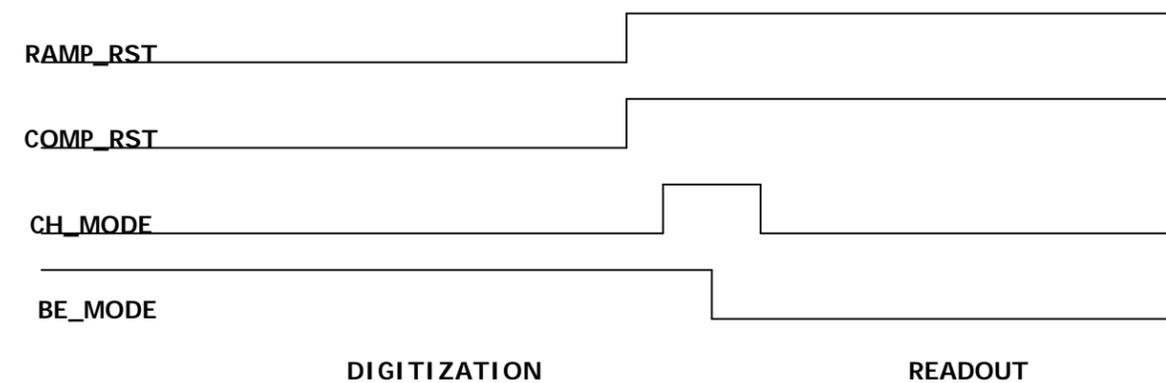
- Apparently happens when signals needed by the FIFO don't happen.
- To be read out, a channel has to either have its comparator fire or reach counter modulo. This status is latched at the exit of Digitize mode.





## Cause #1

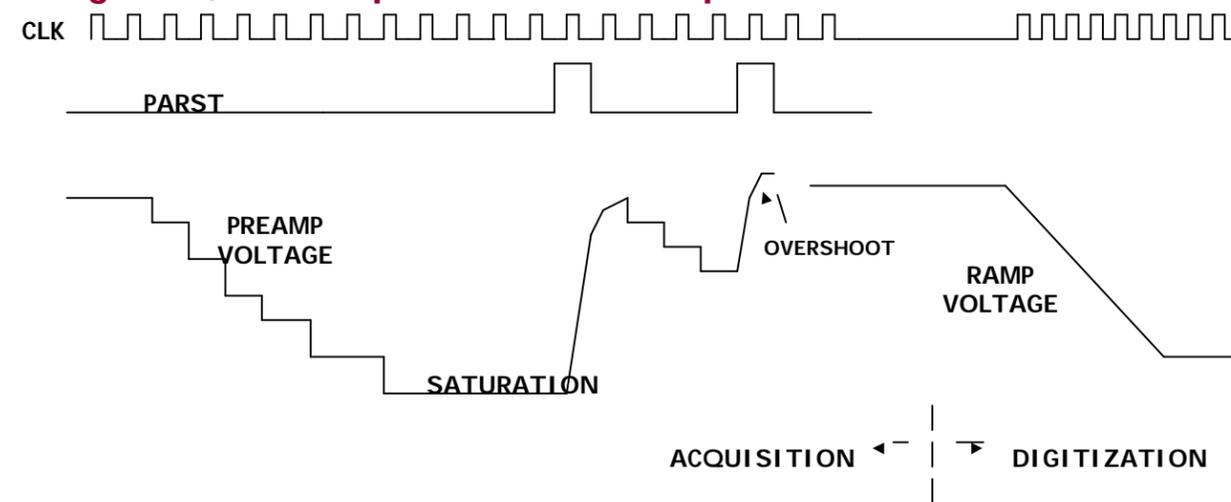
- Original timing diagram from LBL had Ramp\_Reset and Comp\_Reset rising before entering Readout Mode. This allowed many failures.





## Cause #2

- Rising edge of Preamp Reset during pipeline which will be digitized.
- We think that the voltage level of this Pipeline gets bumped above that of Ramp reference level, and ramp slope is negative, so comparator never flips.





## Good News

- Neither of these conditions will happen in the Tevatron