

## 5 READOUT ELECTRONICS

### 5.1 Overview

The readout system for the Run IIb silicon detector will be based on the new SVX4 chip and the existing Run IIa silicon data acquisition system. Sensors are connected to the outside world through hybrids with the SVX4 chips, and an external path consisting in turn of low mass jumper cables, junction cards, twisted-pair cables, adapter cards, and high mass cables followed by Interface Boards, Sequencers and VME Readout Buffers. A brief overview of the main ingredients of the readout system is presented in this section. Conservative solutions allowing for the fastest implementation of necessary changes were favored among different design options.

The SVX4 chip, designed as a joint DØ & CDF project, will be able to function in SVX2 mode and, therefore, will be compatible with the Run IIa readout electronics as discussed in detail in the next section. The chips will be mounted on hybrids. In the outer layers, the hybrids will be glued directly onto the silicon sensors. This allows for wire bonding directly from the chips to the sensors. The readout concept for staves in Layers 1 through 5 is shown in Figure 92. A “double-ended” hybrid design is chosen where chips are mounted on both ends of the hybrid and bonded to two different sensors. The hybrids are fabricated using thick-film technology on a beryllia ceramic substrate. All SVX4 chips on the hybrid are daisy chained for readout through one low mass digital Jumper Cable to the Junction Card. In Layers 2, 3, 4 and 5, the hybrid has 10 SVX4 chips and there are four readout cables per stave: two for axial sensors and two for stereo sensors. In Layer 1, 6-chip hybrids are used and there are three readout cables per phi segment.

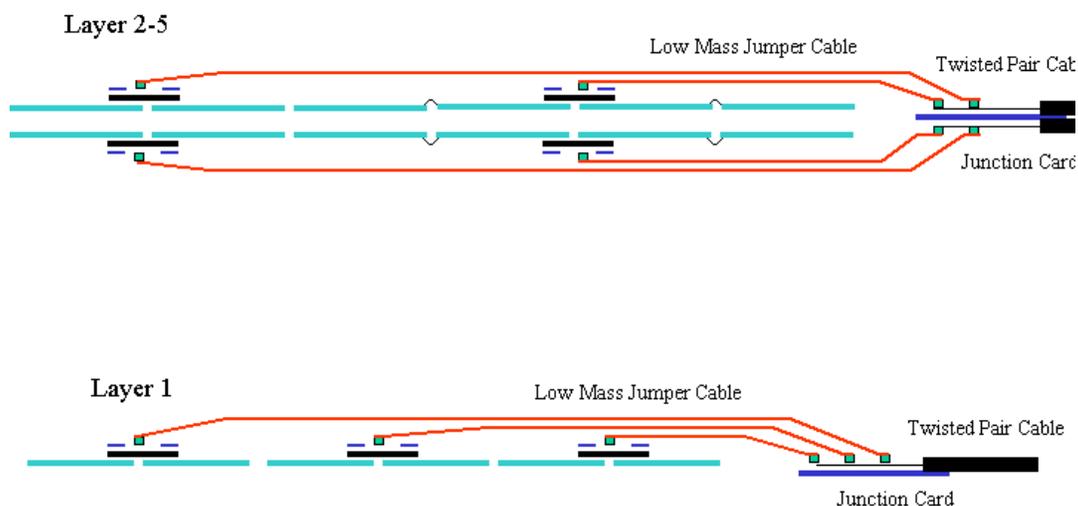


Figure 92 - Concept of readout for Layers 1 through 5

The innermost layer requires a substantially different design due to its very small radius and stringent requirements on the amount of material. For this layer, low mass analog readout cables

will couple the silicon and hybrids as shown in Figure 93. This allows the hybrids and silicon to be mounted independently, moving the mass and heat load of the hybrids out of the active detector volume. One 2-chip hybrid reads out one silicon sensor. To equalize the length of the analog cable between different sensors, the sensor closest to  $z=0$  is connected to the closest hybrid. Digital jumper cables connect the hybrids to Junction Cards. While the added capacitance from the flex cable degrades the signal-to-noise (S/N) ratio, we expect to achieve a  $S/N > 10$  for the SVX4 with analog cable readout even at the end of Run IIb as was explained in Section 3.2. Section 5.3 discusses issues related to the analog cables.

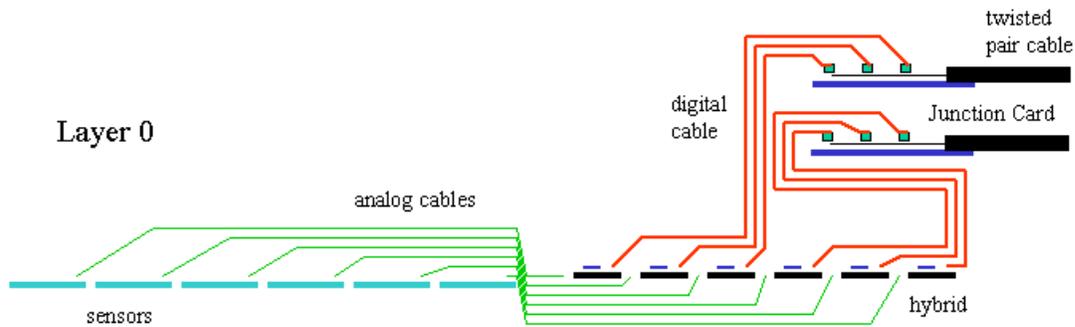


Figure 93 - Concept of readout for Layer 0

The total readout cable count is 888 with the cable count per layer given in Table 18. A detailed discussion of the hybrid and stave electrical properties is presented in Section 5.4.

Table 18 - Cable count per Layer

Layer	Chips per hybrid	# readout cables
0	2	144
1	6	72
2	10	96
3	10	144
4	10	192
5	10	240

A major consideration in the design has been to preserve as much of the existing Run IIa silicon data acquisition system as possible and to reuse the associated cable plant. Nevertheless, a few modifications are necessary to address two important issues:

1. The SVX4, produced in 0.25 micron technology will require lower operational voltage, 2.5 V as compared to 5 V necessary for SVX2. The allowed operational range of 2.25 – 2.75 V for SVX4 poses significant restrictions on the voltage drop in the power lines.

- Modification of control signals are needed to accommodate the difference between the SVX2 chip and the SVX4 chip operating in SVX2 mode.

Figure 94 shows a block diagram of the Run IIA silicon data acquisition. SVX2 chips are read out with approximately 2.5 meter long low mass cables to the passive Adapter Cards located on the face of the calorimeter (Horseshoe). Interface Boards are connected to the Adapter Cards with 6 meter long 80 conductor cables and serve as distributors of low voltages, bias voltages, data and control sequences for the detector. Interface Boards also monitor the temperatures and low voltages. Sequencers on the Platform provide clock and control signals for the SVX2 chips. The sequencers are also used to read out data from the chips and send them to the VME Readout Buffers via optical fibers. Only parts highlighted in gray will be modified for the Run IIB readout system. Adapter Cards and Low Mass Cables will be replaced with new components. Some firmware modifications in the sequencers will also be required as discussed in Section 5.11.

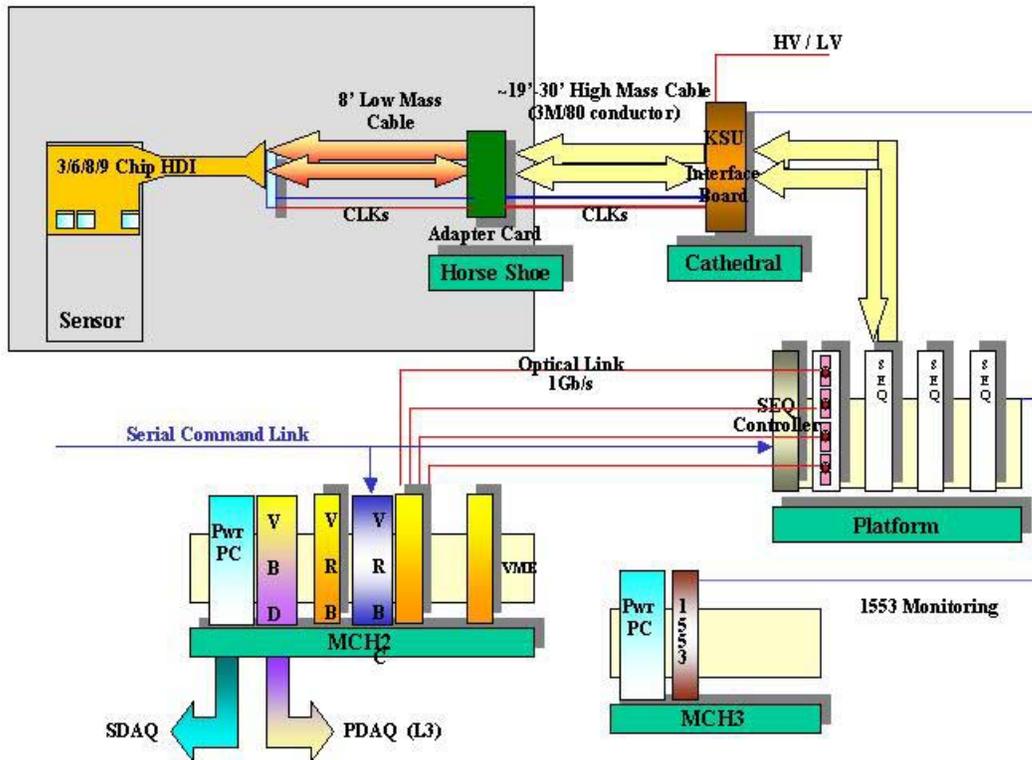


Figure 94 - Block diagram of the Run IIA silicon data acquisition system

Figure 95 shows the block diagram of the new components for the Run IIB data acquisition system. The Run IIA philosophy, having each hybrid connected to a single Interface Board channel, is preserved. However, the segmentation of this connection and the functionality of the intermediate pieces is different from that in Run IIA. A short low mass jumper cable starts from the hybrid and goes to the back of the detector where a passive junction card is located. The

junction card is connected to a new Adapter Card via a 2.4 meter long twisted pair cable. Data lines are driven differentially from SVX4 chips to the Adapter Card in contrast to the Run IIa approach which has single ended readout. Downstream of the Adapter Card, the lines are single ended.

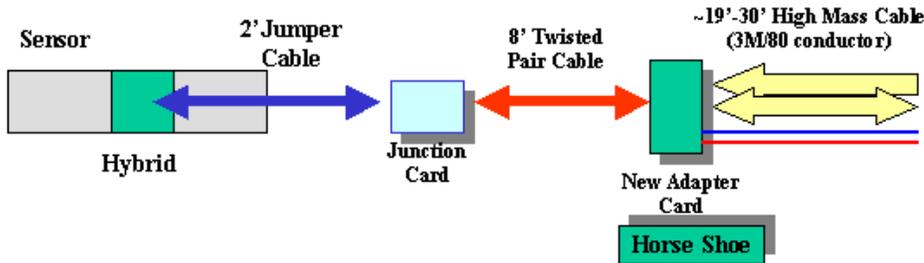


Figure 95 - Block diagram of the new components of the Run IIb data acquisition system

The Adapter Card is the key new component of the data acquisition accommodating most of the necessary modifications. It will perform the voltage regulation and will contain simple logic for the SVX4/SVX2 conversion as explained in Section 5.9. The Adapter Card is connected to the Interface Board with the existing 80-conductor cable. Some changes required for the Interface Boards are described in Section 5.10. Sections 5.6, 5.7, and 5.8 contain information about low mass Jumper Cables, Junction Cards and Twisted Pair Cables. Sections 5.12 and 5.13 have a discussion about low voltage and high voltage supplies and distribution. Results of simulations related to the readout performance are presented in Section 5.14. Grounding issues are discussed in Section 5.15.

## 5.2 SVX4 Readout Chip

The readout of the detector is accomplished by the use of the SVX4 readout chip, which is presently under development. The SVX4 is the last of a series of chips developed for silicon sensor readout by the FNAL-LBL collaboration. Earlier versions of such chips were the SVX-B and SVX-H (used in the readout of the first silicon vertex detectors of CDF), the SVX2 (used in the present DØ detector), and the SVX3 (used in the present CDF vertex detector). The SVX4 design thus draws heavily upon the experience gained from these earlier efforts and incorporates many of the desired features gleaned from this experience.

The SVX4 has 128 inputs with a 48  $\mu\text{m}$  pitch, which receive the charge generated by 128 strips of a silicon detector. The input charge, for a well-defined period of time corresponding to a single beam crossing, is integrated and deposited in a capacitor of a switch-capacitor array called the pipeline. This pipeline has 46 cells, in which 42 can be used to store the charge, thus allowing the successive storage of the charge generated during 42 successive beam crossings. If an event is accepted by the Level 1 trigger framework during any one of the 42 beam crossings, the charge of the appropriate capacitor is digitized by an on board ADC, and the resulting digitized data is sent to the data acquisition system. The data can be read in a read-all mode (i.e. in its totality), in a sparsification mode (i.e. only channels above a certain threshold value), or in a sparsification mode with neighbors (i.e. in addition to the channels above threshold the

channels flanking them are also read out). The chip also has a deadtimeless feature, which allows for the concurrent acquisition of charge by the integrators and the pipeline while digitization or readout is taking place; this feature, which is the salient difference between SVX2 and SVX4, will not be used by DØ. Another difference between SVX2 and SVX3 is that only SVX3 has the dynamic pedestal subtraction capability, in which the gray code counter in the ADC is forced to start when the number of channels with the comparator firing reaches a preset value. By adjusting the preset value to an appropriate number, it effectively removes the average pedestal over the channels, resulting in the increase of dynamic range and the compensation of possible pedestal drift in time. The SVX4 inherits this capability.

The SVX4 will be produced in a deep submicron process (0.25  $\mu\text{m}$ ) by TSMC (Taiwan Semiconductor Manufacturing Corporation). Such submicron processing leads to a very small oxide layer which in turn results in a highly radiation tolerant device, without having to resort to any special manufacturing processing. Chips developed in such process (such as the APV25 chip for the CMS experiment and the VA1 chip for the Belle experiment) have been subjected to radiation doses exceeding 20Mrad with no sign of radiation damage, and will survive the expected doses for all layers of our detector. These submicron process chips require a power supply of +2.5 V, which is different from the +5V and +3.5V of the existing SVX2.

Because the SVX4 chip is a copy of the SVX3 chip used in the present CDF detector, it incorporates features that were not used in the SVX2 and are not part of the control and readout configuration of the Run IIa silicon data acquisition system. These features have to do mostly with the deadtimeless operation mode of the SVX3, which requires additional control lines and a dual clock (front end and back end clocks). However, it turned out that remapping our control lines to the ones required for the SVX3, which channels our clock to either the front end or the back end clock depending on the mode of operation of the chip, was adequate to operate the SVX3. A test board consisting of a single FPGA and simple transceivers was able to perform the required task, i.e. an SVX3 chip was read by the DØ sequencer board, as seen in Figure 96.

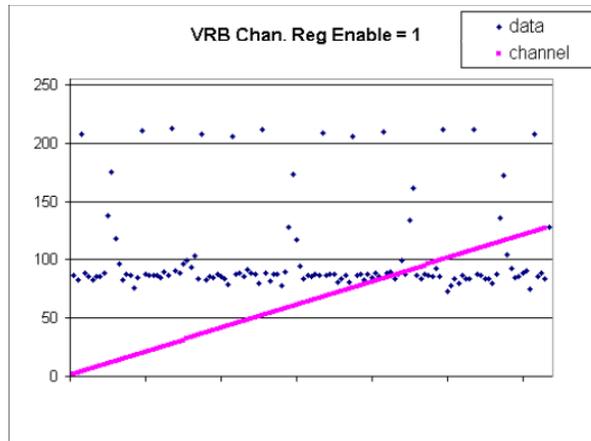


Figure 96. SVX3 chip performing in SVX2 mode with the DØ data acquisition system (November 2000)

As a result of this successful demonstration, DØ adopted the SVX4 chip designed by a FNAL-LBL-Padova team of engineers and has played an active and significant role in the design effort. The required remapping is shown in Table 19.

Table 19. Mapping between SVX2 and SVX4 readout/control lines

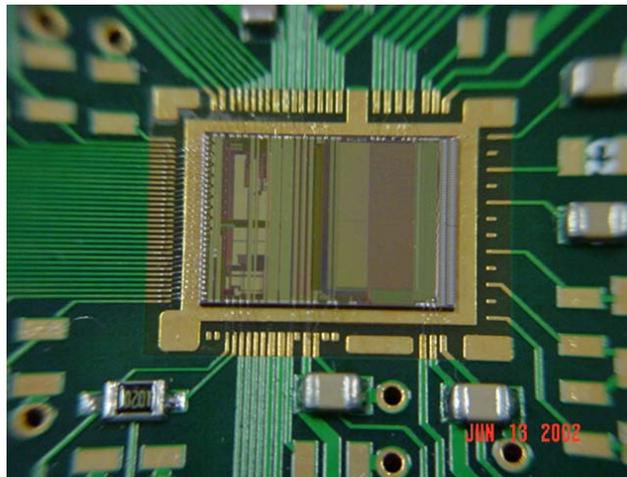
<b>SVX 2</b>				<b>SVX4</b>			
Mode				Mode			
INIT	ACQ	DIG	READ	INIT	ACQ	DIG	READ
BUS 0 PA RESET	BUS 0 PA RESET	BUS 0 PA RESET	Data 0	BUS4 PARST	BUS4 PARST	BUS4 PARST	Data4
BUS1 RREF-SEL	NC	HIGH	Data 1	BUS3 RREF-SEL	BUS3 RREF-SEL	BUS3 RREF-SEL	Data3
BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	Data2	BUS5 L1A	BUS5 L1A	BUS5 L1A	Data5
BUS 3 PIPE SREF	BUS 3 PIPE SREF	BUS 3 PIPE SREF	Data 3	BUS 6 PRD1	BUS 6 PRD1	BUS 6 PRD1	Data 6
BUS4 CNTR RESET	BUS4 CNTR RESET	BUS4 CNTR RESET	Data4	BUS2 PRD2	BUS2 PRD2	BUS2 PRD2	Data2
BUS5 RAMP RESET	BUS5 RAMP RESET	BUS5 RAMP RESET	Data5	BUS 1 RAMP RESET	BUS 1 RAMP RESET	BUS 1 RAMP RESET	Data1
BUS6 COMP RESET	BUS6 COMP RESET	BUS6 COMP RESET	Data6	BUS0 COMP RESET	BUS0 COMP RESET	BUS0 COMP RESET	Data0
BUS7 SR LOAD	BUS7 CAL INJECT	BUS7 N/C	Data7	BUS 7 CAL/SR	BUS 7 CAL/SR	BUS 7	Data7
MODE0	MODE0	MODE0	MODE0	FEMOD	FEMOD	FEMOD	FEMOD
MODE1	MODE1	MODE1	MODE1	BEMOD	BEMOD	BEMOD	BEMOD
CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE
TN	TN	TN	TN	TN	TN	TN	TN
BN	BN	BN	BN	BN	BN	BN	BN
CLK	CLK	CLK	CLK	FECLK	FECLK	BECLK	BECLK
CLKB	CLKB	CLKB	CLKB	FECLKBAR	FECLKBAR	BECLKBAR	BECLKBAR
DATA VALID	DATA VALID	DATA VALID	DATA VALID	OBDV	OBDV	OBDV	OBDV
PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN
PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT

This modification of control configuration can be accommodated by the existing DØ Sequencer readout module. In addition, the use of internal circuitry of the SVX4 allows the chip to operate in the so-called DØ mode. The circuitry can be turned on via an external wire bond to the digital voltage line. For operation in the CDF mode the wire bond must be connected to ground. In the DØ mode, using internal gating, the clock is sent to the appropriate section (front/back end) depending on the chip's internal mode. The same selector also forces the chip to use the PRD1, PRD2, L1A, and CALSR as inputs from the bi-directional differential data bus (for DØ) rather than their single ended dedicated input pads (for CDF). Thus, to use the existing DØ readout

sequencers the only major change required is a new adapter card with transceivers that will adapt the single-ended 5V signals used by the sequencer to differential 2.5V signals used by the SVX4.

In order to test and characterize the prototype chip in various aspects, we used three different test setups. The first setup at LBL is based on a pattern generator controlled by a Linux computer. In simplest terms this setup consists of two FIFOs, a clock oscillator, and an interface board to the computer. It is simple, flexible, well suited for quick extensive tests requiring frequent changes of download parameters and control sequences. However, the LBL setup does not allow clock frequency above 35MHz while the operational frequency is 53 MHz. The second setup is located at Fermilab, consisting of a sophisticated pattern generator with fine adjustment of timing (stimulus machine) controlled by a computer. Because of the capabilities of the stimulus machine, this setup has an advantage in detailed timing, frequency, and duty cycle studies. Most importantly this setup is capable of running at up to 100MHz clock frequency. The two setups above, therefore, are very much complementary. Detailed description of the stimulus setup and tests performed with the setup is available in Section 5.2.1. The third setup used for testing of SVX4 behavior on hybrids is based on the Standalone Sequencer and Purple Card. This setup is described in detail in Section 6.

During the SVX4 production the chips will also be tested on wafers before dicing. The corresponding setup is being prepared at Fermilab by the R.Yarema's group.



*Figure 97. The photograph of the prototype SVX4 chip mounted on chip carrier board.*

The first prototype chips were fabricated, and delivered to Fermilab and LBL in June 2002. Figure 97 shows the first prototype mounted on a chip carrier board in the LBL test setup. Since then, extensive tests have been performed using the three setups described above, as well as independent measurements of the front-end preamplifier. The most important conclusion is that the tests confirm the full functionality of the chips in both CDF and DØ modes. In the following, we list the highlights of some initial test results.

A preamplifier design with excellent frequency response, good reset time, good power supply noise rejection, and good noise performance has been identified. The overall noise of the analog section, i.e. preamp and pipeline combined, has been measured as  $[300+41 \times C(\text{pF})]e^-$  with 100 ns

integration time and 70 ns preamp rise time, where the C is the input load capacitance. The preamp and pipeline gains have been found to be consistent with the specification. Non-linearity including both the analog and digital parts has been measured to be  $<0.3\%$ . For the ramping voltage in the ADC, the offset level and the ramping rate are in good agreement with the expectation by the design. It is confirmed that the data output driver reproduces the input from the daisy chain, and passes the copied signal to the next chip. There are two configuration registers; a serial shift register and a Single Event Upset (SEU) tolerant shadow register. By changing the parameters stored in these registers, all bits have been checked to work as configured. The power consumption has been verified to agree with expectations. The different readout options, such as the sparsification mode, the dynamic pedestal subtraction, and ReadNeighbor feature have been tested.

An important issue to study was the frequency and duty cycle behavior. In the actual detector with a large number of channels, the duty cycle of the clock may be different from the ideal 50% form because of the long transmission lines of various lengths. This requires safety margins for the duty cycle and frequency of the clock. Studies are in progress to characterize the chip performance as function of frequency and duty cycle.

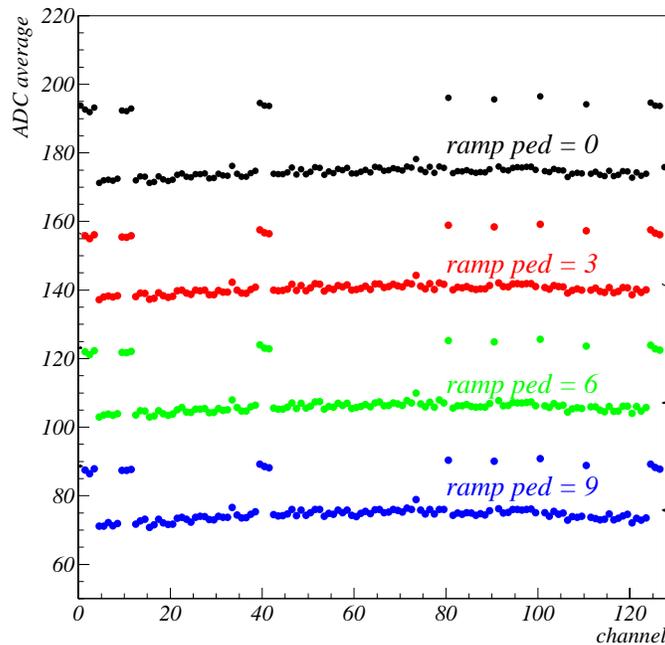


Figure 98. Average of ADC counts for 100 events across the channels. The calibration charge is injected to the channels with higher ADC counts. The offset of ramping voltage in the ADC has changed, and thus the digitized ADC counts for the calibration charge (= difference between the changed injected channels and the others) is constant.

Figure 98 and Figure 99 show the ADC counts for all 128 channels with some configuration parameter settings. The calibration charge is injected to the channels with higher ADC counts. It is verified that variation of the configuration parameters correctly affects the output ADC counts, as seen in the two figures.

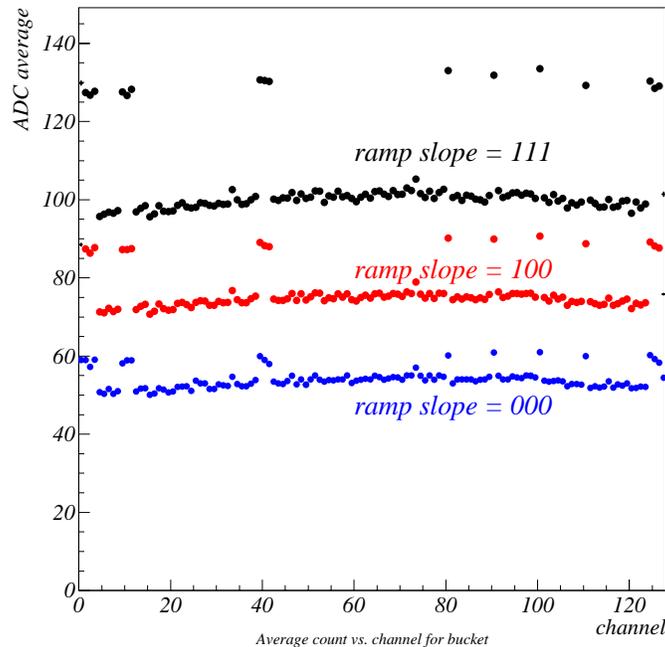


Figure 99. Average of ADC counts for 100 events across the channels. The calibration charge is injected to the channels with higher ADC counts. The ramping rate in the ADC is varied. This gives the change in both the digitized ADC counts and pedestals.

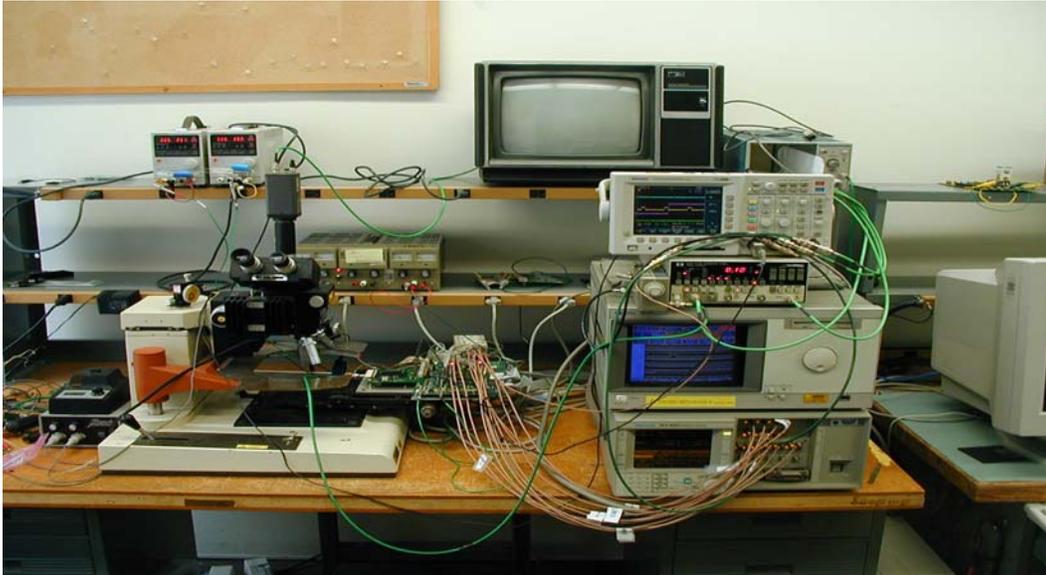
An irradiation test for the analog front end part had been conducted for the test chip, which consisted of only preamp and the pipeline, using a  $^{60}\text{Co}$  gamma ray source. While the test result did not show any significant performance degradation, the prototype SVX4 chip should also be irradiated. We are planning two separate studies. The first one is irradiation by hadron beam for testing the shift register and the Single Event Upset (SEU) tolerant shadow register. To check if there are any corrupted bits in the shift register during exposure, the chip will be kept running and shift register values will be read out continuously. The shadow register also has to be examined at the same time. The second test will check sensitivity to total doses. This test will use a  $^{60}\text{Co}$  gamma source. These two tests will be performed in September 2002.

As shown above, no fatal failures or bugs of chip operation have been found so far. However, some minor bugs were revealed. These include modification of ADC control sequence to facilitate switching between Acquire and Digitize in DØ mode, modifications of two bit assignments in the data field, and layout modifications in ADC for better pedestal uniformity across the channels. The fix list is being created, and the revision of the design is in progress now. The target date of pre-production submission for the next prototype is mid-November 2002.

### 5.2.1 SVX4 tests with Stimulus Setup

The stimulus test stand was originally designed for testing the SVX2 silicon readout ASIC and then upgraded for SVX3 prototyping and testing. We have modified this system for SVX4 testing.

The stimulus test stand consists of a PC with a GPIB interface card, a DAC-812 and a PCL-710 digital counter both connected through an ISA port. A custom DAQ program (SVXEval) was written for Windows 9x. The program algorithmically constructs patterns in memory and transmits them via GPIB to a Tektronix HFS 9003 Stimulus System. The PC also programs a HP 16500B Logic Analysis System over GPIB. The PC is a 200 MHz Pentium with 64 MB of RAM and is running Windows 98. We show the entire system in Figure 100.



*Figure 100. The Stimulus Test Stand. The PC is located to the far right. The Stimulus System is located next to the PC below the Logic Analysis System, HP Pulse Generator, and Tektronix TDS 3034 Oscilloscope (in order from bottom to top). Cables connect the Stimulus System outputs to the SVX4 Adaptor Board located in the middle which is connected to a SVX4 chip carrier. The Adaptor Board and Chip Carrier are mounted on a movable table of the Rucker & Kolls Probe Station that has a Bausch & Lomb MicroZoom microscope connected to the television. The power supplies for the Adaptor Board and SVX4 chip can be seen as well as the power supply to two Picoprobes that are used to probe pads located on top of the SVX4 chip itself.*

The Stimulus System sends patterns to the SVX4 through a custom designed interface board and has a maximum speed of 630 MHz. The frequency for normal operation is 530 MHz which allows an ability to change the waveform at the level of 2 ns. The Stimulus System has a total pattern memory of 64 K vectors which allows a pattern length of 128  $\mu$ s. In practice, the pattern memory is divided into different cycles of SVX4 operation and these individual patterns can be repeated indefinitely.

The HP 16500B Logic Analysis System contains a 4 GHz/1 GHz Logic Analyzer along with a 2GS 32K Oscilloscope. The Logic Analysis System has two HP pods with flying-lead probe tips that are used to monitor the signals being sent to the SVX4 chip via the SVX4 adaptor board and the data output from the SVX4 chip. Each pod has 8 data lines which gives us the ability to monitor 16 different signals in the system. One probe is used to monitor control signals and the other is used to view the data from the SVX4 chip. We are able to graphically view the waveform being downloaded to the chip and the data coming from the chip.

The SVX4 Adaptor Board, designed by the University of Kansas, has multiple functions. Because the Stimulus System cannot generate enough control signals, an EPLD located on the Adaptor Board is used to generate the extra control signals necessary for proper SVX4 chip operation. The Adaptor Board properly terminates the signal and bus lines of the SVX4 chip, contains test points which give convenient connection points for the flying-lead probe tips of the Logic Analysis System, and allows for dual mode (DØ/CDF) operation of the SVX4 chip. We show the SVX4 Adaptor Board in Figure 101.

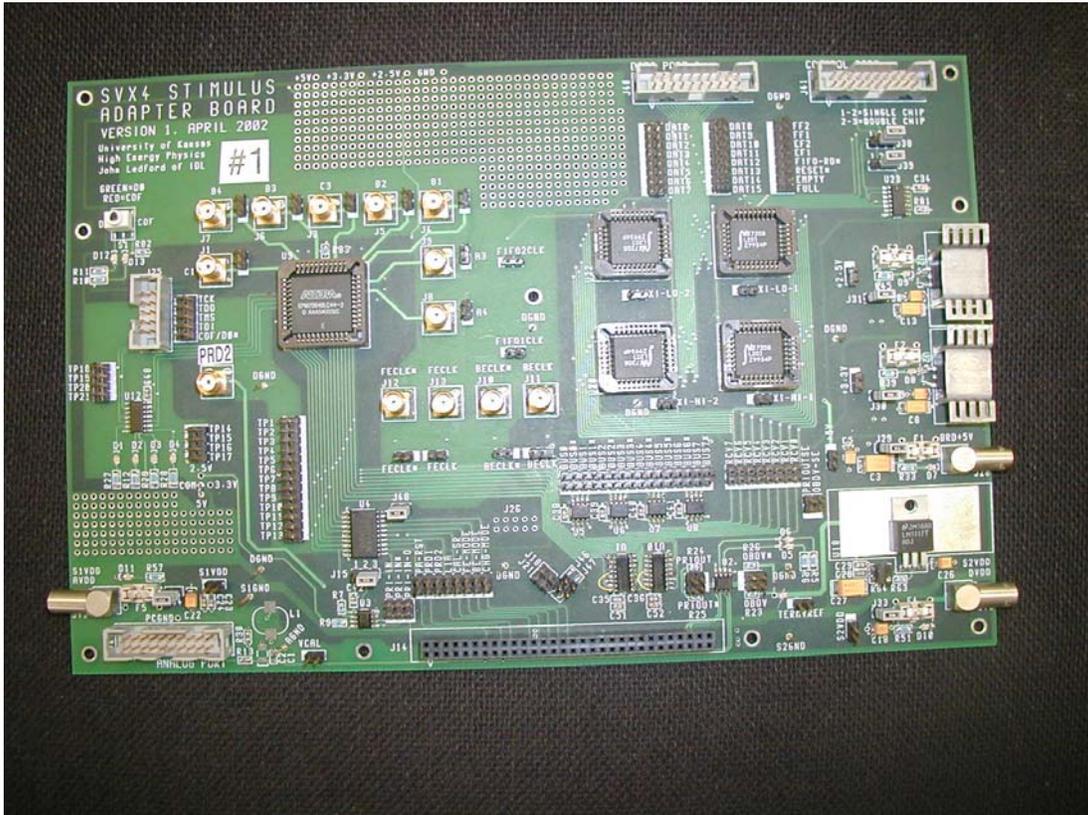


Figure 101: The SVX4 Adaptor Board. The Adaptor Board is used to interface the Stimulus System with the SVX4 chip. This board contains an Altera EPLD which contains a finite state machine used to generate the extra control signal for proper SVX4 operation. It also contains four FIFOs that are used to buffer data between the chip and the computer. The 60 pin connector in the middle of board is the connection used to the SVX4 chip carrier. The Lemo connectors at the sides of the board are used for power connections.

In Figure, we show a cartoon representation of the hardware for the Stimulus Test Stand. The computer sends a pattern to the Stimulus System via the SVX4 Adaptor Board. The SVX4 chip is mounted onto a carrier board. The data from the chip is stored in FIFOs on the Adaptor Board until the computer can read out the data. The Logic Analyzer has two pods which probe test points on the Adaptor Board and gives a graphical representation of the waveform and the data output of the SVX4 chip.

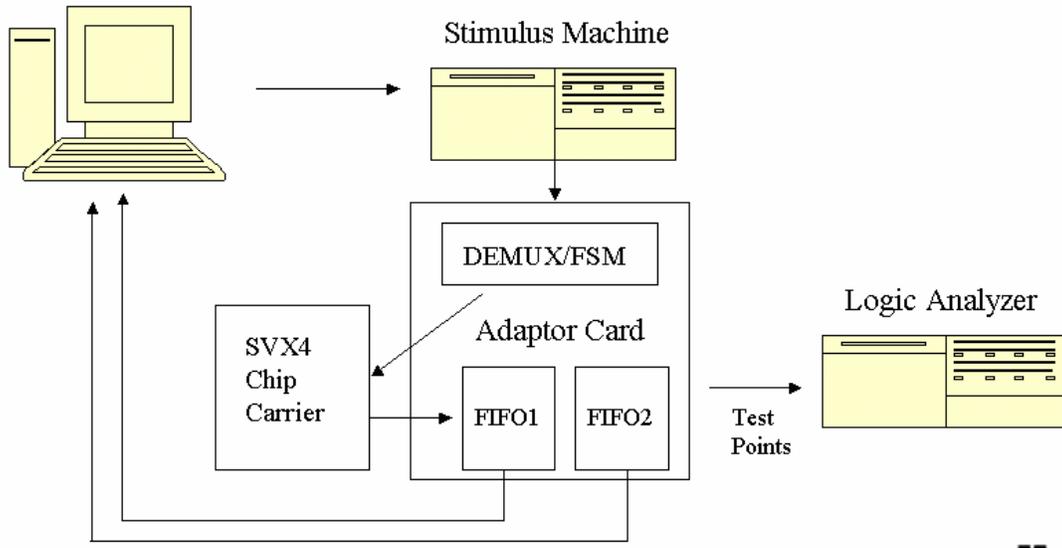


Figure 102. Cartoon representation of the Stimulus Test Stand. The PC is connected to the Stimulus System and the Logic Analyzer through GPIB. The SVX4 Adaptor Board is in the middle with the demultiplexer/finite state machine (programmed inside the EPLD on the board)

The waveforms that are downloaded to the chip are generated algorithmically and can be altered by a graphical waveform display/editor provided by the software. We show the waveforms for the DØ mode and CDF mode of the SVX4 chip in Figure 103.

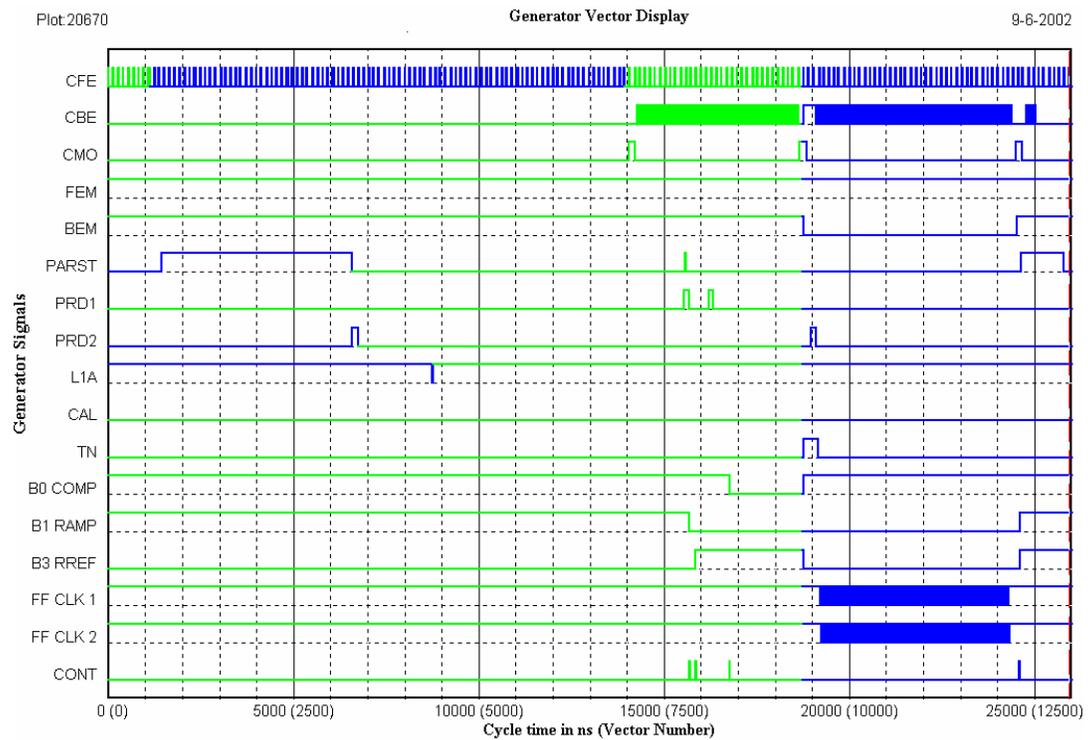
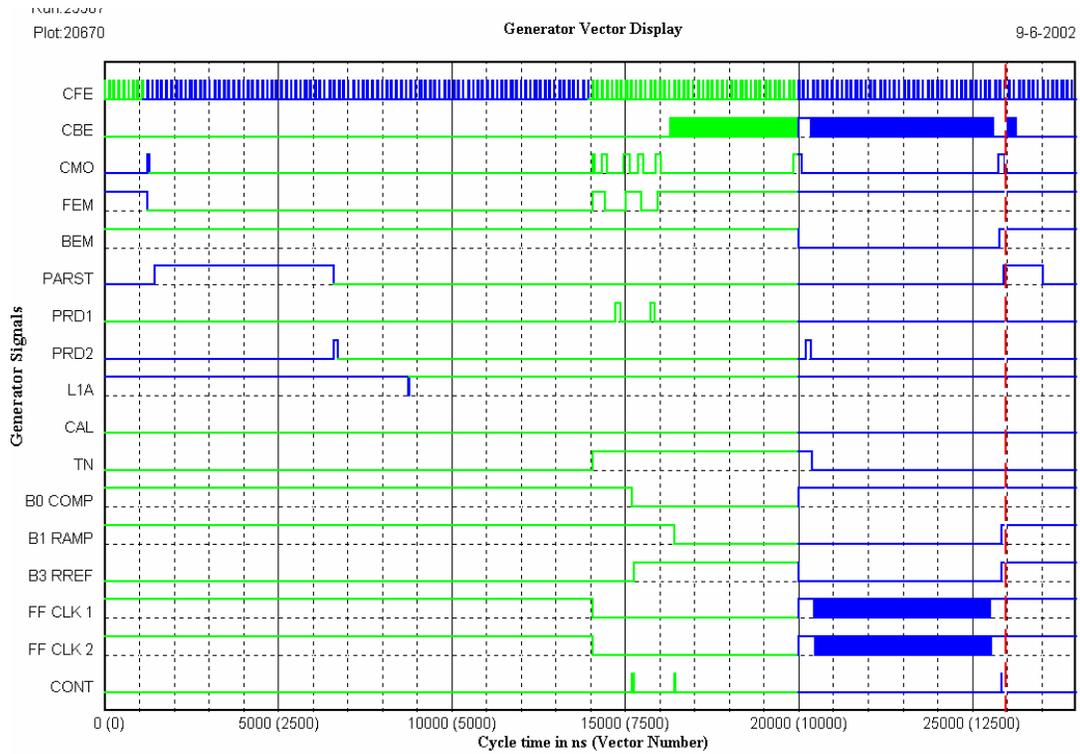


Figure 103. DØ (upper) and CDF (lower) waveforms. These waveforms are generated algorithmically by the DAQ software and are download to the SVX4 chip via the adaptor board. The three signals corresponding to setup of the ADC (COMP, RAMP, and RREF) are shown here only for understanding the timing. The actual signals are generated by the EPLD by using the control (CONT) signal. The FIFO clocks are no longer used.

The stimulus system is fully operational and we are proceeding with the SVX4 performance tests. An interesting measurement done with the setup is study of the current consumption of the SVX4 during an entire data cycle. A data cycle consists of entering the Acquire cycle followed by the Digitization cycle and Readout cycle. We used a calibrated current probe on the individual power supplies (AVDD and DVDD) and then we connected both power supplies together and measured the contribution from both the front-end and back-end from the single supply. This is important because it is necessary to know what the average and peak currents that the power supplies must be able to generate when powering a stave inside the detector.

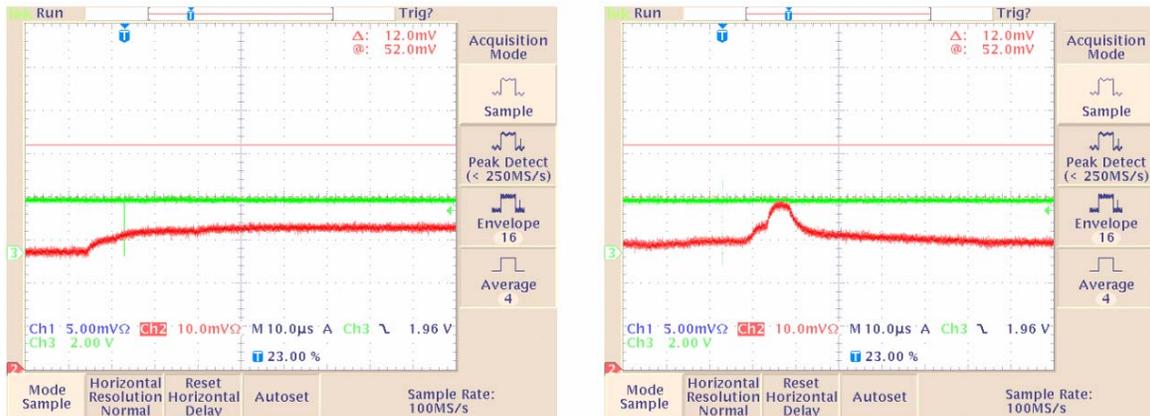


Figure 104. Current consumption of the SVX4 Version 2 chip. The left hand picture is the current consumption for an independent supply connected to AVDD=2.5 V. The vertical scale is 20 milliamps/division with zero in the lower left corner. The right hand picture is the current consumption of an independent power supply connected to DVDD=2.5 V. The scale is also 20 milliamps/division with zero in the lower left corner.

For consistency we powered AVDD and DVDD from one power supply to measure the combined current draw from the front-end and back-end during one data cycle. This is shown in Figure.

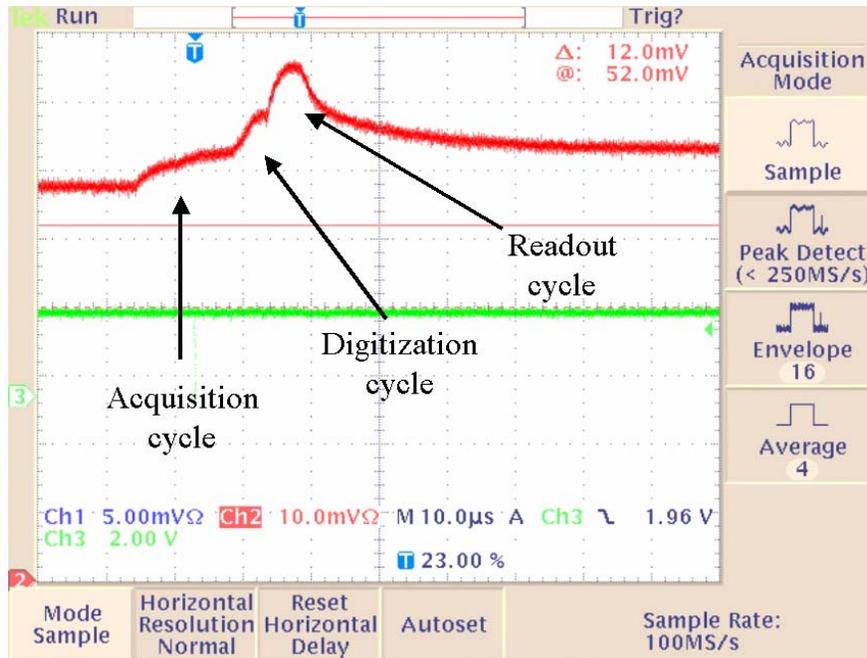


Figure 105. Current consumption of the SVX4 Version 2 chip. The vertical scale is 20 milliamps/division with zero is the lower left corner. Both AVDD and DVDD are connected to the same power supply: AVDD=DVDD=2.5 V. The scale is also 20 milliamps/division with zero in the lower left corner. The sum of the individual currents sum to the total within a few percent.

### 5.3 Analog Cables

In the current design of Layer 0, the analog signals from the silicon sensors are transmitted to the hybrid containing the SVX4 chips by flexible circuits up to 435 mm long with fine-pitch copper traces. While very attractive because of material and heat removal from the sensitive volume, this approach represents a considerable technical challenge. Addition of the analog cable deteriorates the noise performance of the silicon sensors. Procurement of the flex cables and the complicated ladder assembly are other non-trivial issues. Nevertheless, a similar design is used by CDF for the readout of the innermost layer L00 in the Run IIa SVX detector, which can be considered as a proof of technical feasibility.

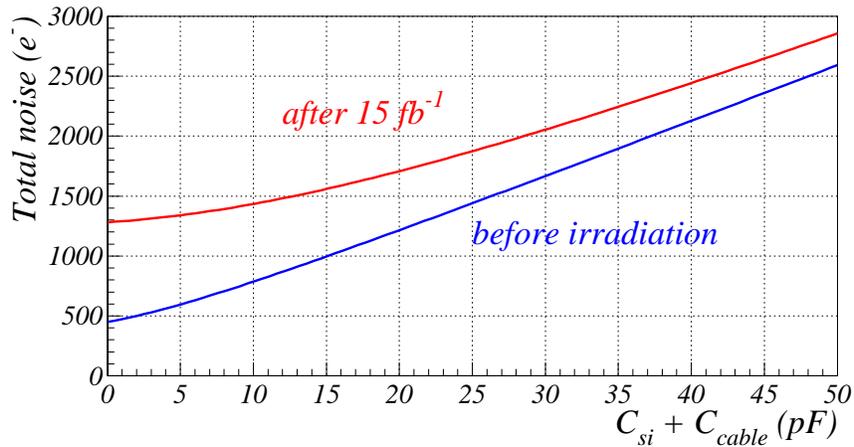


Figure 106. Expectation for the total noise as a function of sum of sensor and cable capacitance.

One of the most important aspects in the design and technical realization of a long analog cable is the capacitance between the traces, which has to be as small as possible. Any load capacitance will contribute to the noise seen by the preamplifier. Our design goal is to maintain a S/N ratio of better than 10 for Layer 0 after irradiation corresponding to  $15 \text{ fb}^{-1}$  of data. Figure 106 shows the expected noise level as a function of capacitance summed over silicon sensor and analog cable. Assuming that a minimum ionizing particle creates 22,000 electrons by traveling through a silicon sensor with the thickness of  $300 \mu\text{m}$ , the total capacitance must be kept below 33 pF to maintain the S/N better than 10 given the measured SVX4 noise performance. The 8 cm long silicon sensor will have about 10 pF of capacitance. This means that the analog cable is required to have capacitance less than 23 pF or  $0.53 \text{ pF/cm}$ .

The flexible dielectric substrate of the cable affects the capacitance. The material of choice in high-energy applications is polyimide such as Kapton HN with a dielectric constant of 3.5 at a frequency of 1MHz. This material is radiation hard with good mechanical and electrical properties. Other synthesized polyimide materials on the market achieve a lower dielectric constant by adding halogens. They are not radiation hard and are not in compliance with CERN and Fermilab fire safety regulations. Although materials like polyethylene or polypropylenes are used in the flex industry and possess a lower dielectric constant, they are also not radiation hard up to the 10-15 MRad level, to which the innermost layer of the silicon tracker will be exposed. The material choices for the flex cable are, therefore, limited to the standard polyimide.

Considering the tight schedule and the technical difficulties, we investigated a design that allows a manufacturer to produce cables reliably, and also satisfies the capacitance requirement.

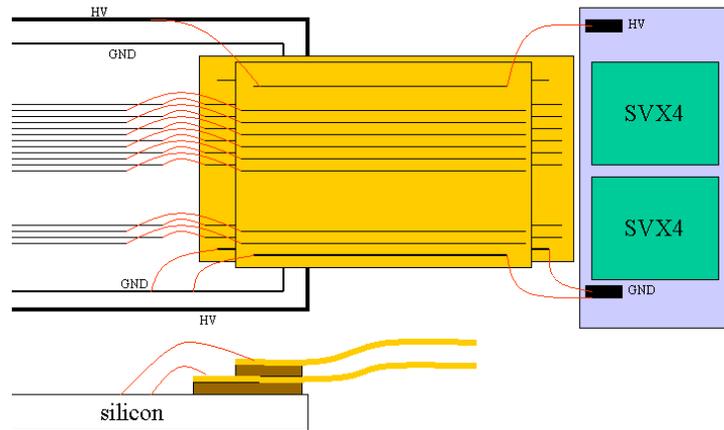


Figure 107. Schematic view of the proposed connections between the sensor, analog cable and the hybrid for Layer 0

Figure 107 shows the schematic view of the proposed arrangement for the sensor, analog cable and the hybrid. Two cables with constant 91 micron pitch are laminated together with a lateral shift of 45  $\mu\text{m}$ . This works effectively as a cable with 45  $\mu\text{m}$  pitch. We think this is a simpler alternative to the L00 approach which has fan-in and fan-out regions adapting the 45 micron pitch to 100 micron pitch. We also investigated the dependence of the cable capacitance on the trace width to understand the trade-off between the reliability and performance.

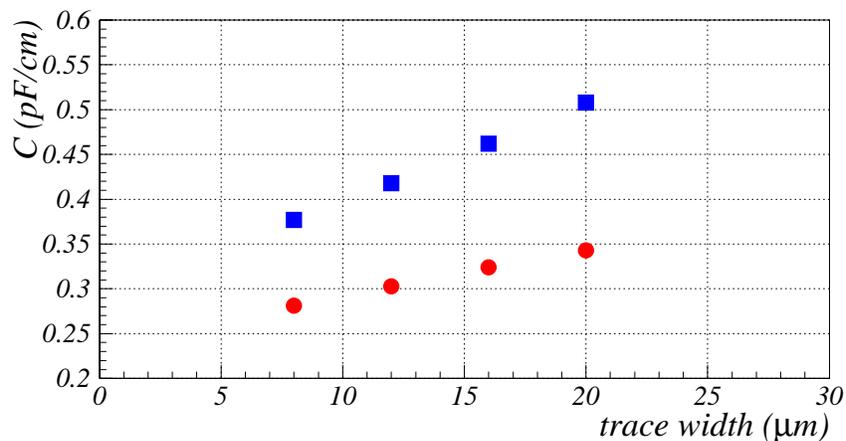


Figure 108. Capacitance calculations by ANSYS. The capacitance of one trace to all other traces is shown as a function of trace width. The blue squares represent 50  $\mu\text{m}$  trace pitch, and red circles 100  $\mu\text{m}$

Figure 108 shows the expected capacitance for various trace width and different pitch by finite element calculations using the ANSYS program. The height of the traces is assumed to be 8  $\mu\text{m}$

in the calculations. It turns out that the 100  $\mu\text{m}$  pitch cable reduces the capacitance by 30% compared to the 50  $\mu\text{m}$  pitch. Besides, the dependence on the trace width is weaker for the 100  $\mu\text{m}$  pitch, correspondingly 0.0052 pF/cm/ $\mu\text{m}$  for the 100  $\mu\text{m}$  pitch and 0.0109 pF/cm/ $\mu\text{m}$  for the 50  $\mu\text{m}$  pitch. Based on this result of the calculations, we adopt the following design as a baseline: 16  $\mu\text{m}$  trace width and 91  $\mu\text{m}$  constant pitch with no fan-in/out region. The 16 micron trace width is a factor of two larger than the trace width of the L00 CDF cable, which we expect to result in increased reliability and higher production yield of the cable. In the final design the pitch is reduced from 100 to 91  $\mu\text{m}$  because the HV trace must hold up to  $\sim 1000$  V and, therefore, needs to be separated by more space on the cable.

In order to reduce the capacitance contribution from the adjacent cables, a spacer will be placed between the cables. A candidate for the spacer material is polypropylene mesh sheet with dielectric constant 3.5. Taking into account the 50% volume occupancy due to the mesh structure, and the possible reduction of the amount of material by punching more holes, the dielectric constant can be effectively as low as 1.5. The thickness of the spacer would be 200  $\mu\text{m}$  at maximum because of mechanical constraints. The capacitances calculated by ANSYS for the configuration with two cables and a spacer are summarized in Table 20.

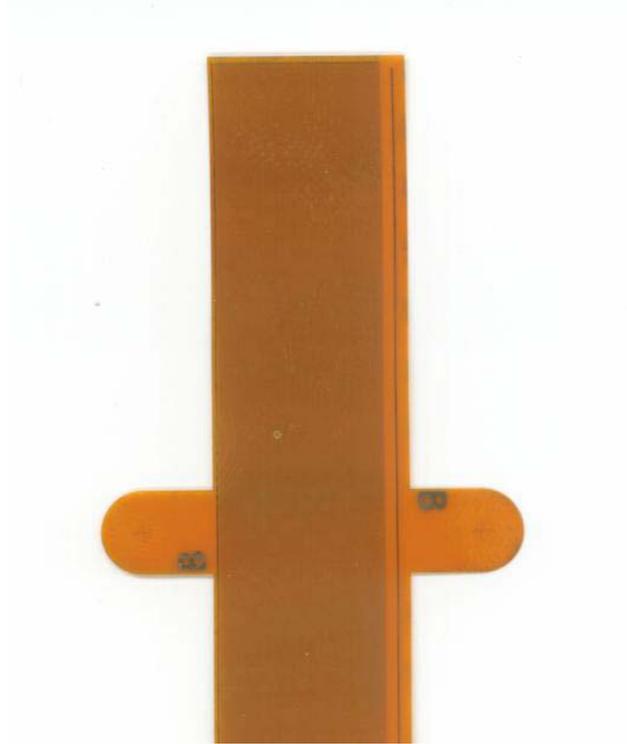
*Table 20. Capacitance in one trace relative to all other traces calculated by ANSYS. The first line is for a single cable, and the other for the configuration where two cables are laminated together with the 200  $\mu\text{m}$  thick spacer. The first column is the dielectric constant for the spacer.*

$\epsilon_r$ of spacer	Capacitance (pF/cm)
Single cable	0.339
1	0.342
2	0.466
3	0.585

This result indicates that separating two cables by a proper spacer can maintain cable capacitance below the required value. From this encouraging result, DØ adopts the method of using two 91  $\mu\text{m}$  pitch cables for one chip readout, in which a pair of cables with a spacer functions as a 45  $\mu\text{m}$  pitch cable. Hence the trace pitch can be almost twice that of the old design, resulting in relief of the technical difficulty.

Based on good prior experience with high density interconnects (HDI) from Dyconex Inc. in Zurich, Switzerland, we contacted them in May 2001. After a few iterations of their prototyping and our technical evaluation, in July 2002 they delivered 27 good prototypes. Figure 109 is a photograph of one of the prototype cables. The copper traces are gold-plated, and the bonding pads have been confirmed to be bondable. Out of the 27 cables, 25 cables satisfy the specification in the number of open traces. While the specification is that 128 traces out of 129 (one trace is spare) are continuous, 16 cables have no opens, and 9 cables have 1 open. Another important requirement is capacitance. The specification is  $<0.40$  pF/cm. The capacitance of one

trace to neighboring two traces has been measured to be 0.30 pF/cm. From ANSYS calculations, 10-15% of increase is expected from contributions besides the two neighbors. Measurements on the old prototype cable with all the traces were shorted together had verified this increase rate. Therefore, 0.35 pF/cm is a fair estimate of the capacitance. This is within the specification.



*Figure 109. Photograph showing the edge of the most recent prototype cable.*

### **5.3.1 Layer 0 Prototype**

In Layer 0, the tight space constraints and heat dissipation require us to use a low-mass analog cable to couple the silicon sensor and the SVX4 chip mounted on the hybrid. As discussed in Section 5.3, special attention has to be paid to the capacitance increase caused by the long analog cable, to avoid degradation of the noise performance. In addition, the experience of the Run IIa L00 in CDF reveals other possible noise sources: noise due to capacitive coupling between the detector and nearby floating metal such as cooling tubes, and also RF pickup noise by the analog cable.

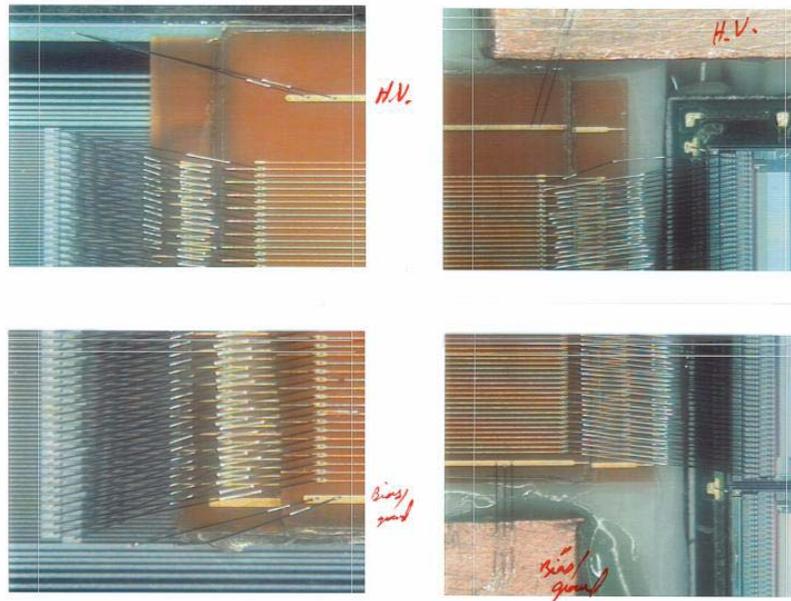


Figure 110. The photograph of the connected region between the sensor and the analog cable (left) and between the cable and the chip (right).

In order to study the effect of these additional noise sources, a L0 prototype was assembled from a L0 prototype sensor manufactured by ELMA, an analog cable manufactured by Dyconex, and a Run IIa hybrid for the readout. The wire-bonding regions for the sensor to the analog cable and for the cable to the chip are displayed in Figure 110. The L0 prototype fixture is put inside a plastic box for light tightness, and is well insulated to avoid any capacitive coupling to the assembly. There are three SVX2 readout chips mounted on the hybrid. Out of the three, two are used to read out the signal from the sensor through the analog cable, while the remaining chip does not have any input loads, and serves as a reference noise level in the test setup. In the noise study described in this section, the noise level is defined as the RMS of pedestal distributions for 100 events.

Apart from the electrical measurements described below, this prototype is a successful demonstration of the proposed arrangement for analog cables. The prototype allowed us to come up with specifications on exact dimensions for the final system and to verify the feasibility of bonding between the cables and the sensor and between the cables and the hybrid.

First we measure the noise level in an electrically quiet environment (accomplished by wrapping the whole fixture by aluminum foil connected to ground), to estimate the amount of additional noise due to the load capacitance of the analog cable. The left plot in Figure 111 shows the noise level for each channel. The projection in each chip is shown in the right. From Gaussian fits of the distributions, the average noise level is 2.2 ADC counts, compared to 1.4 ADC counts in the third (reference) chip. Assuming one ADC count is equivalent to 1000 electrons, the increase of noise level can be translated as 800 electrons. Using the fact that a minimum ionizing particle creates roughly 22,000 electrons in a sensor, the observed noise from the additional capacitive load is acceptable even for the old SVX2 chip.

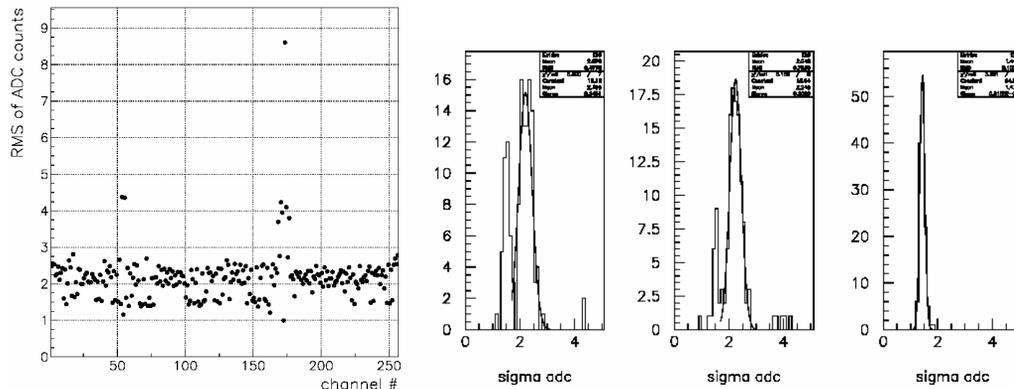


Figure 111. The noise level for each channel (left). The channels with very high (or low) noise are caused by wire-bonding failure. The right plots show the projection of the left one for each of the three chips mounted on the hybrid. The first and second chips are used for the readout, while the third is a reference for the noise level.

The second study is a comparison of the noise levels with and without external shielding. Figure 112 shows the noise for each channel without the shielding. The noise level is increased by 1 to 13 ADC counts (corresponding to 1000 and 13,000 electrons, respectively), depending on the location. This noise increase implies the existence of RF pickup. Another interesting observation is the wing-like shape of the noise distribution. This is attributed to a shielding effect by traces themselves in the middle of cables, where neighboring traces work as a shield for each other; this effect is less significant at the edges of cables. This result unfortunately indicates that the analog cable indeed works as an antenna, and that shielding of the cable is crucial.

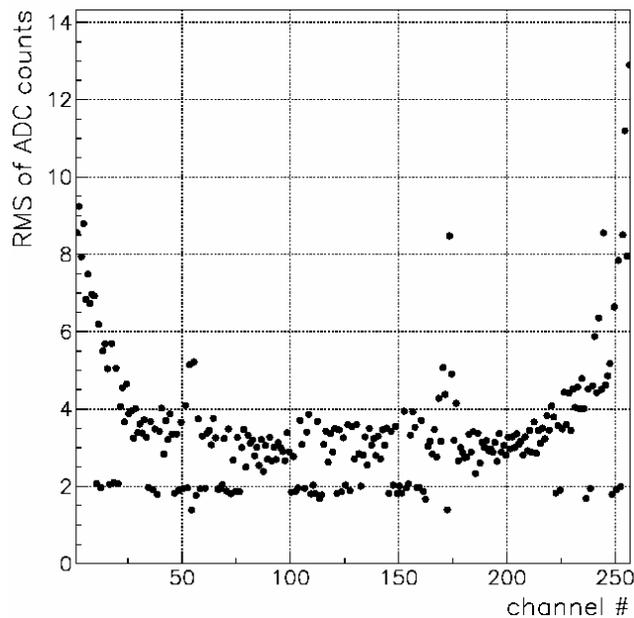
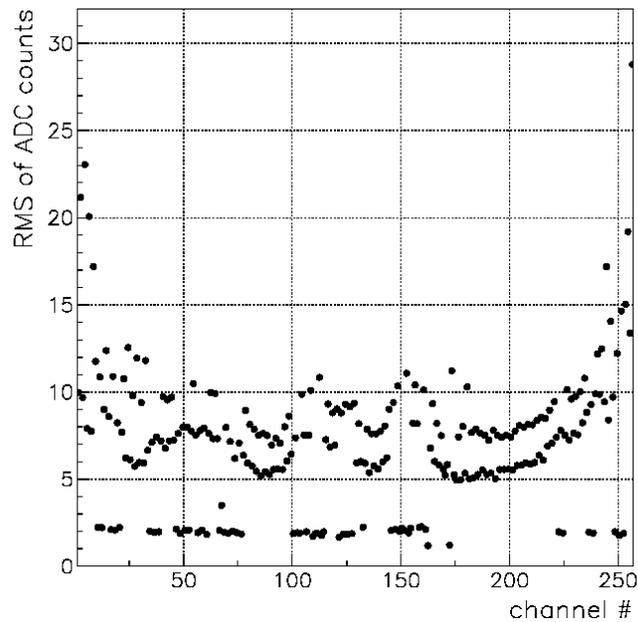


Figure 112. The noise level for each channel. The L0 prototype fixture is not shielded at all.

The next study is for the noise due to capacitive coupling of external sources to the analog cable. We placed a piece of aluminum foil under the analog cable. The aluminum foil was not grounded and thus was floating. Figure 113 shows the noise level for each channel, clearly indicating the capacitive coupling between the analog cable and the aluminum foil by two distinctive features. First, there is an even-odd effect. This comes from the difference in distance between the floating aluminum piece and the signal traces on the cable, i.e. one cable is laminated on top of the other and thus its distance is twice as great. Second, higher noise is observed near non-connected channels (those were bonding failures). The non-connected channels have signal traces without effective grounding through the preamplifier, leading to stronger capacitive coupling to the aluminum foil.



*Figure 113. The noise level for each channel. An aluminum piece without grounding connection is placed under the cable.*

Figure 114 shows the pedestals and noise for a different prototype with a grounded shield. As one can see the grounding removes the noise and pedestal structure and reduces the noise to a level expected from the capacitive load.

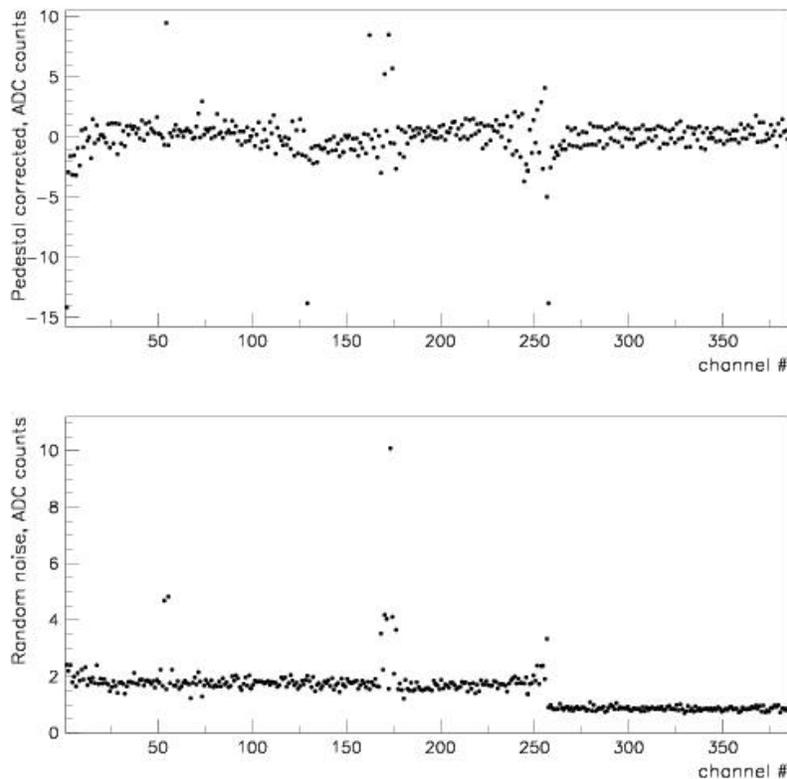


Figure 114. Pedestal and noise for L0 prototype with grounded shielding

From the test results above, a particular concern for L0 is the proximity of sensors to highly conductive K13C carbon fiber, which will be used for cooling tubes and mechanical support structures. These elements have the potential to produce strong capacitive coupling to the sensors, similar to what CDF experienced in Run IIa with L00 cooling tubes, and to what we have seen in the L0 prototype. Therefore, it is imperative that all carbon fiber in the detector be effectively shorted to the bias filter grounds to prevent capacitive noise transmission to the sensor readout.

A test was conducted to determine the feasibility of shorting a prototype L0 carbon fiber cylinder to a filter ground plane. The carbon fiber was driven with the source power from the network analyzer. A sensor/filter mockup constructed of aluminum and Kapton layers was mounted on the cylinder with the network analyzer input wired to the sensor aluminum layer, and both the source and input grounds wired to the filter plane. Transfer functions to the sensor were measured with different configurations for shorting the carbon fiber to the filter plane. Strips of 1  $\mu\text{m}$  thick aluminized Mylar, 0.5 mil aluminum, or copper tape were attached across the filter and carbon fiber. The effectiveness of the grounding strips was tested with and without additional copper tape coupling to the carbon fiber. The aluminized Mylar strips were minimally effective in reducing power to the sensor. Aluminum and copper strips performed equally well. The power reduction was independent of the number of strips, but proportional to the amount of copper tape used to couple the strips to the carbon fiber, up to a maximum reduction of 40 dB at

1 MHz. Further studies determined that aluminum foil embedded in the carbon fiber provides very good coupling for grounding to the filter plane. The embedded aluminum will have 2mm wide strip extensions that will be folded over and shorted to ground pads on the filter. Further details of the carbon fiber grounding studies can be found in 5.15.

Based on the grounding scheme studied above, we plan to assemble another L0 prototype that will be mounted on the carbon fiber structure, in which the carbon fiber is shorted to the bias filter ground through the 2 mm wide aluminum strip. Noise reduction by this proposed grounding scheme must be identified with the prototype module.

## 5.4 Hybrids

This section describes the hybrid design and related electrical issues for the stave design. The proposed beryllia hybrids minimize the amount of material in the detector and are a well-established technique used previously in a number of experiments.

Commonly, the circuits connecting the SVX chips to the low mass jumper cable are called “hybrids.” The hybrids will be based on the technology of thick film deposition on ceramics successfully used in a number of high energy physics experiments including all CDF SVX detectors and the CLEO microvertex detector<sup>27</sup>. In our case, the 380 micron beryllia substrate will be used to reduce the amount of material in Layers 1 through 5 where the hybrids will be mounted directly in the sensitive volume. For Layer 0 which has off-board hybrids at higher Z, the material issue is of less importance. However, beryllia ceramic is preferred here because of its significantly better thermal conductivity with respect to alumina.

Thick film deposition by screen-printing is a mature technology allowing for a minimal via size in dielectric of 200 micron and minimum trace width of 100 micron. Multi-layer designs are routinely achievable. Typical thickness of dielectric and metal layers are 40 and 7 micron, respectively. We have identified CPT, Oceanside CA and Amitron, NH as our potential vendors. Both companies have solid backgrounds in hybrid production.

There are four types of hybrids in the proposed design. Two of them are 10-chip, double-ended versions for Layers 2 through 5: one for axial sensors (L2A hybrid) and one for stereo sensors (L2S hybrid). The others are a 6-chip, double-ended version for Layer 1 (L1 hybrid) and a 2-chip version for Layer 0 (L0 hybrid).

In addition to providing a secure mount for the SVX chips and cable connector, the hybrids also have capacitors for bypassing the analog and digital voltages and the detector bias. The low-mass flat cable connects to the hybrid with an AVX connector plug (hybrid side) and receptacle (cable side). These are 0.5mm pitch, low profile 50-pin connectors with a maximum height of 3.1 mm above the surface of the hybrid. The CDF Run IIa SVX detector uses similar connectors with a low failure rate. Placement of the connector on the hybrid allows for easy testing of hybrids with and without attached silicon sensors during all phases of the hybrid and stave production. This is essential for the modularity of the design and for quality checking during

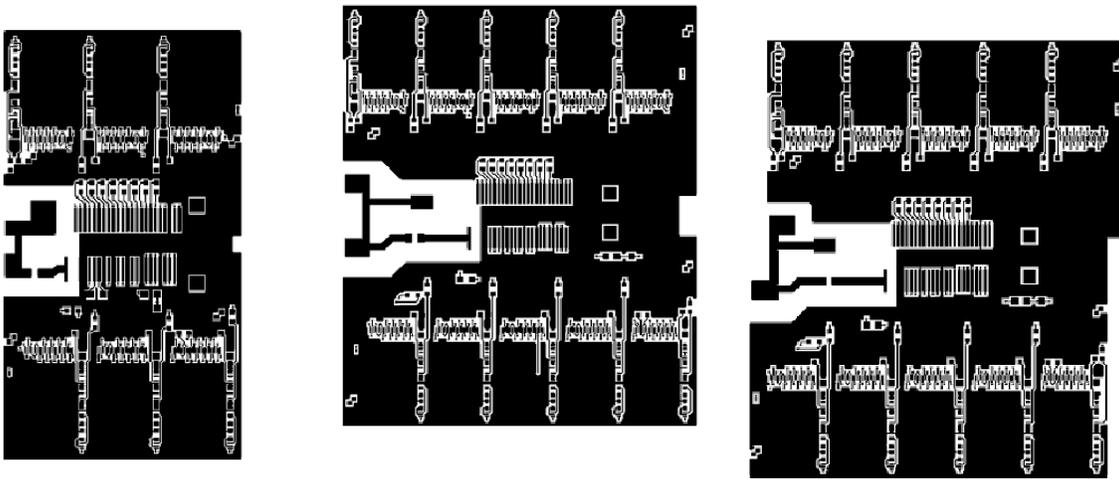
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<sup>27</sup> Nucl.Inst.Meth. **A435**, 9-15, 1999.

stave production. The extra material introduced by the connector is small and is crossed by particles only after two precise measurements in Layers 0 and 1.

The SVX control signals and readout bus lines are routed from the connector to the SVX4 chips via 100-micron wide traces. The traces stop near the back edge of each chip, where they transition into gold-plated bond pads. Aluminum wire bonds connect these pads to the bond pads on the chips. The chip power will be routed from the connector on a power plane, and there will be a dedicated ground plane in the hybrid. The total number of metal layers is 6.

Figure 115 shows the top metal layers of L1, L2A and L2S hybrids. As one can see, the layout of all these hybrids is very similar to each other. The dimensions of these hybrids are 45mm x 25mm for L1, 50mm x 41.9mm for L2A and 50mm x 43.8mm for L2S. The total hybrid thickness is specified to be smaller than 0.9 mm.



*Figure 115. Top metal layer for L1 hybrid (left), L2A hybrid (center) and L2S hybrid (right)*

Figure 116 specifies the adopted channel numbering scheme for 10-chip hybrids. The first chip to read out will be the chip in the corner closest to the HV pin on the connector. The readout then proceeds anti-clockwise with respect to the hybrid top side. The order of channels inside the chip is also shown. Six-chip L1 hybrids and two-chip L0 hybrids will be read out similarly.

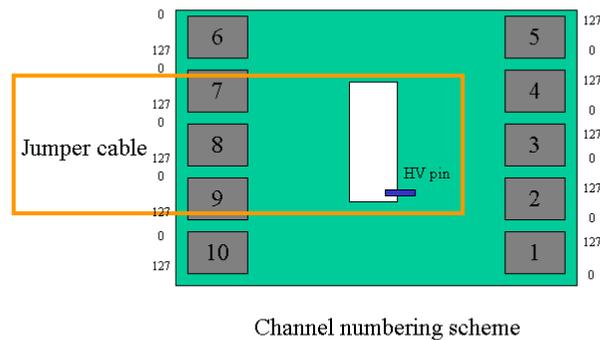
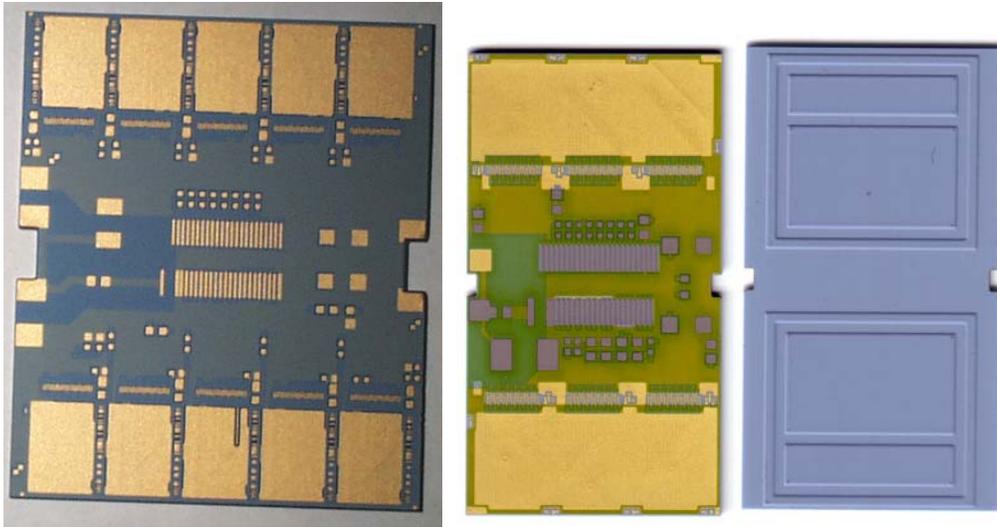


Figure 116. Numbering scheme for 10-chip hybrid

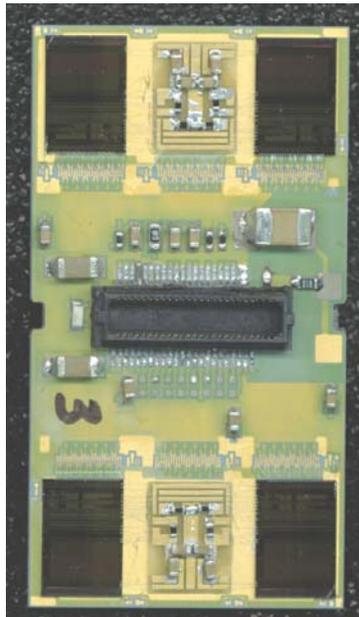
We received 18 prototypes of the L1 hybrid from CPT in April 2002, and 23 prototypes of L2A hybrids from Amitron in July 2002. All CPT hybrids passed electrical tests for continuity and shorts. We found, however, one open trace on 4 Amitron hybrids. The flatness of the CPT hybrids was measured to be within the specification of 50 microns. The Amitron hybrids showed a considerable bowing, approximately a factor of 3 larger than the specification.

Figure 117 shows the prototype hybrids: top view of L2A hybrid from Amitron (left); L1 hybrid from CPT, top view (center) and bottom view (right). Notice that the L1 hybrid has no components or traces in the inter-chip area. This particular prototype has been developed under the assumption of a separate small board (“finger”) placed between chips to provide all side bonding connections. This design is used by the CDF SVX detector in Run IIa. Later we abandoned this idea and found a way to integrate the finger into the hybrid, thus making overall design simpler. The L2A prototype has all necessary side components integrated in the layout. The back side of all hybrids will have a special printing to avoid glue in the area of the guard ring; see right photo in Figure 117. This should improve the breakdown voltage (hence, the radiation hardness) of the design, preventing potential discharge path through the glue in the region of the largest voltage difference between the edge of the detector and the first signal traces. The printing has two “pedestals” in the central area of the backside raising the hybrid above the guard rings of both sensors.



*Figure 117. Prototype hybrids : Top view of L2A hybrid from Amitron (left); L1 hybrid from CPT, top view (center) and bottom view (right).*

In July 2002 we assembled several L1 prototype hybrids (Figure 118). The prototype has 4 SVX4 chips at the corners of the hybrid. The two central chips were replaced by a simple finger kludge board to provide all side connections for two neighboring chips.



*Figure 118. Prototype L1 hybrid*

Using this hybrid and two prototype L1 sensors from ELMA we also assembled a L1 prototype module (Figure 119). Only two chips, #2 (bottom left) and #3 (bottom right) were bonded to sensors.

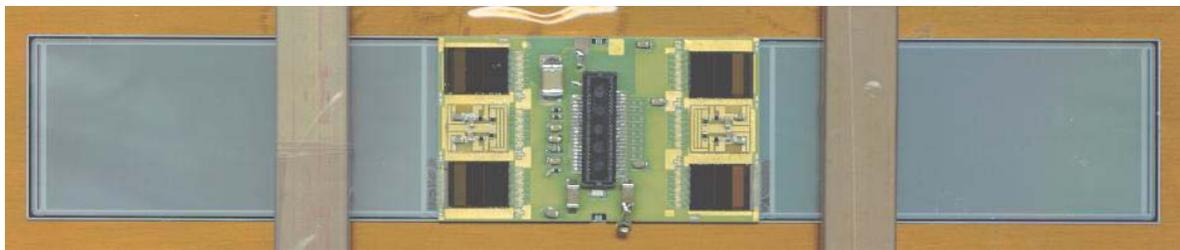


Figure 119. L1 prototype module

Figure 120 shows the channel ID, pedestal and total noise  $\times 10$  from readout of this L1 module. Noise is defined as the RMS of the pedestal. Four SVX4 chips are represented on the plot. The channel ID is incremented for each of them from 0 to 127. The value of pedestal was set at around 30 ADC counts. The noise level is approximately 1.0 ADC counts for chips 1 and 4, and 1.7 ADC counts for chips 2 and 3. The difference is explained by the extra capacitance load from the silicon sensors. The sensors were biased above depletion voltage at 50V. The total HV current for both sensors was 1.5  $\mu\text{A}$ . Several noisy channels are visible for chips bonded to the detector. Making some assumptions about calibrations, we determine a preliminary noise of 700 e for bare chip and 1100 e for chips connected to silicon. This corresponds to a S/N of  $\sim 20:1$  for the prototype module, assuming a MIP signal is 22000 e. Work is in progress to improve understanding of the noise level.

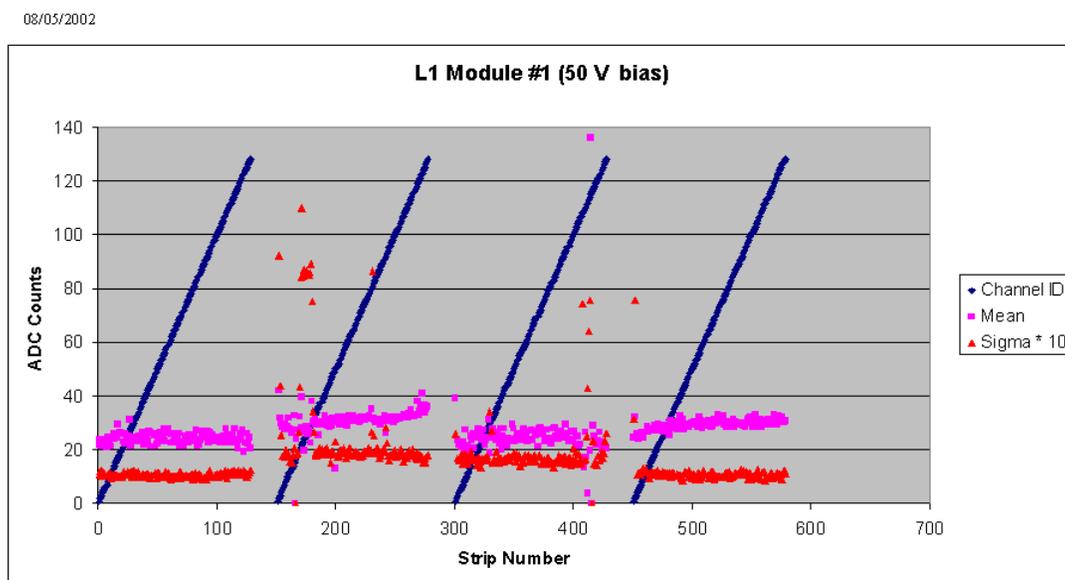


Figure 120. Channel ID, pedestal and noise plots for L1 prototype module

## 5.5 Cables, Adapter Card and Interface Board Overview

A primary goal of the Run IIB readout chain design is to preserve as much of the Run IIA electronics and cable plant as possible. In particular, we want to keep: 1) the Interface Boards (IBs), located at the base of the central calorimeter, that relay digital signals between the sequencers and the SVX4 chip, supply both low-voltage power and high-voltage bias, and monitor current and temperature; 2) the high-mass cables, consisting of 3M 80 conductor cables and parallel coaxial clock cables that run from the IBs to Adapter Cards on the calorimeter face. Because of the complexity of these IBs, any required changes beyond the scope of component replacements or hand-wired jumpers will likely mandate complete replacement. Also, the space for connectors on the IB face is saturated. A required line count into the IB exceeding that available on the 80-conductor cables could not be accommodated.

As described below, the present design aims to preserve the IBs by replacing the Run IIA passive Adapter Cards on the calorimeter face with active ones that translate between single-ended (IB) and differential (SVX4) signals, and that also regulate supply voltages. The long (up to 2.7 m) Run IIA low-mass cables, which do not have differential-signal capability, will be replaced with new cables comprised of Twisted Pairs connected by small, passive Junction Cards to new, relatively short, low-mass Digital Jumper Cables.

## 5.6 Digital Jumper Cables

Digital Jumper Cables (DJCs) will carry digital signals and power between the hybrids and the Junction Cards, where they connect to the Twisted-Pair Cables. In all, each DJC carries 11 pairs of differential signals, 6 single-ended signals, 5 sense lines, 2 power voltages and ground, and sensor bias of up to 1000 V. They will be flex-circuit striplines similar to the low-mass cables used in Run IIA, which minimize the amount of material in the sensitive volume. Although they will be shorter than the Run IIA cables, they will be narrower and carry more signal traces, so that the feature size is 20% smaller. There will be 888 DJC's 14.7 mm wide, with a distribution of lengths between 44 cm and 103 cm. Signal traces 125 microns wide with 300 micron pitch, and also broad power and ground traces, will be located on both sides of a Kapton dielectric 102 microns thick. The layout for all five layers is the same, with a 50-pin, 0.5 mm pitch AVX 5046 connector soldered to pads on both ends. DJC's for Layers 2-5 will be made with 1-ounce rather than ½-ounce copper traces because of their larger (10-chip) power requirements. The DJC's will be reinforced by thin G10 backing behind the connectors to make them more robust during handling. Photographs of one end of a 50 cm prototype DJC (before connector installation) are shown in Figure 121 and Figure 122.



Figure 121. Digital jumper prototype cable: side opposite the connector



Figure 122. Digital jumper prototype cable : connector side

The prototyping program aims to qualify at least two vendors as well as to validate the design. As of 30 August 2002, one vendor (Honeywell FM&T) has successfully produced both 50 cm and 100 cm prototypes, while a second (Basic Electronics, Inc.) has produced 50 cm cables and is now working on the 100 cm version.

A hybrid stuffed with four SVX4 chips has been successfully read out with a 50 cm DJC. In addition, thirty 50-cm prototypes have so far been bench-tested, both singly and daisy-chained to make a 100 cm cable. The results are: 1) only a few fabrication defects have been found, all of them bad solder joints at the connectors; 2) the high-voltage trace gives no problems, even at several hundred volts above the required 1000 V; 3) signal quality after 100 cm is good; 4) measured impedances (107 ohms for differential lines, 61 ohms for single-ended lines) are close to design values; 5) cross-talk is negligible for differential lines and acceptable ( $\leq 13\%$ ) for single-ended lines.

## 5.7 Junction Cards

Junction Cards are impedance-controlled passive boards that mate Digital Jumper Cables with the Twisted-Pair Cables that run to the Adapter Cards. They will be mounted near the present location of the Run IIA H-disks, and will have a maximum size of  $25 \times 90 \text{ mm}^2$ . Junction Cards must be mechanically robust and securely mounted. All attached cabling will be stress-relieved whenever possible. The Twisted-Pair Cables will be soldered to one end of the cards for increased strength, while the Digital Jumper Cables will plug into 50-pin AVX 5046 connectors. Junction Cards for Layers 0 and 1 will each join three pairs of cables, while those for Layers 2 – 5 will each join two pairs. Bypass capacitors to smooth the supply voltages will also be located on the Junction Cards because there is limited space for large capacitors on the hybrids.

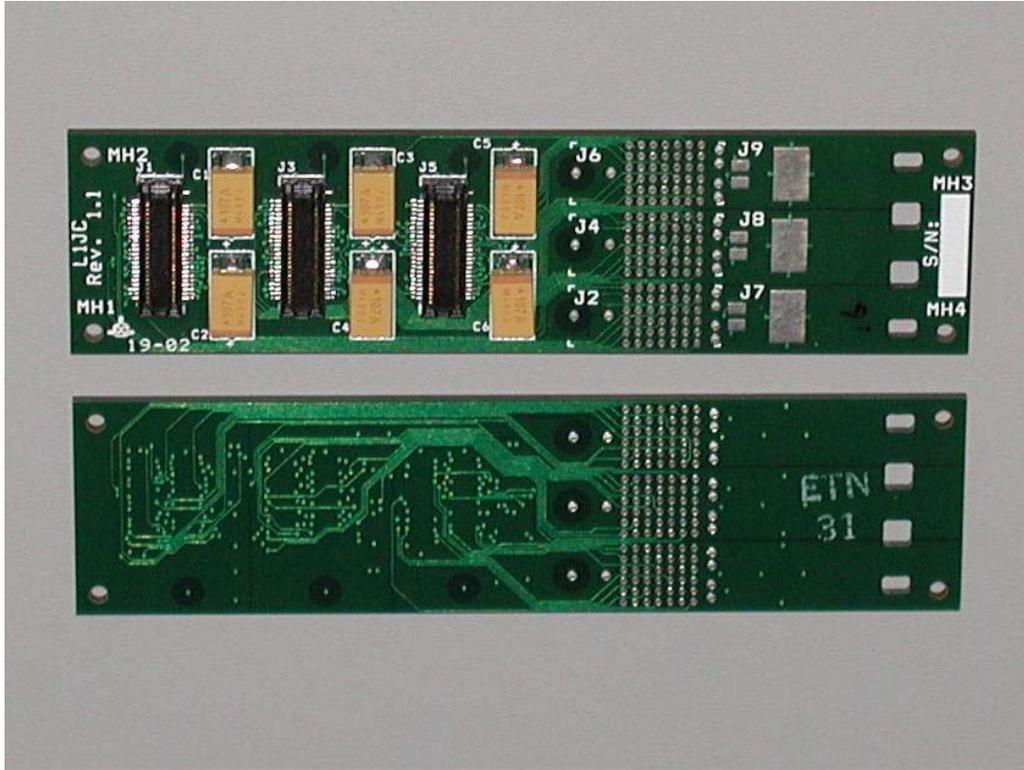


Figure 123. Prototype junction card

As of 30 August 2002, prototypes for the L0-1 Junction Cards were in hand, and the schematic for the L2-5 version is complete. Figure 123 is a photograph of a prototype Junction Card.

## 5.8 Twisted Pair Cable

The Twisted Pair Cable, approximately 2 meters long, connects the Junction Cards and Adapter Cards. The cable is soldered to the Junction Card on one side and is terminated by connectors on the Adapter Card side. The cable mass is not a major issue because the cable is outside of the tracking volume. The total outer diameter of a Twisted Pair bundle can be as small as 5-6 mm.

The twisted pairs were chosen because 11 of the signals used by the SVX4 chip are differential. The 5 slower single ended lines will also use twisted pairs. The cable assembly has 2 power lines and their returns, 1 HV line and its return, 15 signal twisted pairs, one temperature sensor twisted pair and 2 voltage sensor pairs. The clock signals are transmitted via two coaxial cables in the same assembly. Two versions of the Twisted Pair Cable are envisioned (Layers 0-1, Layers 2-5) depending on the HV and power requirements.

Figure 124 specifies connections between junction card and adapter card.

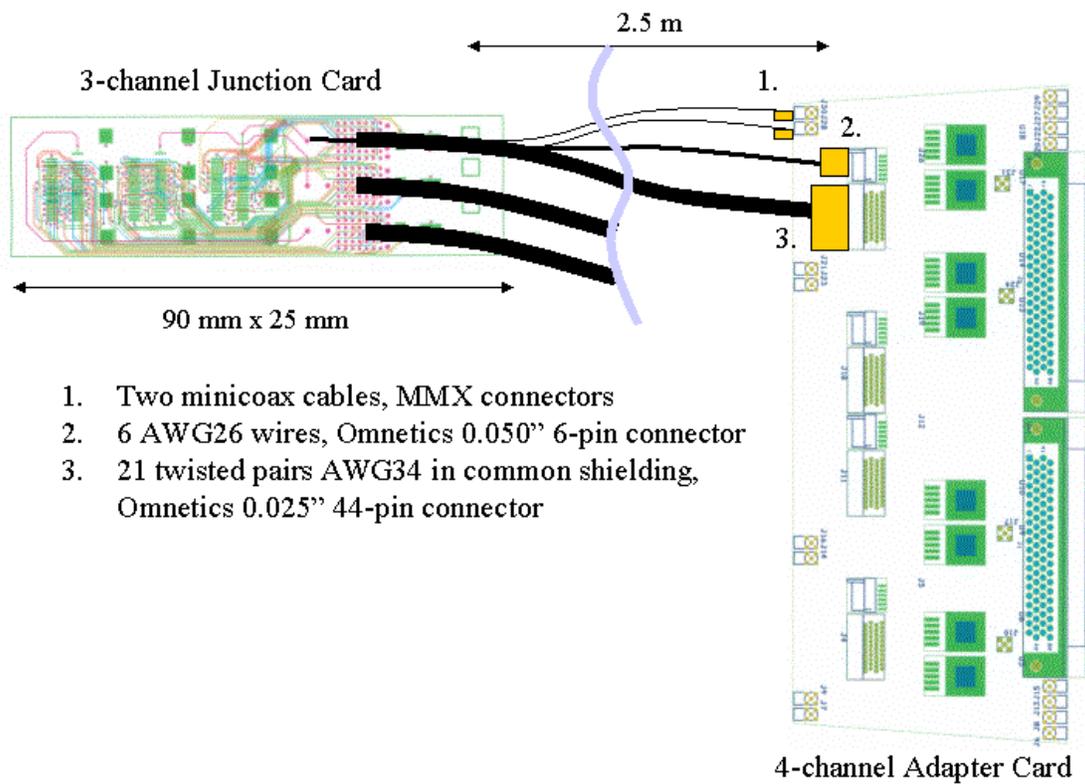


Figure 124. Schematic connection between junction card and adapter card

Figure 125 shows prototype cables for the twisted pair cable assembly; from left to right : two connectors for micro-coax cables, 44-pin Omnetics connector for signal pairs, 6-pin Omnetics connector for HV and power lines. The signal twisted pair was produced by New England Wire and was terminated to the connector by Omnetics.



Figure 125. Prototype cables for the twisted pair assembly; from left to right : two connectors for micro-coax cables, 44-pin Omnetics connector for signal pairs, 6-pin Omnetics connector for HV and power lines.

## 5.9 Adapter Card

For Run IIB, new active Adapter Cards will replace the passive cards now mounted on large “horseshoes” on the north and south faces of the calorimeter. They will 1) translate single-ended TTL logic signals from the Interface Cards to differential signals to and from the SVX4 chips; 2) regenerate clock signals; 3) regulate the two 2.5 volt SVX4 supply lines to within the narrow 250 mV tolerances of the SVX4. To use the limited mounting space more efficiently, each Adapter Card will service four or six channels rather than the two channels of Run IIA. Each pair of channels requires an 80-pin mini-D connector and four miniature coax connectors to interface with the High Mass Cables and associated clock coax cables, and two fine-pitch connectors on the Twisted-Pair side. Additional connectors are required for powering the adapter board itself, and for strobing lines.

Suitable components have been found and tested for signal translation and refreshing, and a voltage-sensing regulator circuit that will use sense lines in the Twisted Pair and Digital Jumper Cables has been successfully bench-tested. Layout of the prototype boards is complete (Figure 126), and three have been fabricated and tested. The largest remaining issue is how to remove the heat, about 600 watts on each calorimeter face. Heat sinks must be designed to transfer heat

effectively from Adapter Card components to the horseshoe mounting plates, and the horseshoes themselves must be cooled.

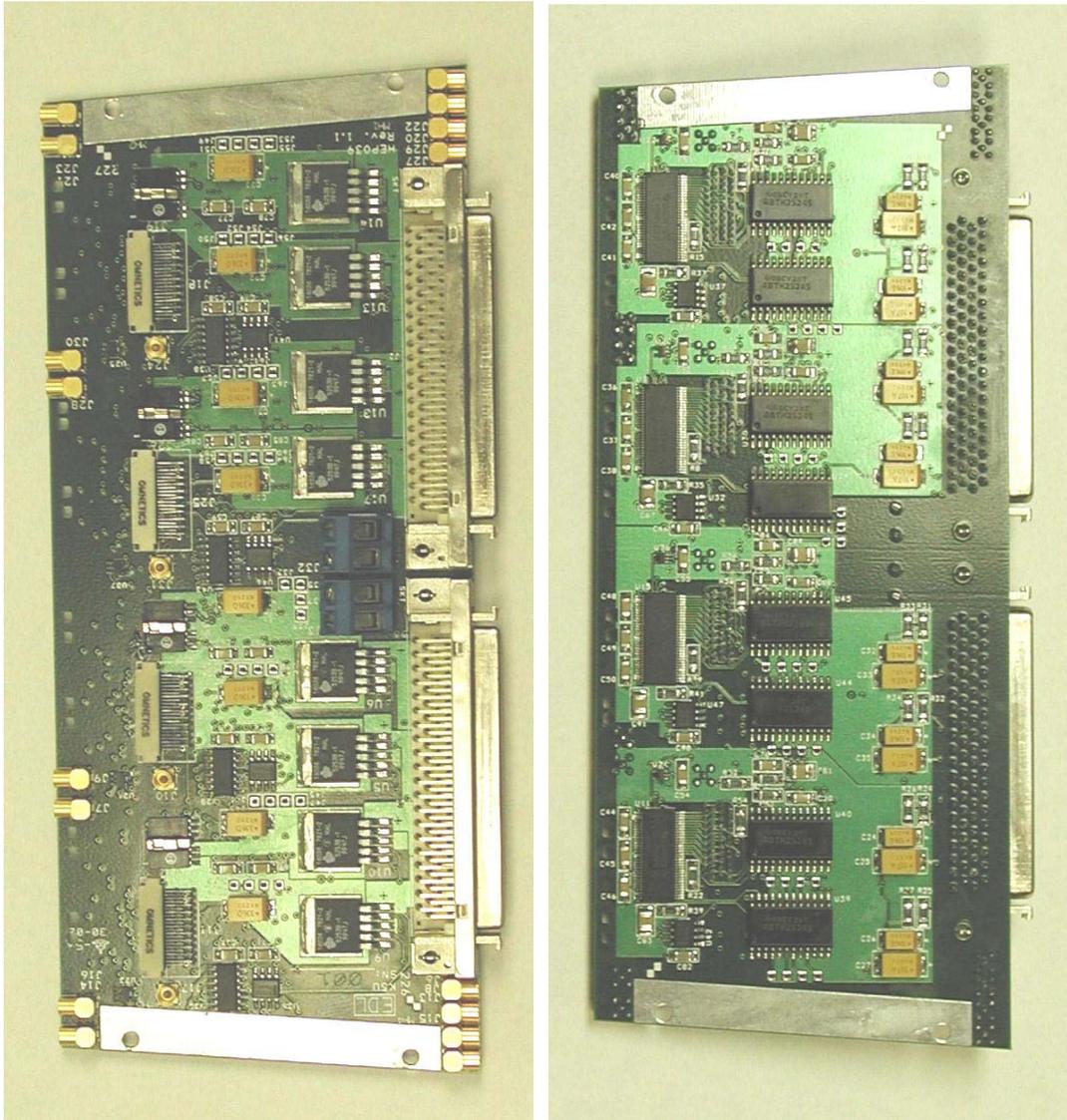


Figure 126. Top and bottom sides of a prototype adapter card

## 5.9.1 Adapter Card Implementation Details

Table 21 - Preliminary adapter card input connector (80 conductor cable from interface board).

Pin #	Function	Pin #	Function
1	Secondary Bias A	41	NC
2	GND	42	NC
3	GND	43	Primary Bias A
4	GND	44	3.3 V
5	Temperature A	45	3.3 V
6	VCAL A	46	3.3 V
7	D7 A	47	3.3 V
8	D6 A	48	2.5 V Unregulated AVDD A
9	D5 A	49	2.5 V Unregulated AVDD A
10	D4 A	50	2.5 V Unregulated AVDD A
11	D3 A	51	2.5 V Unregulated AVDD A
12	D2 A	52	2.5 V Unregulated AVDD A
13	D1 A	53	2.5 V Unregulated AVDD A
14	D0 A	54	2.5 V Unregulated AVDD A
15	Priority In A	55	2.5 V Unregulated DVDD A
16	Mode 0 A	56	2.5 V Unregulated DVDD A
17	Mode 1 A	57	2.5 V Unregulated DVDD A
18	Change Mode A	58	2.5 V Unregulated DVDD A
19	DValid A	59	2.5 V Unregulated DVDD A
20	Priority Out A	60	2.5 V Unregulated DVDD A
21	GND	61	3.3 V
22	Temperature B	62	3.3 V
23	VCAL B	63	3.3 V
24	D7B	64	3.3 V
25	D6 B	65	2.5 V Unregulated AVDD B
26	D5 B	66	2.5 V Unregulated AVDD B
27	D4 B	67	2.5 V Unregulated AVDD B
28	D3 B	68	2.5 V Unregulated AVDD B
29	D2 B	69	2.5 V Unregulated AVDD B
30	D1 B	70	2.5 V Unregulated AVDD B
31	D0 B	71	2.5 V Unregulated AVDD B
32	Priority In B	72	2.5 V Unregulated DVDD B
33	Mode 0 B	73	2.5 V Unregulated DVDD B
34	Mode 1 B	74	2.5 V Unregulated DVDD B
35	Change Mode B	75	2.5 V Unregulated DVDD B
36	DValid B	76	2.5 V Unregulated DVDD B
37	Priority Out B	77	2.5 V Unregulated DVDD B
38	Primary Bias B	78	GND
39	NC	79	GND
40	NC	80	Secondary Bias B

Table 22 - Preliminary adapter card output connector pinout.

Pin #	Function	Pin #	Function
1	Primary Bias	21	D2+
2	Secondary Bias	22	D2-
3	AVDD	23	D1+
4	GND	24	D1-
5	Sense A +	25	D0+
6	Sense A -	26	D0-
7	Temperature	27	DV+
8	Temperature Return	28	DV-
9	VCAL	29	Priority Out +
10	NC	30	Priority Out -
11	D7+	31	Clock +
12	D7-	32	Clock -
13	D6+	33	Mode 0
14	D6-	34	Mode 1
15	D5+	35	Change Mode
16	D5-	36	Priority In
17	D4+	37	Sense D +
18	D4-	38	Sense D -
19	D3+	39	GND
20	D3-	40	DVDD

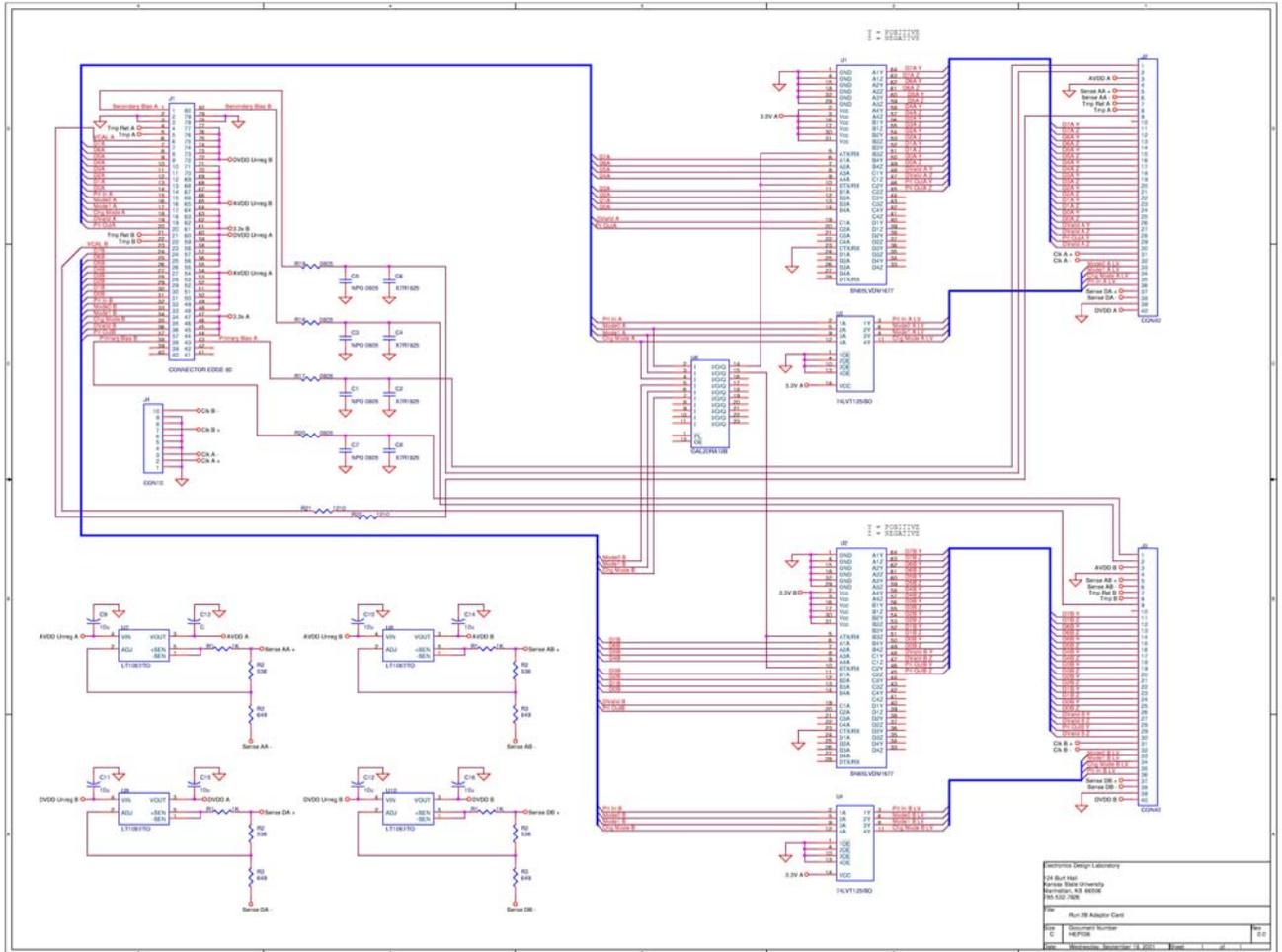


Figure 127 - Preliminary schematic for the adapter card.

### 5.9.2 Purple Card

A variant of the Adapter Card, called the “Purple Card”, will be used in test stands for testing and burn-in of hybrids and sensors. The Purple Cards combine the functions of the Adapter Cards and Twisted-Pair Cables, and some functions of the Interface Boards, in these simplified test stands; they serve as an interface between the same Stand-Alone Sequencers used in the Run IIA test stands and Digital Jumper Cables. Engineering information gleaned from early use of the Purple Cards will be applied to improve the Adapter Card design. As of 30 August 2002, six Purple Cards have been built, and a Purple Card has successfully read out a 4-chip hybrid. A second iteration on this card is underway, incorporating modest design and layout revisions motivated by SVX4 testing. Figure 128 shows a prototype Purple Card.

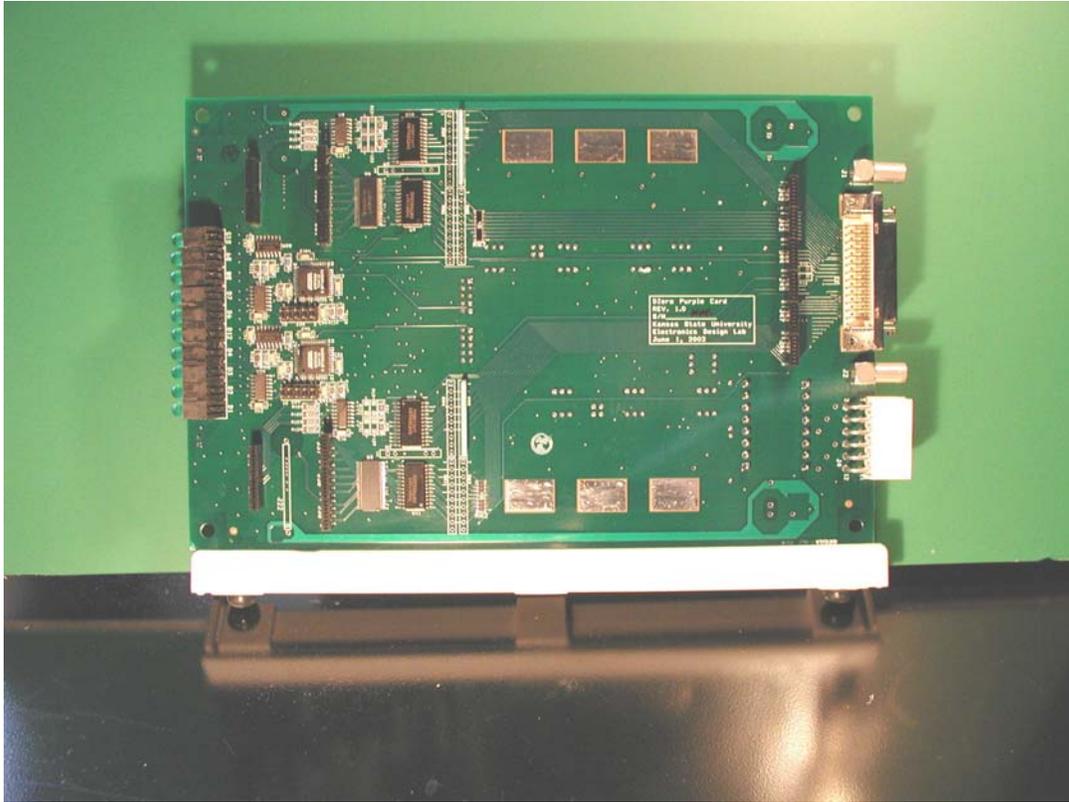


Figure 128. View of a prototype Purple Card

## 5.10 Interface Board

In order to avoid the considerable expense of designing and building new Interface Boards (IB), the existing IBs must be recycled. All new features for Run IIb are incorporated into the active Adapter Card. The IB detector bias distribution was tested to + 200 V, -100 V (including the switching relay) and should be safe for 300 V for silicon Layers 2-5. Bias cables for Layers 0-1 (up to 1000 V) cannot go through either the IB's or the existing high-mass cables, but will be routed separately.

Required changes on the IB which have been identified to date include: 1) replacing data line terminations (24 resistor changes per channel); 2) probable changes in control line termination, and in the clock equalizer circuit; 3) new set points for current and temperature trips; 4) reprogramming of 5 PLDs; 6) changes to priority-out signal threshold and hysteresis (this line was underdriven by the SVX2 chip). The total number of changes is about 200 per IB.

## 5.11 Sequencer

The firmware in the sequencer needs to be adjusted for the difference between the SVX4 chip operating in the SVX2 mode and real SVX2 chip. The changes are rather straightforward and imply remapping of the SVX2 lines to SVX4 lines. The required remapping was shown in the section describing the SVX4 chip.

## 5.12 Low Voltage Distribution

Currently VICOR switching power supplies<sup>28</sup> are used to provide power for the SVX2 chips and Interface Boards. For Run IIb we intend to preserve those supplies and the distribution scheme through the Interface Boards.

The massive power lines from the VICOR supplies are split between different channels in the fuse panel. After the individual protection fuses, the power is distributed to the custom J1 backplane of 9U x 280 mm custom crates. The J2 and J3 backplanes of the crates provide connectors for the cable runs to the sequencers, while J1 contains connectors for low-voltage power for each Interface Board and up to eight dependent silicon hybrids, the 1553 connector and bus (used to monitor the SVX4 power and current, and hybrid temperature), and a connector to bring in 16 bias voltages and returns for eight hybrids.

We are investigating the feasibility of replacing the J1 backplane. This would have the benefit of eliminating the existing fuse panels; these panels are time-consuming to wire, and contain ~150 fuses which experience has shown to be somewhat unreliable due to oxidation of contacts. A small number of fuses would still need to be placed for safety reasons on J1 and perhaps on the IB (replacing existing ferrite beads there). Another advantage of J1 replacement is that remote sensing from the external power supplies would go to the J1 bus instead of stopping at the fuse panel. We will have more space at the backplane because a 34-pin bias connector can be replaced with a smaller one, since the new single sided detectors only need one bias voltage. The feasibility of this scheme must be established, and mechanical and electrical layouts need to be done. The Interface Board side of the backplane would be unchanged.

## 5.13 High Voltage Distribution

Reliable high voltage operation is crucial to ensure the increased radiation tolerance of the new Silicon Tracker. Operation at voltages up to +1000 V is specified for the Layers 0 and 1 and up to +300 V for the Layers 2 through 5.

The high voltage bias will be applied to the backplane of the single-sided silicon sensors. For 10-chip hybrids the high voltage will arrive at the hybrid on the Jumper Cable and will be routed to a side pin of the AVX connector. Two neighboring pins will be removed to ensure a safe distance to the nearest ground. The proposed scheme has been tested to operate reliably to 2 kV with a prototype jumper cable and a stuffed L1 prototype hybrid. The bias voltage will be brought to the sensor backplane with a foil wrapped around the sensor edge and glued to the backplane with a conductive silver epoxy. The foil will be insulated from the sensor edge and from the outside with a 50 micron Kapton tape. For Layer 1 the backplane connection will be provided similarly to the 10-chip hybrids while for Layer 0 the bias voltage will be fed to a line on the analog cable and then will be connected to the backplane of the sensor near the end of the cable.

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<sup>28</sup> 4 kw MegaPAC AC-DC Switcher, Vicor Corporation, Andover, MA.

Despite the fact that Run IIa silicon detectors require operating bias voltages only within  $\pm 100$  V, the specifications of the existing Run IIa HV power supplies are adequate for Run IIb detectors. Software compatibility and reliable operation of the current system during the first year of Run IIa are two other important considerations. Therefore, the most straightforward upgrade path for the HV system will be to keep the existing Run IIa system increasing the number of channels as needed.

For all layers one HV line is used per hybrid. Therefore, each sensor in Layer 0, two sensors in Layer 1 and two or four sensors in Layers 2-5 will share the same HV line. The total number of HV lines is 888 corresponding to the total number of hybrids. A possibility of bias splitting between two or more hybrids in the outer layers should be considered to reduce the number of HV channels. The table below shows HV currents per strip, per hybrid and per stave calculated for sensors irradiated by equivalent of 15 inverse fb. For layers 2-4 the 20 cm long sensor gangs were considered for calculation of current per hybrid.

Table 23. HV currents per strip, per hybrid and per stave for Layers 0-4

Layer	Radius,m	uA/strip	uA/hybrid	uA/stave
0	18	1.2	310	NA
1	35	0.46	360	NA
2	54	0.28	530 max	1790
3	86	0.12	230 max	770
4	116	0.06	180 max	550

Based on the above information the proposed splitting of the HV channels is the following:

- One HV channel per hybrid for layers 0,1 and 2
- One HV channel per two hybrids for layer 3
- One HV channel per stave (i.e. four hybrids) for layers 4 and 5

The splitting equalizes currents for HV channels servicing different layers. The total number of required HV channels in the proposed scheme is 492.

In the Run IIa system, bias voltages are supplied from a BiRa VME 4877PS High Voltage Power Supply System<sup>29</sup>. The system utilizes the three HVS power supply types shown in Table 24.

<sup>29</sup> Model VME 4877PS High Voltage Power Supply System Manual, March 1988, Bi Ra Systems, Albuquerque, NM.

Over-voltage protection is provided through trim potentiometers located on the front panel of the modules.

*Table 24 - HVS power supply types used in the DØ Run IIa silicon bias voltage system.*

HVS type	max output voltage, kV	max output current, mA	number of channels
HVS5.5P-1	+5.5	2.3	116
HVS5.5N-1	-5.5	2.3	152
HVS2P	+2.0	3.2	116

Each of the ten VME crates in the Run IIa HV system holds a Power PC controller and six motherboards containing eight Bi Ra power supplies each. Power to the VME crates is delivered from Lambda power supplies. Run IIb system with 492 HV channels will require 62 motherboards, as well as 11 VME crates with controllers and power supplies. It is prudent to assume some amount of spare channels so we plan to populate all 66 slots in 11 crates with motherboards that will increase the total channel count to 528. In terms of infrastructure this will not be a big change since the current SMT HV system is already using 10 VME crates. However, the number of positive HV pods will need to be increased considerably.

The Run IIa fanout and breakout boxes will need a replacement. The fanout boxes are used to split HV channels between different HDIs and to provide hardware protection against accidental application of HV higher than 150 V. The breakout boxes are used to distribute HV to the Interface Boards and to transfer temperature signals from the Interface Boards to interlock control systems. For Run IIb design we plan to combine the fanout and breakout boxes and move the temperature control functionality to a separate system.

It has been checked that the HV path through the Interface Board and 80-conductor cables can sustain up to 300 V and, therefore, can be preserved in Run IIb for Layer 2-5 bias distribution. The design goal for HV distribution for the inner two Layers is operation at 1000 V. In this case, the HV cabling needs to bypass the Interface Board and go directly to the Adapter Card via a separate cable.

## 5.14 Performance

Increased luminosity in Run IIb will result in high occupancy in the detector especially for the inner layers. This has several implications for the readout performance. Two areas of concern, the SVX4 dynamic range and the detector readout time, were addressed in our simulations with results presented in this Section.

The charge-sensitive preamplifier of the SVX4 chip integrates incoming signals and, therefore, needs to be reset regularly to prevent saturation. The saturated preamplifier will result in

inefficiency of the detector. The reset time in SVX4 is equal to several hundred nano-seconds. Usually the resets are performed during the Tevatron abort gaps, which are periods of time within one revolution without collisions. Along with other modifications the high luminosity regime of the Tevatron operation in Run IIB will include reduction of the available abort gaps to possibly one per revolution. The current 36 bunches x 36 bunches operation allows for 3 abort gaps per revolution.

The full GEANT simulation with the Run IIB geometry discussed in Section 8.5, and realistic clustering in the silicon has been used to estimate charge accumulated per strip after 450 minimum bias events. A scenario of 150 beam crossings before a reset with 3 minimum bias interactions per beam crossing was assumed. Figure 129 shows the charge per strip in the innermost layer after 450 minimum bias events. The left plot corresponds to the sensors in the central (closest to  $z=0$ ) barrels. The right plot corresponds to the sensors in the end barrels. The central sensors are crossed by a larger number of particles while the incidence angles are shallower for the end sensors allowing for a larger deposited charge. As shown by arrows in both cases about 1% of strips will receive charge in excess of approximately 100 fC, which corresponds to 25 minimum ionizing particles. The dynamic range of the SVX4 chip was chosen to be 200 fC, leaving some margin for high luminosity operation. The expected inefficiency caused by the preamplifier saturation is expected to be less than 0.1%.

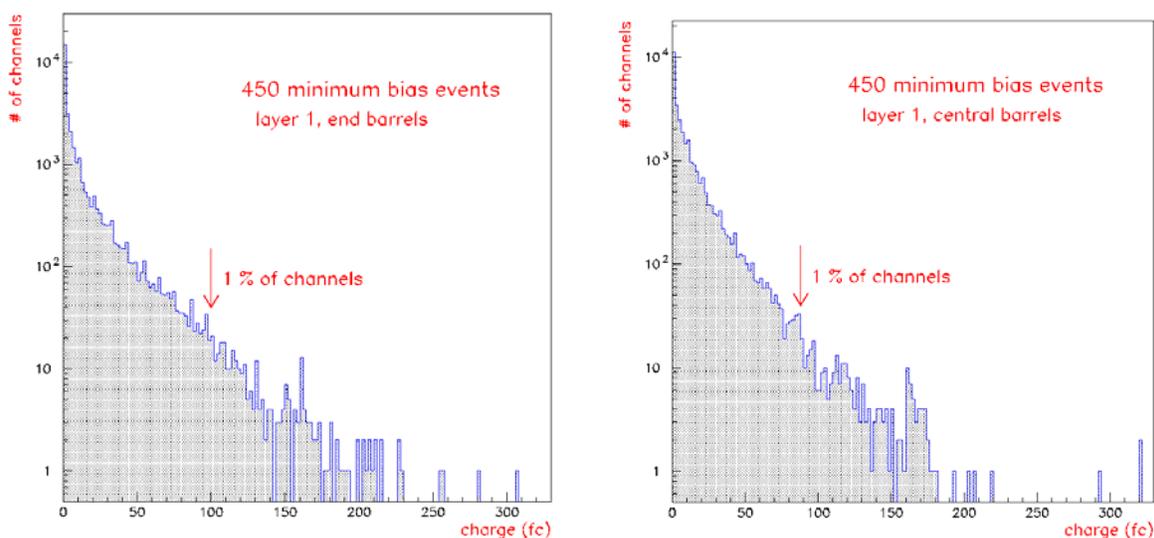


Figure 129 - Charge per strip in the innermost layer (labeled layer 1 in the figure) after 450 minimum bias events. The left plot corresponds to the sensors in the central, closest to  $z=0$ , barrels. The right plot corresponds to the sensors in the end barrels.

Another important performance issue for data acquisition is the readout time. A p-pbar interaction triggered for readout will be accompanied by several minimum bias interactions. To investigate a wider range of Level 1 triggers, several simulated samples were used: minimum bias, two jet and WH events. The maximum number of strips per readout cable in a layer was determined for each event. This number corresponds to the slowest chain of readout in this layer

and is relevant to estimate the readout time for the detector and the associated dead time. The number of hit strips has been scaled by appropriate factors to account for the closest neighbors that normally are also included in the sparse mode readout. The factors were determined from the cluster size distributions and were typically around 1.7 for the cases without noise and 2.8 for the cases with noise. Figure 130 shows the maximum number of strips per readout cable as a function of radius for minimum bias events (left plot) and QCD two jet events (right plot). Each layer corresponds to two points in those plots from different sublayers. Four different cases were considered: without noise for the two thresholds of 4 and 5 ADC counts, and with noise (rms 2.1 ADC counts) for the same thresholds. The average simulated signal was equal to 20 ADC counts corresponding to a S/N ratio of 9.5. Figure 131 shows the maximum number of strips per readout cable as a function of radius for WH + 0 minimum bias events (left plot) and WH + six minimum bias events (right plot).

Comparison of the inner three layers with the highest rates suggests that Layer 1 with 6 chips in the readout chain and Layer 2 with 10 chips will operate in similar conditions for all types of events. Layer 0 with 2 chips in the readout chain has rates a factor of 2 lower. However, this layer will experience the worst radiation damage and, as a result, a lower S/N. The effect of the noise on occupancy depends on the threshold. For the threshold over noise ratio equal to 2.4 the deterioration of S/N from 9.5 to 8 increases the maximum number of readout strips by 40% in Layer 0, by 50% in Layer 1 and by 75% in Layer 2, all for two jet events. The largest increase is observed in the 10-chip readout chain of Layer 2 due to the simple fact that the number of noisy strips is proportional to the number of chips. A lower S/N ratio in the innermost layer 0 can easily increase the number of readout strips by a factor of two and make its rate comparable to the Layers 1 and 2. As a result of these simulations, we feel it is prudent to daisy-chain only two chips in Layer 0 and leave a safety margin to accommodate higher noise occupancy in this layer after irradiation.

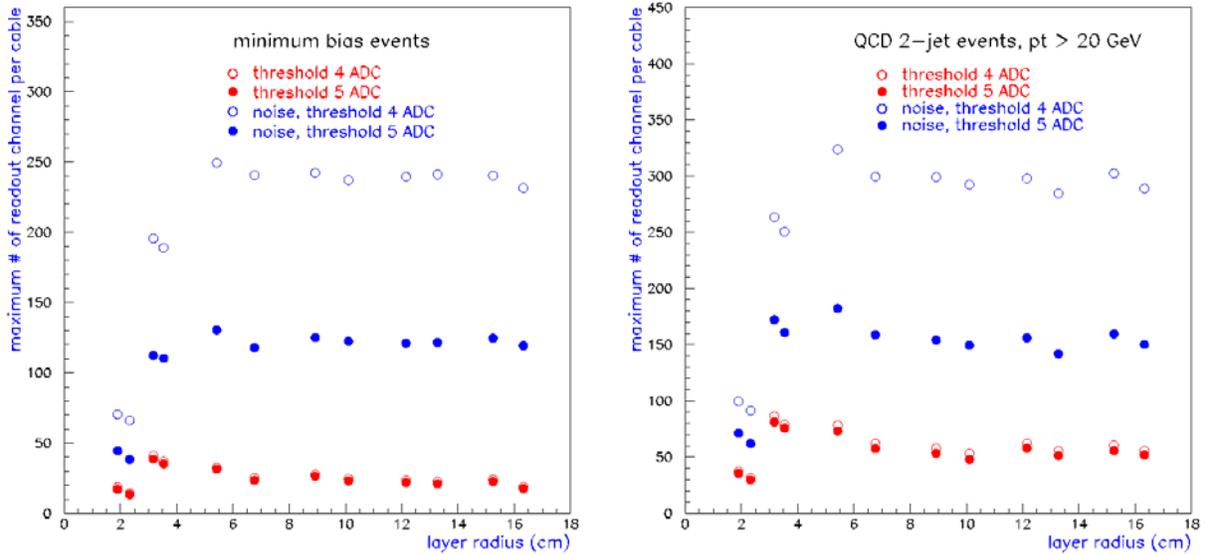


Figure 130 - Maximum number of strips per readout cable as function of radius for minimum bias events and QCD two jet events

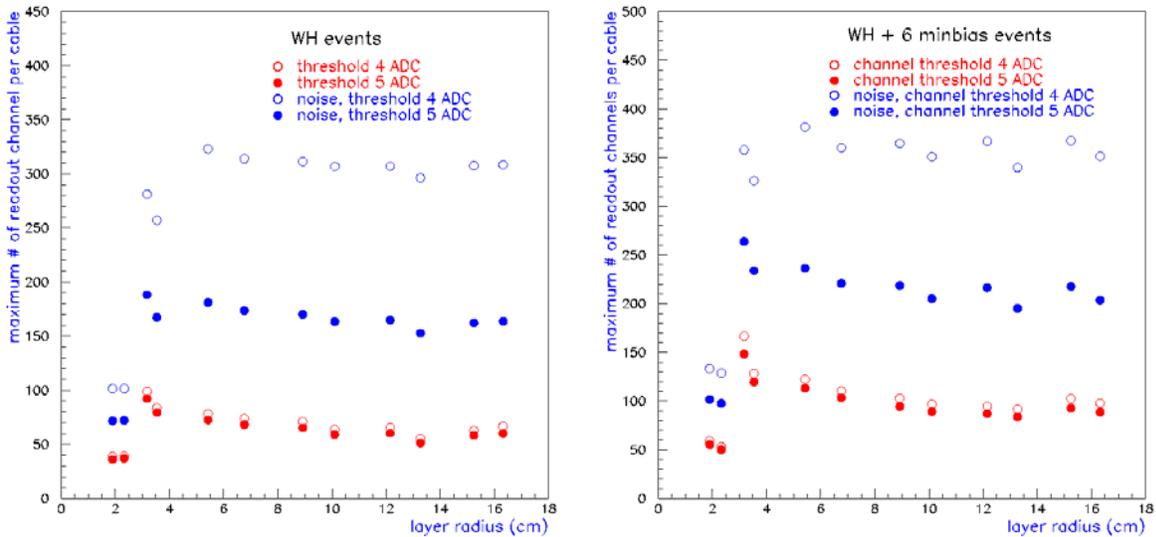


Figure 131 - Maximum number of strips per readout cable as function of radius for WH + 0 minimum bias events and WH + 6 minimum bias events.

The above information is useful for the evaluation of the deadtime. The readout of SVX4 is driven by a 53 MHz clock. Two bytes of data per channel (address and amplitude) require two clock cycles. This gives a total readout time of an SVX4 chip of about 4 microseconds for a typical occupancy of 100 strips. The deadtime will be determined by the SVX4 digitization time, readout time and the pipeline reset time after the readout. Though the correct calculation

should combine information from all silicon layers and all levels of the DØ trigger in a queue analysis, essentially one buffer structure of the DØ data acquisition makes a simple rough estimate possible. The total deadtime can be estimated as

$$3 \text{ (digitization)} + 4 \text{ (readout)} + 4.2 \text{ (pipeline reset)} = 11.2 \text{ microseconds}$$

At 10 kHz Level2 trigger input rate, corresponding to 100 microseconds between Level\_1\_Accept signals, the deadtime will be equal to approximately 11.2%. The deadtime and the readout time are acceptable for the DØ data acquisition system and in particular for the Silicon Track Trigger at Level 2.

## 5.15 Carbon Fiber Grounding Studies

A significant concern in the electronic and mechanical design of the detector is the proper grounding of carbon fiber elements. Highly conductive carbon fiber will be used for the cooling tubes and mechanical support structures. These carbon fiber elements have the potential to exhibit strong capacitive coupling to the sensors. The experience of CDF in Run IIa with L00 cooling tubes has shown that sensor coupling to nearby floating metal can be a very troublesome source of noise. It is imperative that all carbon fiber in the detector is effectively shorted to the hybrid (L1-L5) or bias filter (L0) grounds to prevent capacitive noise transmission to the sensor readout.

The first test on the carbon fiber was to verify its conductivity through capacitive coupling. Two identically sized plate capacitors were constructed: the first with one copper plate and one type K139 carbon fiber plate, the second with two copper plates. Both capacitors were measured to be  $132 \pm 2$  pF. Additionally, each capacitor was individually connected in series to a network analyzer to produce a high-pass filter. The transfer functions and break frequencies for the two capacitors were identical. Therefore, the conductivity of the K139 carbon fiber is high enough to make it virtually indistinguishable from copper in terms of capacitive noise transmission. Furthermore, K139 is the carbon fiber type that will be used in L2-L5. K13C, which is more conductive than K139, will be used in L0-L1 where the proximity of sensors to carbon fiber is much greater.

Because the grounding concerns are most acute in L0, a test was conducted to determine the feasibility of shorting a prototype L0 K13C carbon fiber cylinder to a hybrid or filter ground plane. The test configuration is shown in Figure 132. The interior of the castellated L0 cylinder was driven with the source power from the network analyzer. A sensor/filter mockup constructed of aluminum and Kapton layers was mounted on the cylinder with the network analyzer input wired to the sensor aluminum layer, and both the source and input grounds wired to the filter plane. Transfer functions to the sensor were measured with different configurations for shorting the carbon fiber to the filter plane. One to four 1/8" wide strips of 1  $\mu$ m thick aluminized Mylar, 0.5 mil aluminum, or copper tape were attached across the filter and carbon fiber. The effectiveness of the grounding strips was tested with and without additional copper tape coupling to the carbon fiber. The aluminized Mylar strips were minimally effective in reducing power to the sensor. Aluminum and copper strips performed equally well. The power

reduction was independent of the number of strips, but proportional to the amount of copper tape used to couple the strips to the carbon fiber, up to a maximum reduction of 40 dB at 1 MHz.

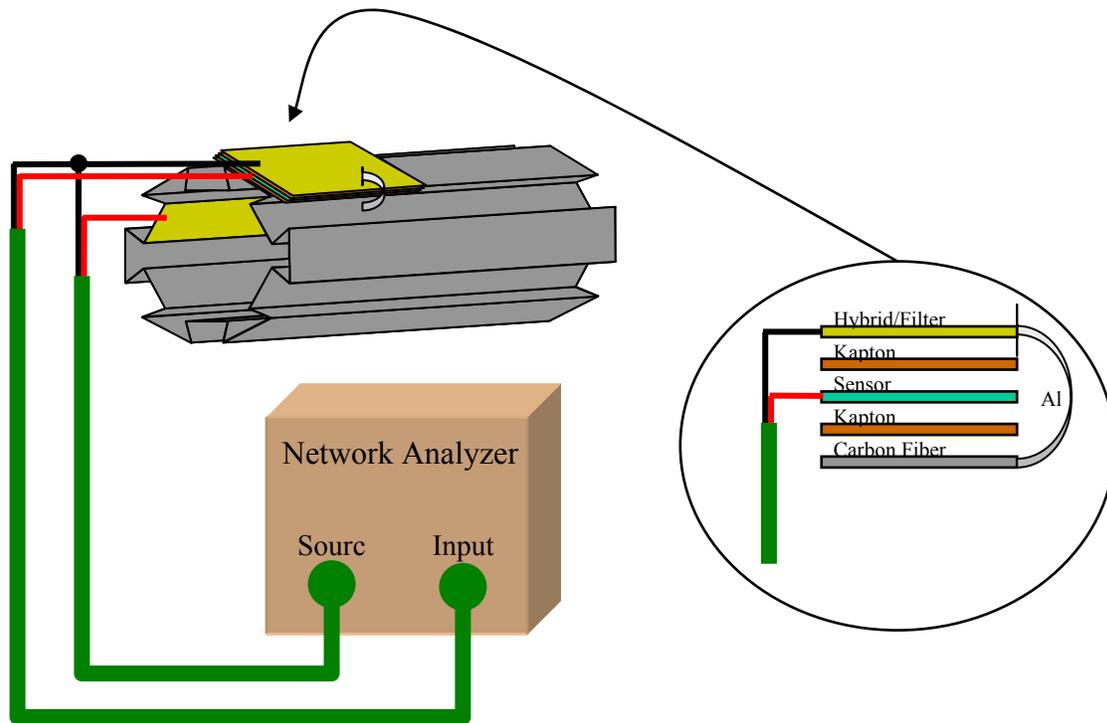


Figure 132. L0 Grounding test setup.

A more systematic test of the relation of attenuation to the coupling area to carbon fiber was performed using a 36 in<sup>2</sup> parallel plate copper-carbon fiber capacitor. Figure 133 shows that increasing the area of copper tape coupling to the capacitor dramatically increased the attenuation up to a saturation point of about 4 in<sup>2</sup>.

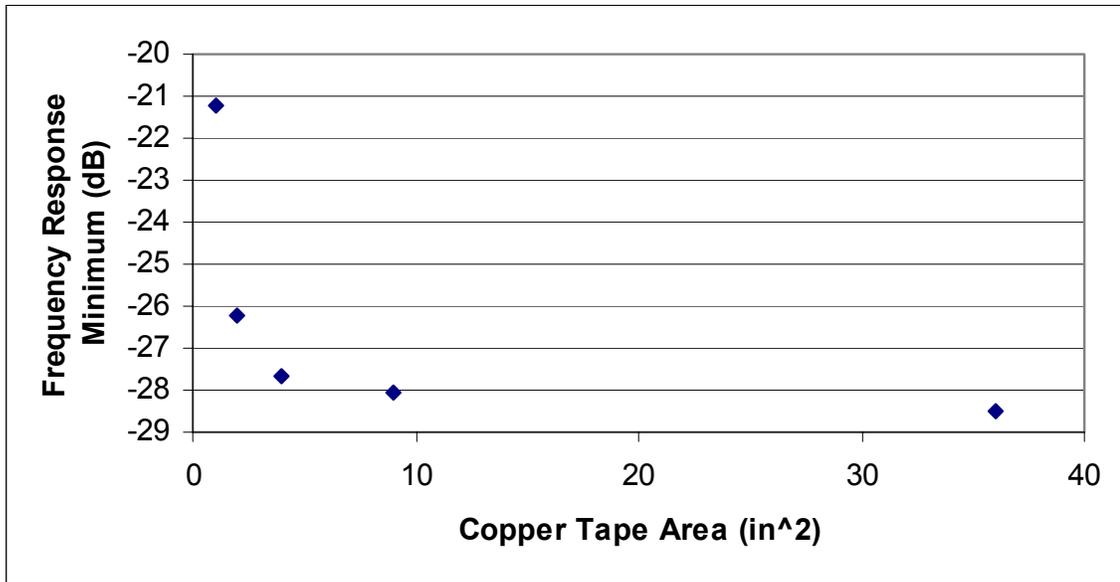


Figure 133. Attenuation at 74 MHz as a function of coupling contact area.

Because copper tape coupling would be unfeasible in the detector, a coupling test was carried out using carbon fiber pieces with embedded aluminum foil and aluminized Mylar. A new sensor/hybrid mockup was built and mounted on different pieces of K13C carbon fiber with various amounts of surface area covered with embedded aluminum. The embedded aluminum extends out to grounding strips that fold over and attach to the hybrid/filter plane. A diagram of this setup is given in Figure 134. The coupling point on the actual planes will be 2 mm wide ground pads.

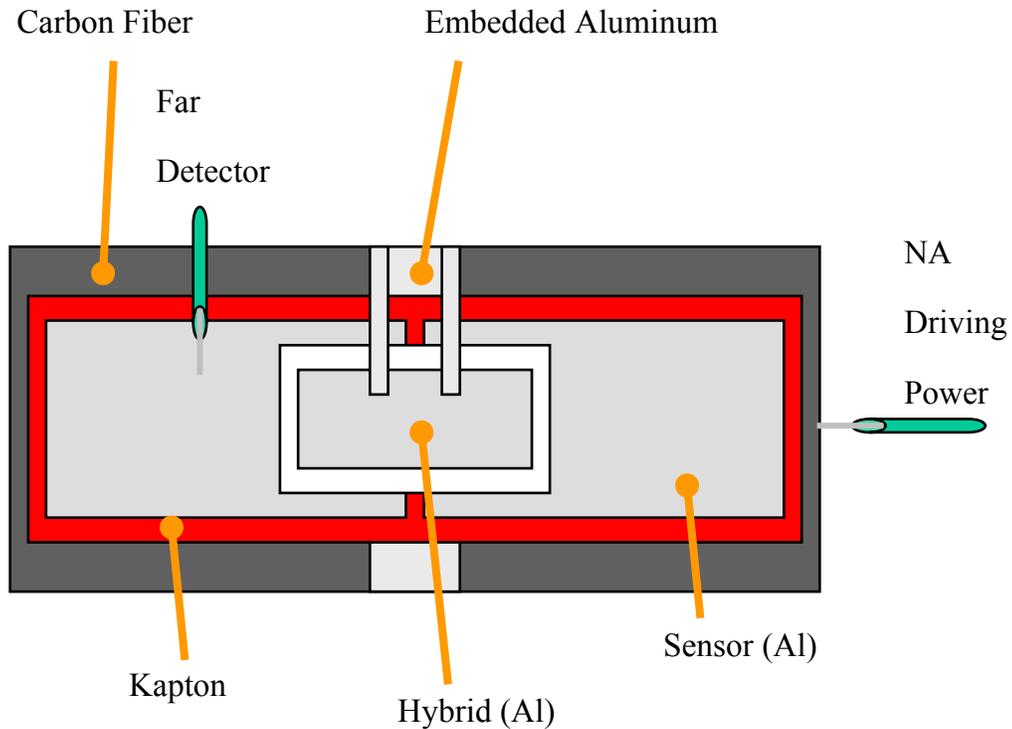


Figure 134. Embedded aluminum coupling contact test setup.

Aluminized Mylar grounding produced significantly less attenuation than aluminum; about 10 dB less below 20 MHz. This test also verified that the attenuation is not affected by the size of the grounding strips. Measurements of transfer functions were taken with different areas of embedded aluminum and equal sized grounding strips. Those data confirmed that the attenuation increases with contact area to the carbon fiber. The maximum area of embedded aluminum tested was 4 in<sup>2</sup>, giving a power decrease of at least 30 dB for all frequencies below 50 MHz. Coupling to carbon fiber through embedded aluminum has thus been shown to be an effective grounding technique, although the optimum area of embedded aluminum is yet to be determined.

## 6 PRODUCTION AND TESTING

### 6.1 Overview

This section describes the full chain of testing of the individual components needed to build silicon readout modules and the assembly of the components into modules and staves. The building and testing sequence is described, starting from individual components, resulting in fully certified staves. It relies on the successful production and testing effort DØ organized during the construction of the Run IIa Silicon Microstrip Tracker.

The essential building blocks of a detector module are the silicon sensors, the SVX4 readout chips, and the readout hybrids. Each component is tested as described below before it is assembled into a module. After the assembly the modules are tested again before they are mounted on staves. A detailed description of the staff assembly and installation is included in Section 4.4. Testing of staves and of the full readout system are also included below.

The basic production and testing sequence is the following:

1. SVX4 chips are tested as described in Section 5
2. Bare hybrids are tested for continuity and shorts by the manufacturer
3. 100% (5-10%) of bare preproduction (production) hybrids are re-tested
4. SVX4 chips and passive components are surface mounted on the hybrids
5. Fully assembled hybrids undergo an initial functionality test
6. Hybrids that pass the functionality test are burned-in at Fermilab
7. Sensors are produced and tested at the manufacturer
8. 100% (5-10%) of the preproduction (production) sensors are re-tested
9. Sensors and burned-in hybrids are assembled into a detector module.
10. Detector modules undergo initial functionality test at Fermilab
11. Detector modules that pass the functionality test are burned-in at Fermilab
12. 5-10% of burned-in detector modules are subject to more detailed QA tests
13. Burned-in modules are assembled into staves (L2-L5) or mounted on support structure (L0-L1)
14. Up to 6 detector modules are read out simultaneously

Each of the steps in the testing procedure is described in detail below.