



Run 2B Silicon Electronics

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WBS 1.1.2

- Overview
- SVX4 chip
- Analog flex cable
- Hybrids/ L1 module
- Interfacing to Run 2A readout
- Summary



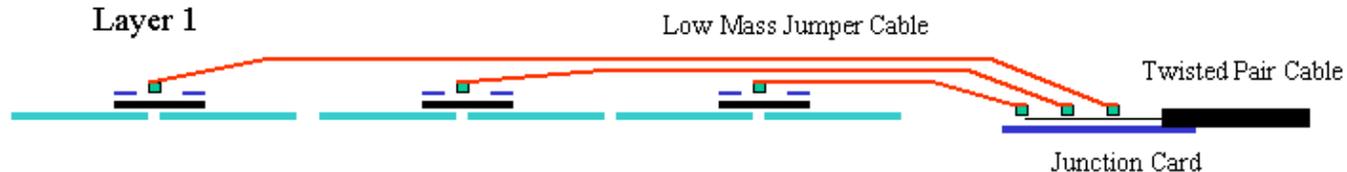
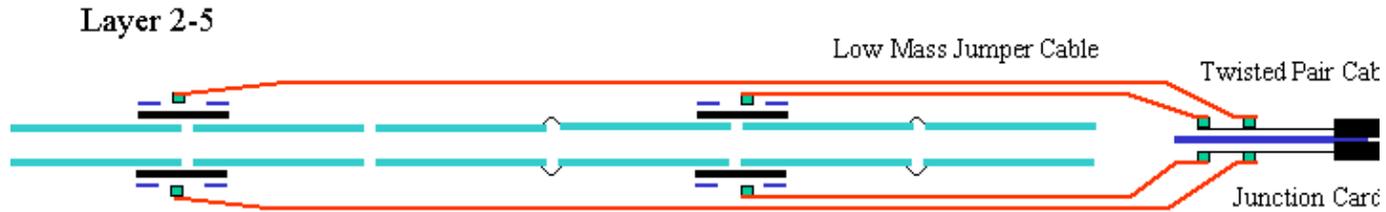
Readout

- Run2B Silicon readout is based on
 - ◆ new SVX4 chip
 - ◆ Run 2A readout with minimal modifications
 - ◆ Conservative, low risk solutions with minimum R&D
- Baseline established in September 2001
 - ◆ Went through several reviews
 - ◆ Steady progress last months
 - ◆ Conceptual design stage evolved to detailed design & prototyping stage
- In the following will concentrate on latest developments
 - ◆ Up to date documentation

<http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/readout/readout.html>



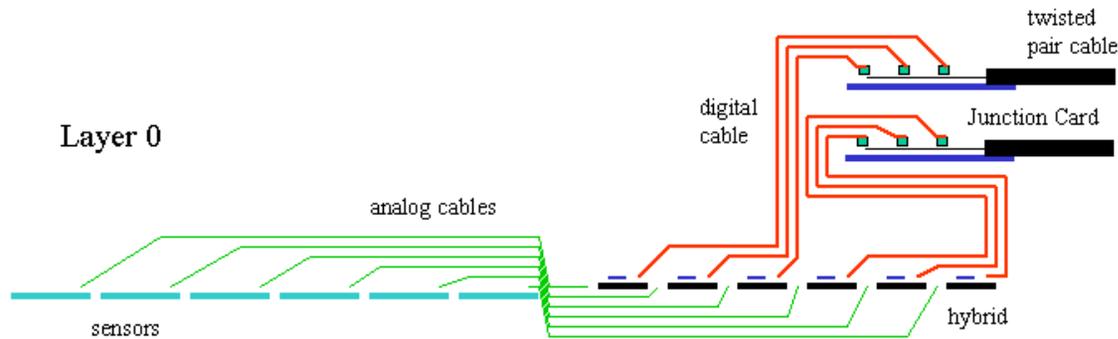
Layers 1 - 5 Readout



- On-board double-ended beryllia hybrid
- Reduction of readout cables is achieved by
 - Analog ganging : connected strips in L2-5
 - Digital ganging : chips bonded to different sensors are daisy chained on hybrid in L1-5
- Low mass digital flex (jumper) cable with connectors on both sides



Layer 0 Readout

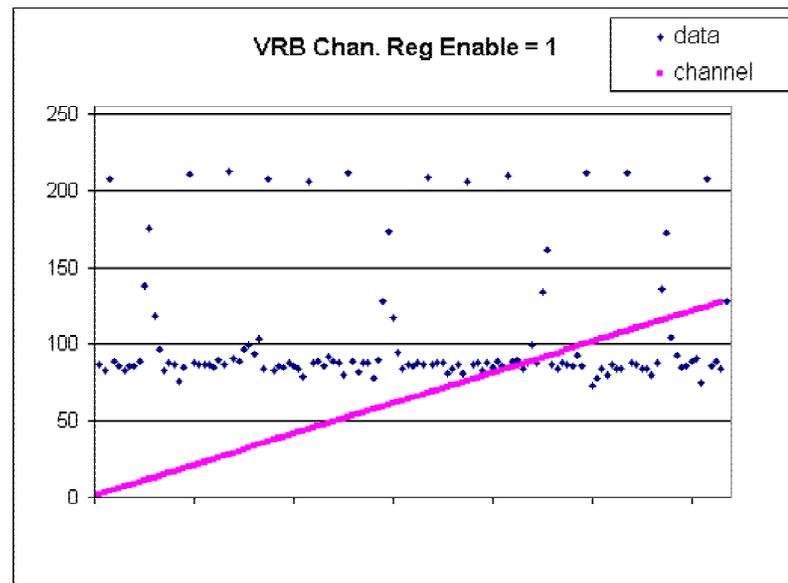


- small radius & minimal material => flex analog cables
- flex length is equalized
- two-chip hybrids, no ganging
- beyond hybrid : identical to L1
- challenging :
 - noise performance
 - manufacturing and assembly



SVX4 Chip

- New chip : SVX4
 - ◆ Designed by Fermilab/LBL/Padua
 - ◆ 0.25 μm technology, intrinsically radiation hard
 - ◆ Based on SVX3, compatible with SVX2
 - ◆ Several new schematics solutions
 - ◆ D0 will use differential readout
 - ▲ Use the same pad ring as CDF
- D0 DAQ can operate with SVX3 chips
 - ◆ D0 DAQ was designed for SVX2
 - ◆ Some remapping of control signals is required
 - ◆ Tested in Nov 2000, one SVX3 chip was read out with D0 Sequencer

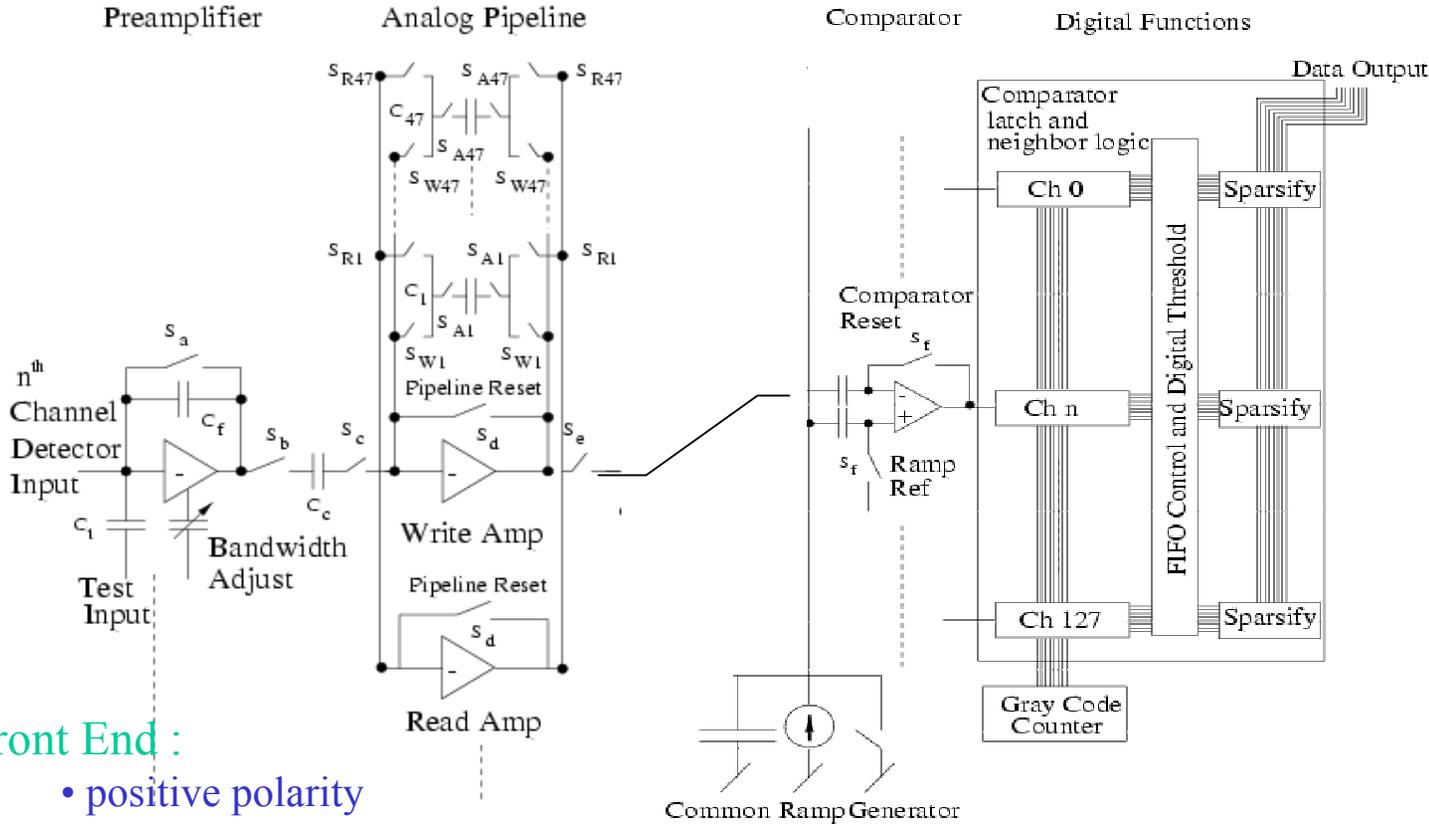


SVX3 Address & Data, 128 channels





SVX4 Chip



Front End :

- positive polarity
- gain 3 mV/fC, 5% uniformity
- load 10 – 40 pF
- risetime 60-100 nsec
- dynamic range 200 fC
- ‘black hole’ clumping
- reset time 200 nsec
- pipeline 42 cells

Back End :

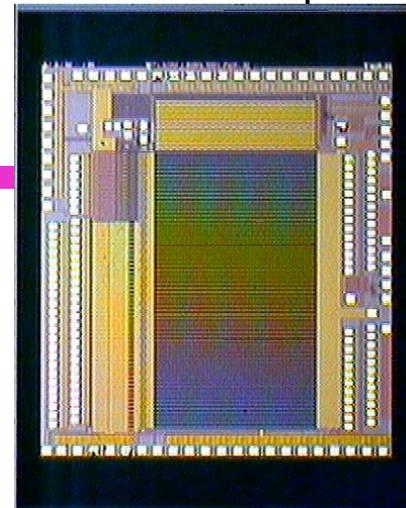
- Wilkinson ADC, 106 MHz counter
- dynamic pedestal subtraction
- data sparsification
- neighbor logic
- differential output drivers upto 17 mA
- configuration register



SVX4 Chip

- Front End design completed in June 2001
 - ◆ FE test chip tested in September 2001
 - ◆ Optimum preamp ENC = $450e + 43.0e/pF$
 - ◆ Pipeline validated
 - ◆ Excellent radiation hardness
- Full chip layout and simulation completed in March 2002
 - ◆ Two versions for prototyping
 - ▲ Conservative
 - ▲ On-chip bypassing of analog voltage
 - ◆ Chip dimensions 9.17 mm x 6.42 mm, power < 0.5W/chip
 - ◆ Chips back from TSMC on June 10th, DO share is ~250 chips of each version

FE test chip



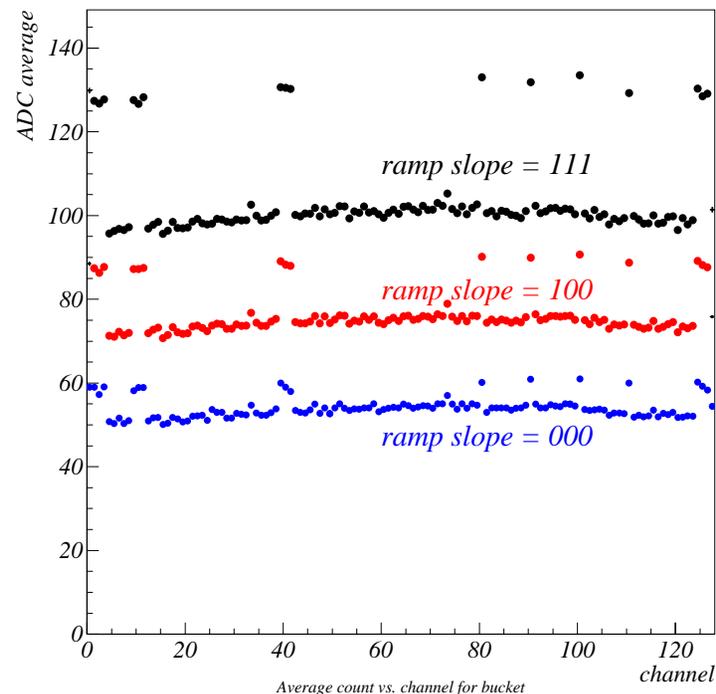
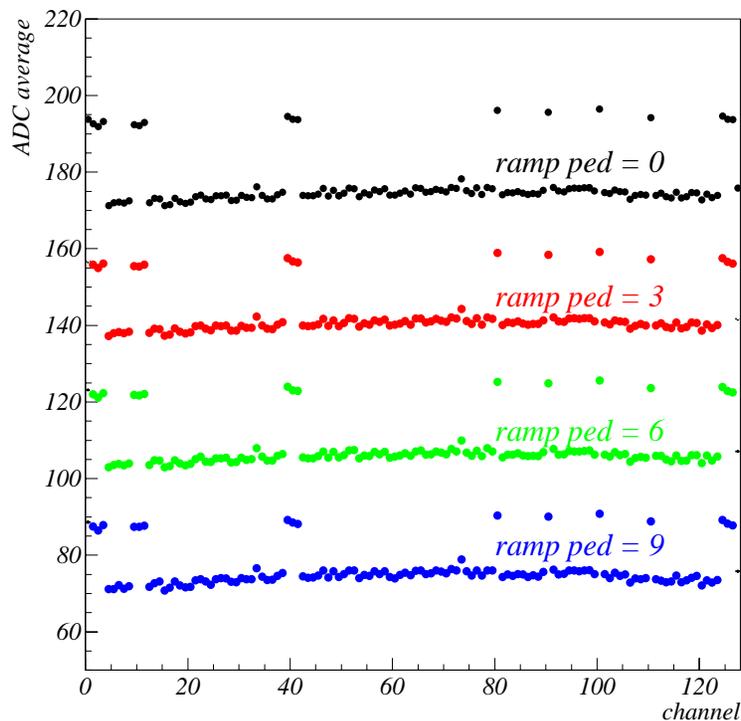
SVX4 on chip carrier





SVX4 Chip

- Prototype chip works both in CDF and D0 modes!
 - ◆ Major success : open up ways to test downstream electronics
- Joint test effort of CDF & D0 underway at LBL and Fermilab
 - ◆ Important to test prototypes as extensively as possible to minimize extra submissions





SVX4 Chip

- **Noise performance**

- ▲ ENC = 300e + 41e/pF C (Fermilab)
- ▲ ENC = 600e + 32e/pF C (LBL)
- ▲ S/N L1 prototype : 20/1

- **Known problems:**

- ◆ Add pull-up to USESEU
- ◆ Add pullup or pulldown to DØ-mode
- ◆ Pull MSB of ChipID high.
- ◆ Pedestal uniformity
- ◆ Logic changes to FECLK gating/ADC control/FE control in DØ-mode

- **Tests to do**

- ◆ Frequency & duty cycle margin
- ◆ Systematic test of all SVX4 specifications
- ◆ Power consumption in various modes
- ◆ SVX4 with silicon - black hole clamping feature, behaviour with various cables

- **Radiation hardness tests**

- ◆ SEU study at UC Davis. preliminary : OK after 10 Mrad, problems after 15 Mrad
- ◆ ⁶⁰Co gamma irradiation in Sacramento : Sept 02
- ◆ 14 MeV proton irradiation of L1 hybrid at KSU : Sept 02

	Parameter	Spec	Met
Preamp	Gain	3mV/fC	✓
	Gain Unif.	< 5%	✓
	Risetime	60-100 ns	✓
	Rise adjust.	4 bits	✓
	Noise	2000e @ 40pF	✓
	Dyn. range	> 200 fC	✓
	Cal inject		✓
Pipeline	Reset time	< 20ns	✓
	Ped. Uniformity	<500e	
	Linearity	<0.25%	✓
	Diff. non-lin.	<0.5 LSB	
Output	Risetime	2ns - 4ns	✓
	Bus	bi-directional	✓
	Priorities In-Out		✓
Regstr/Cntn	Cells	SEU tolerant	
	Bit assignments		✓
	Resets		✓
	ch. 63 latch		✓
	D0 mode		



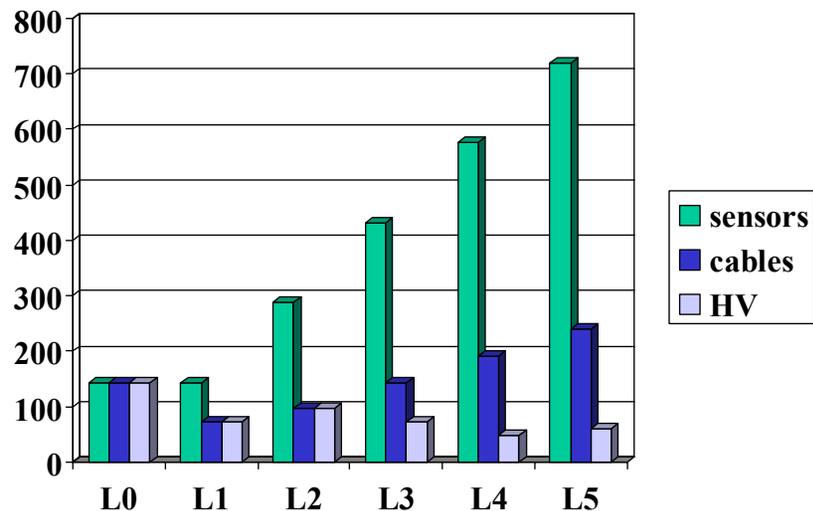
Cable Count

Layer SVX4/Hybrid # readout # HV cables
cables

Layer	SVX4/Hybrid	# readout cables	# HV cables
0	2	144	144
1	6	72	72
2	10	96	96
3	10	144	72
4	10	192	48
5	10	240	60

all layers 888 492

Run 2A 912 440 +

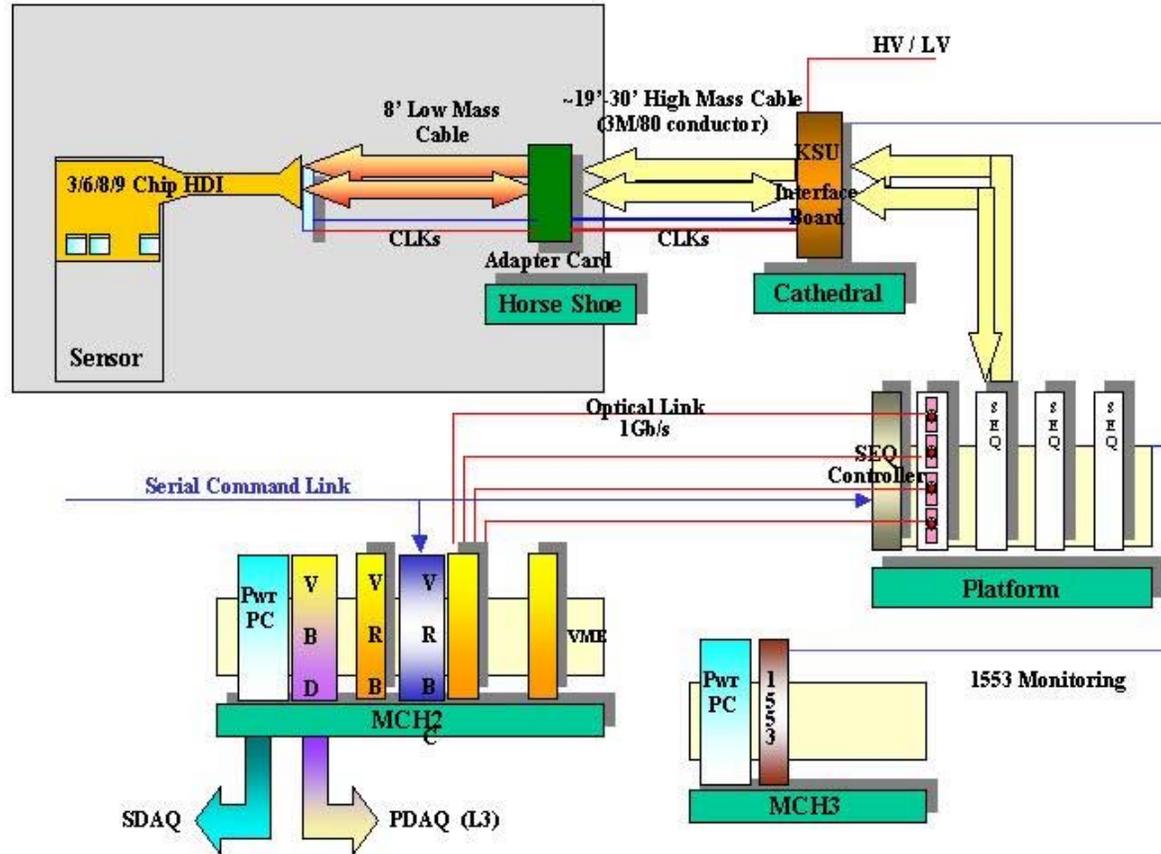


of sensors and cables per layer

Run 2B readout cable count is smaller than Run 2A cable count



Changes of Run 2A Readout



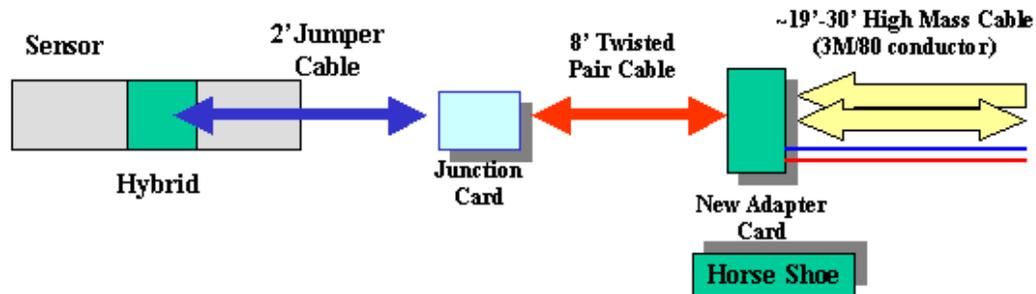
Modifications

- Signal level translation 5 V - 2.5 V
- Tight spec on 2.5 V (2.25 - 2.75 V) => Voltage regulation
- Mapping between SVX4 and SVX2
- Differential / Single-Ended translation
- Some changes in LV / HV power supplies, Interface Crates



Run 2B Readout

- One hybrid is an independent unit
 - ◆ Separate cable up to an accessible region
 - ▲ Same as in Run2A, proven to be successful during Run 2A commissioning
 - ◆ Minimizes readout time
 - ◆ Simpler testing and stave construction
 - ◆ High reliability, less interference between hybrids

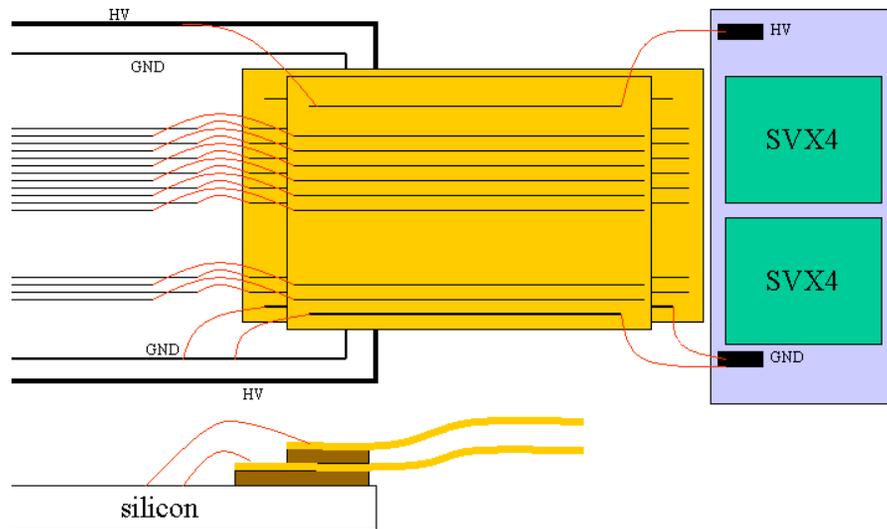


- Jumper Cable - Junction Card - Twisted Pair Cable - Adapter Card
- New Adapter Card is active, implements necessary modifications
- Junction Cards are located in an accessible area
- Twisted Pair Cable is well suited for differential SVX4 readout



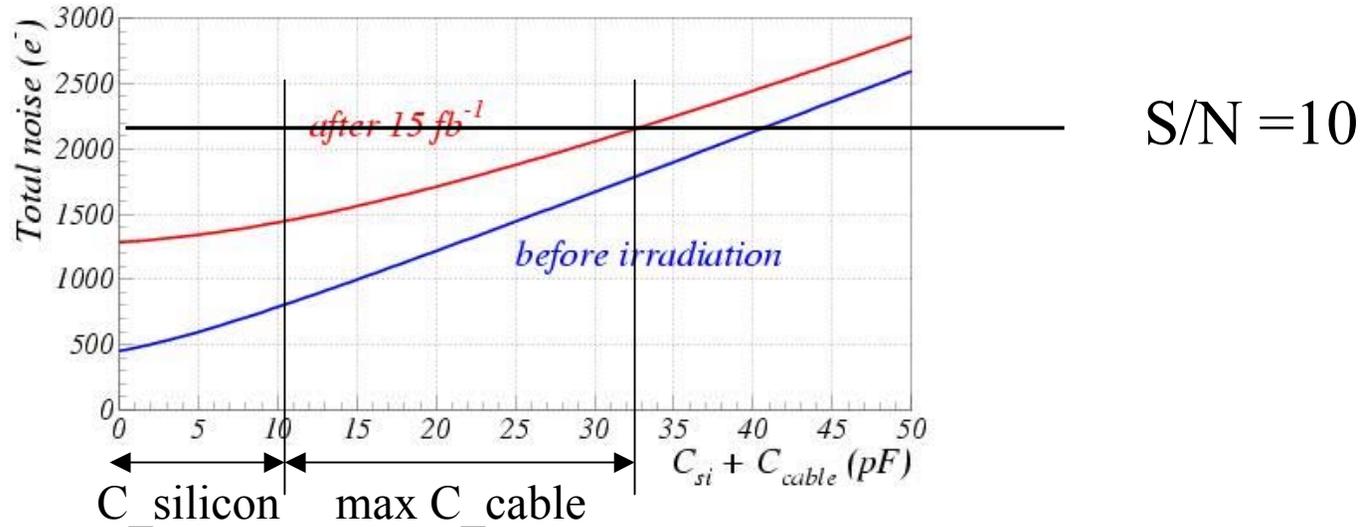
Analog Flex Cables

- Low mass, fine pitch cables for Layer 0
 - ◆ Trace width 15-20 μm
 - ◆ Constant 100 μm pitch without fan-out region
 - ◆ Two cables shifted by 50 μm , effective pitch 50 μm matches sensor pitch





LO noise performance



Acceptable cable capacitance is determined by noise performance

$S/N = 10$ after $15 \text{ fb}^{-1} \Rightarrow C_{\text{cable}} < 0.55 \text{ pF/cm}$ for 42 cm long cable
typical $C_{\text{silicon}} \sim 1.2 \text{ pF/cm}$



Analog Flex Cables

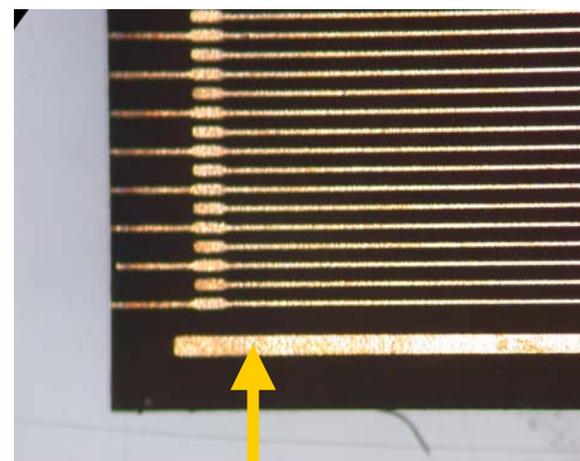
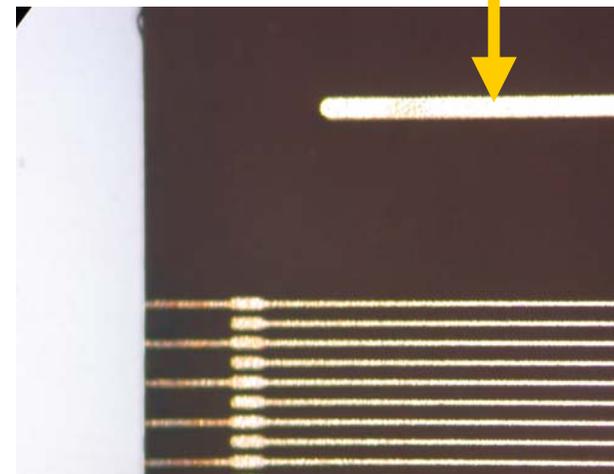
- **Dyconex**

- ◆ Designed by Fermilab, Universitaet Zuerich
- ◆ Second prototype run
 - ▲ pitch 91 μm , trace width 16 μm
 - ▲ Used regular etching technology
 - ▲ March 2002 : 15 mechanical grade cables + 12 good cables
 - ▲ July 2002 : 27 good cables
- ◆ Results on 39 prototype cables:
 - ▲ Good quality of imaging
 - ▲ Allow one open trace out of 129

Open traces	0	1	2	>2
cables	22	13	4	0

- ▲ Measured trace width : 10-12 μm
- ▲ Capacitance, resistance measurements under way
 - Preliminary $C=0.35 \text{ pF/cm}$

HV trace

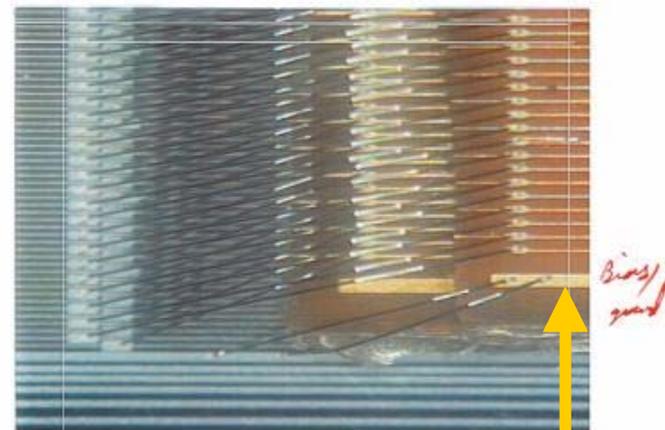
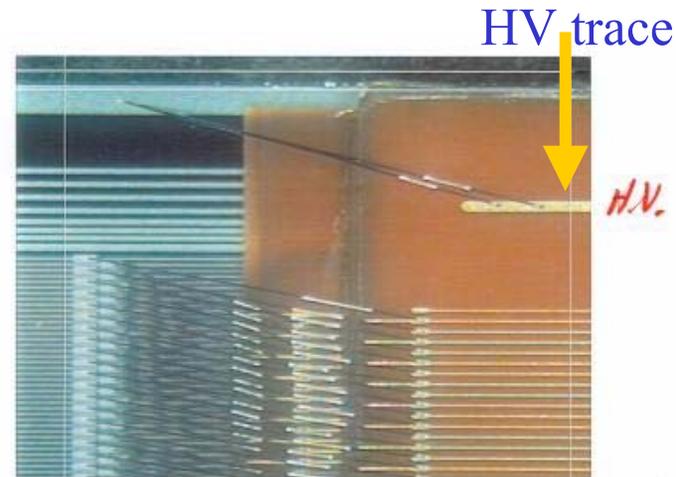


GND trace



LO module prototype

- Built LO module prototype in May 2002
 - ◆ Dyconex cables
 - ◆ ELMA LO sensor
 - ◆ Run2A HDI with 3 SVX2 chips
- Proof of principle
 - ◆ Simpler approach works
 - ◆ Developed handling & assembly procedures
- Measured
 - ◆ Noise $\sim 1900 e^-$ - agrees with SVX2 performance
 - ◆ Shielding geometry studies (next slide)
- Building new prototype with SVX4



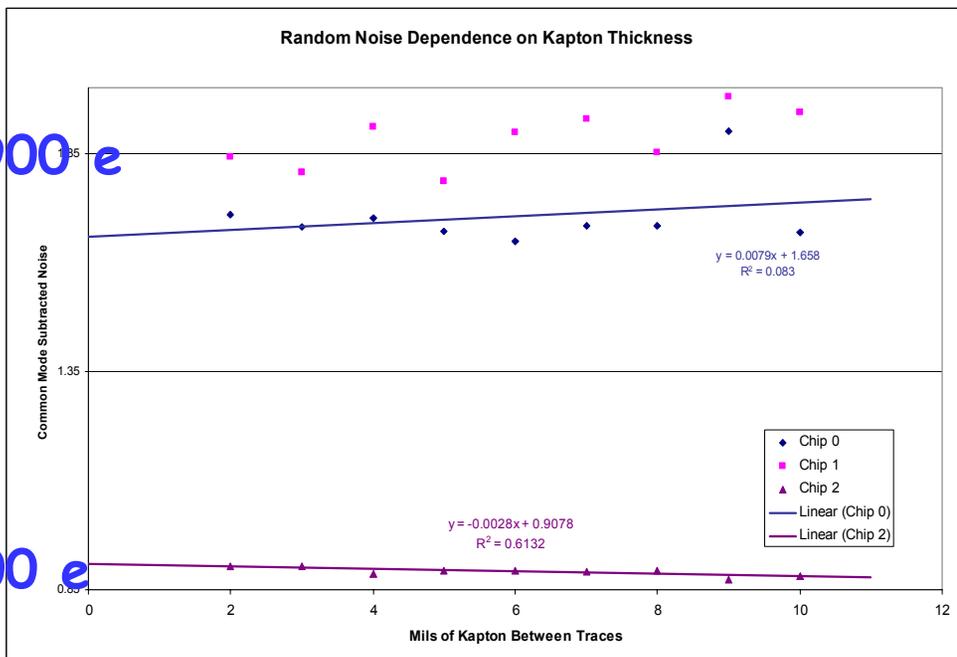
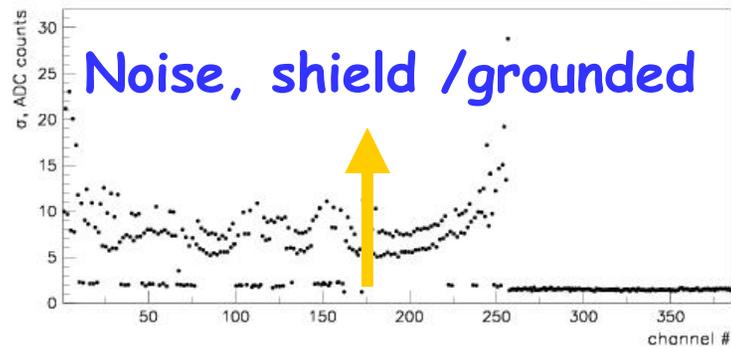
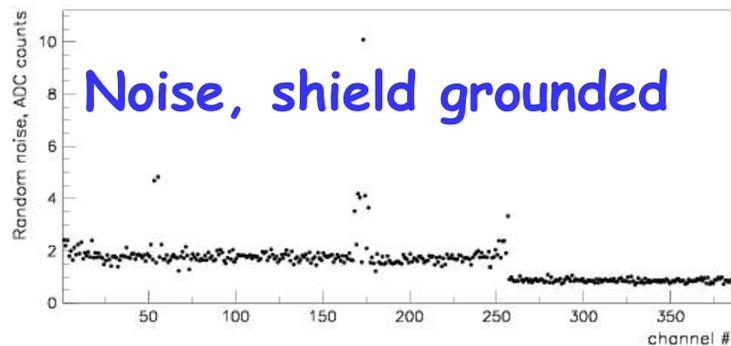
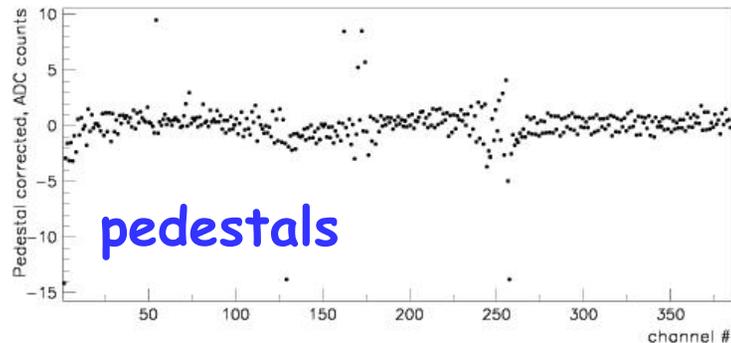
GND trace



Analog Flex Cables

Noise studies

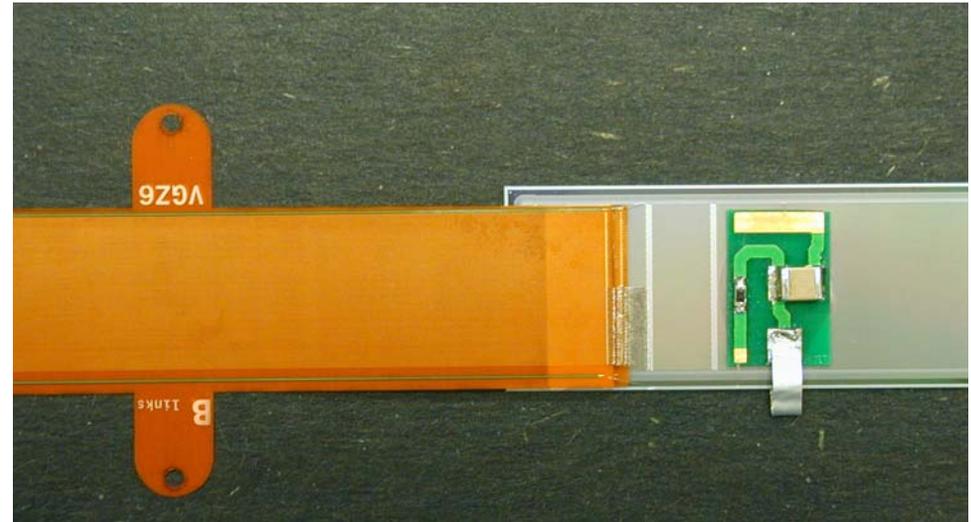
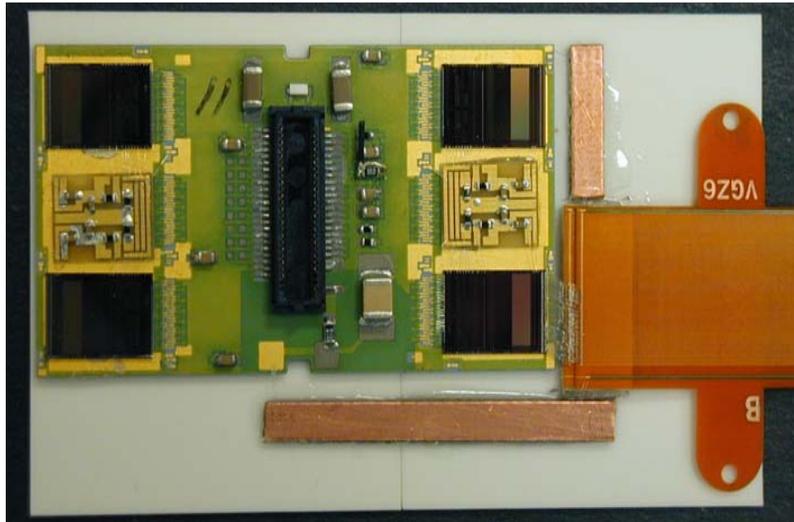
- ◆ Noise vs. two cables separation
- ◆ Shielding effects
- ◆ Noise vs. distance to shielding



Noise vs two cable separation

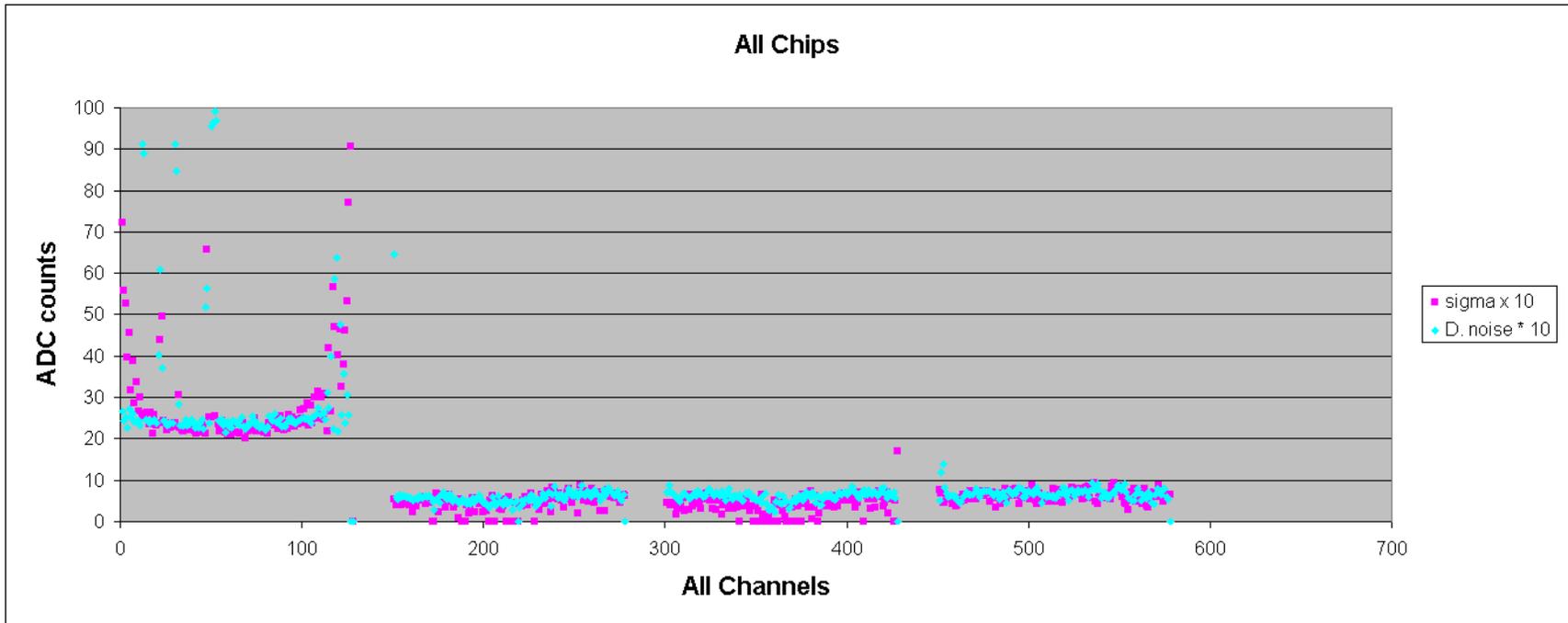
DO LO module prototype with SVX4

- First LO prototype with SVX4
 - ◆ ELMA LO sensor, two Dyconex 42.5 cm analog cables
 - ◆ L1 prototype hybrid
 - ◆ Verification of SVX4 performance
 - ▲ With large capacitive load
 - ▲ With long antenna on the input



DO L0 module prototype with SVX4

- Preliminary results
 - ◆ Noise ~ 2.3 ADC counts
 - ▲ Bare chip 0.7 counts





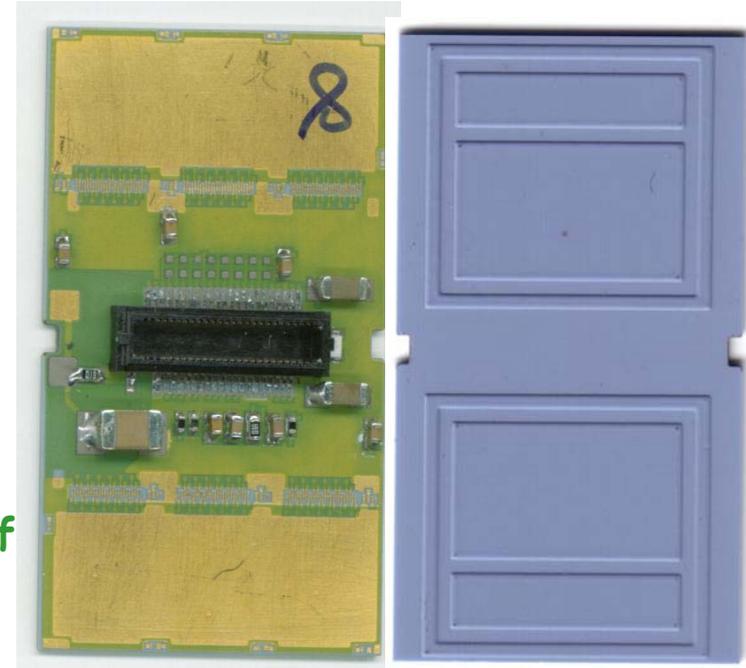
Hybrids

- Based on Beryllia ceramic
 - ◆ Minimize material, BeO thickness 0.38 mm
 - ◆ Good heat conductor
 - ◆ Established technique
- Multilayer structure on the substrate
 - ◆ six Au layers
 - ▲ GND & power planes, 4 um thick
 - ▲ Traces, 8 um thick, 100 um wide
 - ◆ five 40 um dielectric layers, total thickness 0.8 mm
 - ◆ Three technologies for vias in dielectric
 - ▲ Etching (Fodel dielectric), min via size 4 mils
 - ▲ Pattern diffusion, min via size 5 mils
 - ▲ Screen printing, min via size 8 mils
 - ◆ Screen printing is our baseline
 - ▲ Cost effective
 - ▲ More vendors capable to screen print on BeO
 - CPT, Oceanside CA - used by CDF
 - AMITRON, North Andover MA



Hybrids

- Four types of hybrids
 - ◆ Layer 0 : 2 chips
 - ◆ Layer 1 : 6 chips, double-ended
 - ◆ Layers 2-5 : 10 chips, double-ended
 - ▲ Axial
 - ▲ Stereo, different width, electrically identical to axial
- For all hybrids
 - ◆ ~10 mil spacing between vias
 - ◆ 50 pin AVX 5046 connector, 3 mm high
 - ▲ Allows for easy testing during all phases of production and assembly
 - ▲ Used by CDF for Run 2A SVX
 - ◆ bypass capacitors, termination resistors
 - ◆ temperature sensor
 - ◆ HV routed to side pin with 4 neighbors removed, tested to 1600 V
 - ◆ Reserved space ("nuts") for assembling purposes



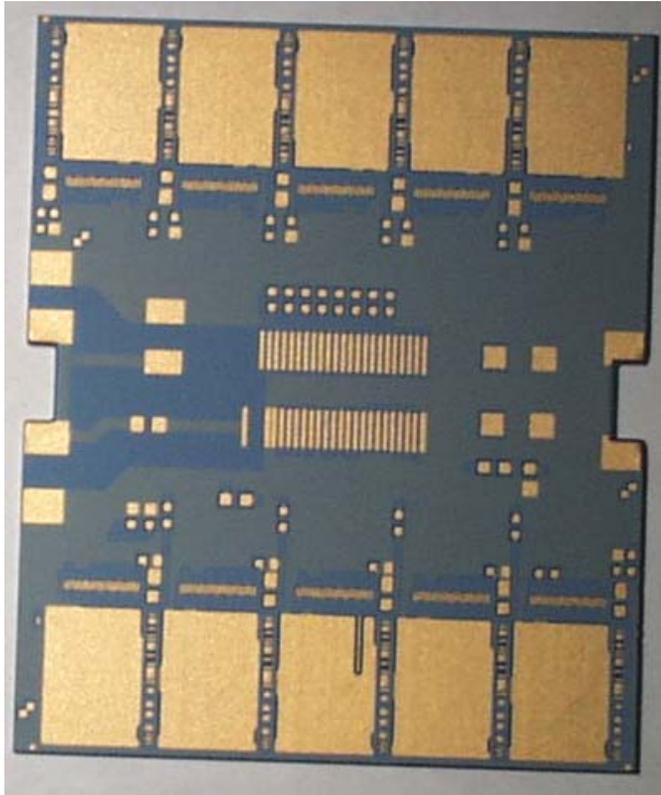
Layer 1 hybrid prototype



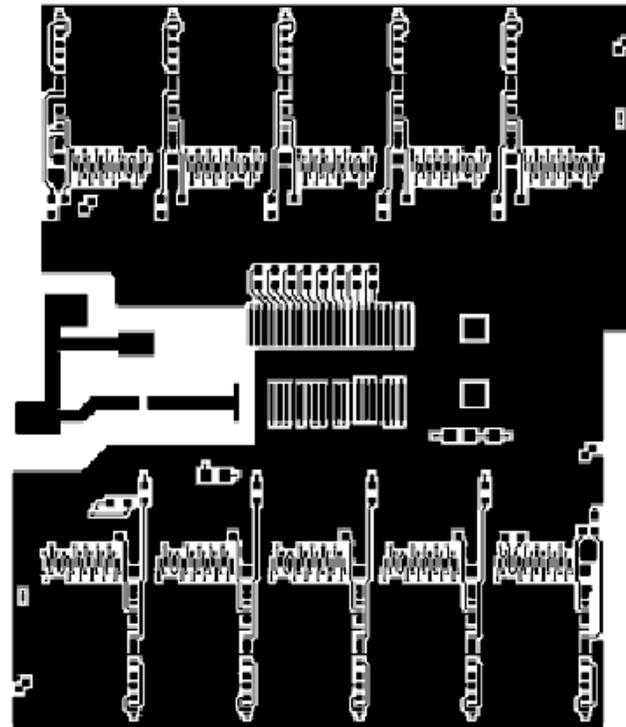
Hybrids

Layers 2-5 10-chip hybrids :

design similar to Layer 1 6-chip hybrid



L2-5 Axial hybrid, top layer
Prototype from Amitron

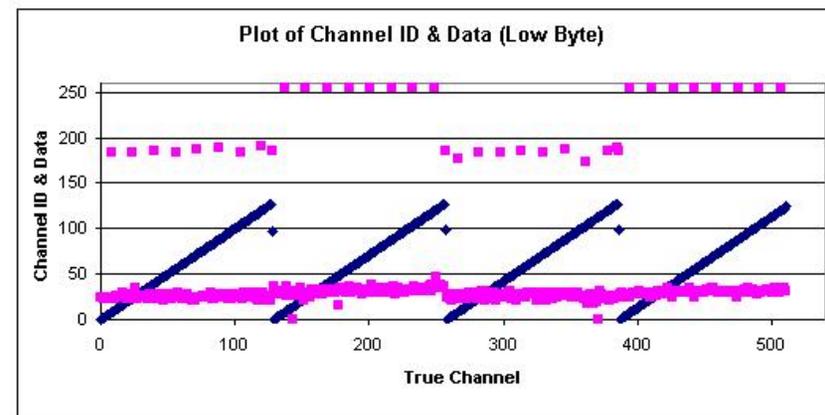
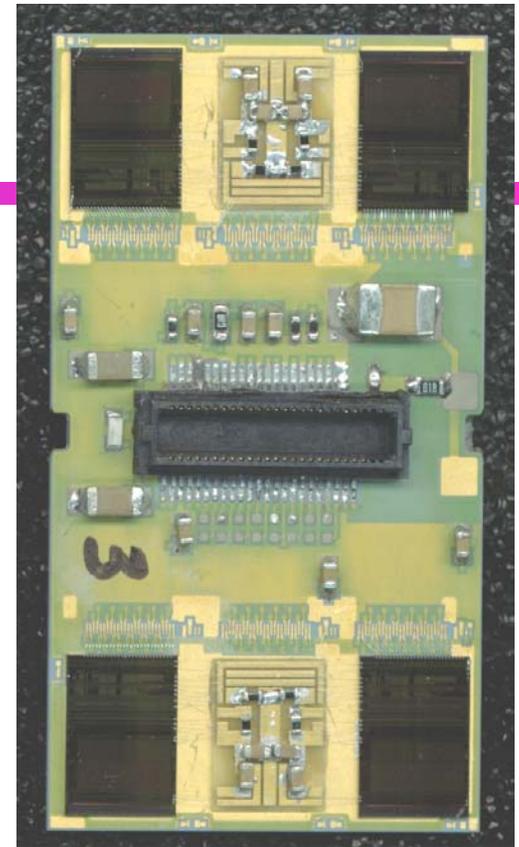


L2-5 stereo hybrid



Hybrids

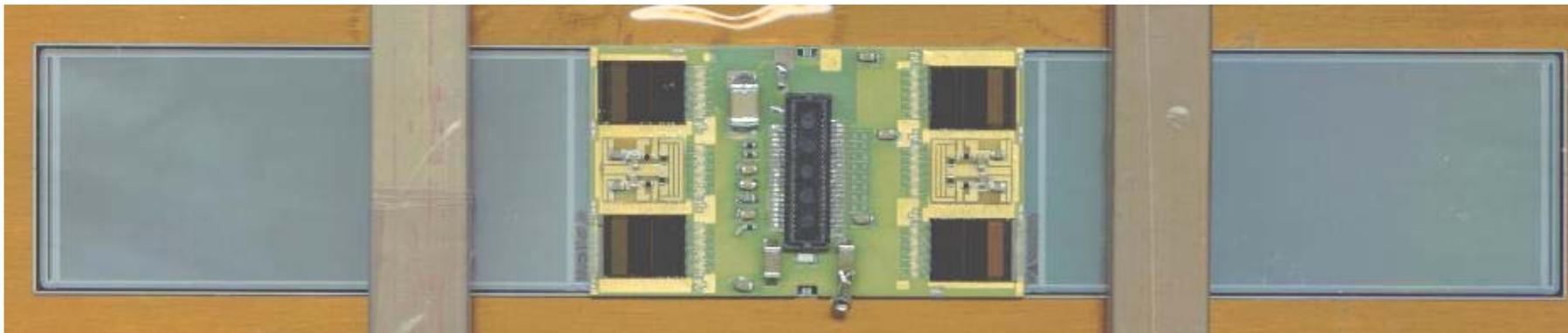
- L1 hybrid prototype
 - ◆ Designed by Fermilab
 - ◆ Received 18 hybrids from CPT in April
 - ◆ Mechanical (thickness, flatness, dimensions, gluing)
 - ▲ Flatness 30-60 um (spec 50 um)
 - ▲ Other dimensions OK
 - ◆ Electrical (done by U.Kansas, Fresno State U.)
 - ▲ 17 tested, no faults found
 - ◆ Stuffed 7 hybrids
 - ▲ 6 hybrids worked
 - ▲ Using burn-in stand hardware&software





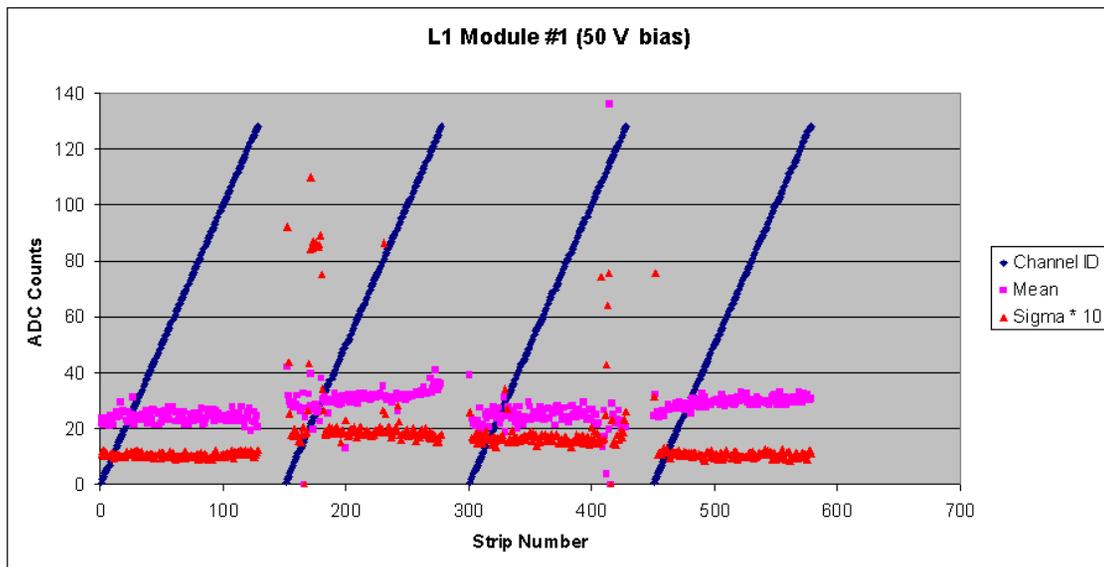
L1 module prototype

- L1 module prototype



08/05/2002

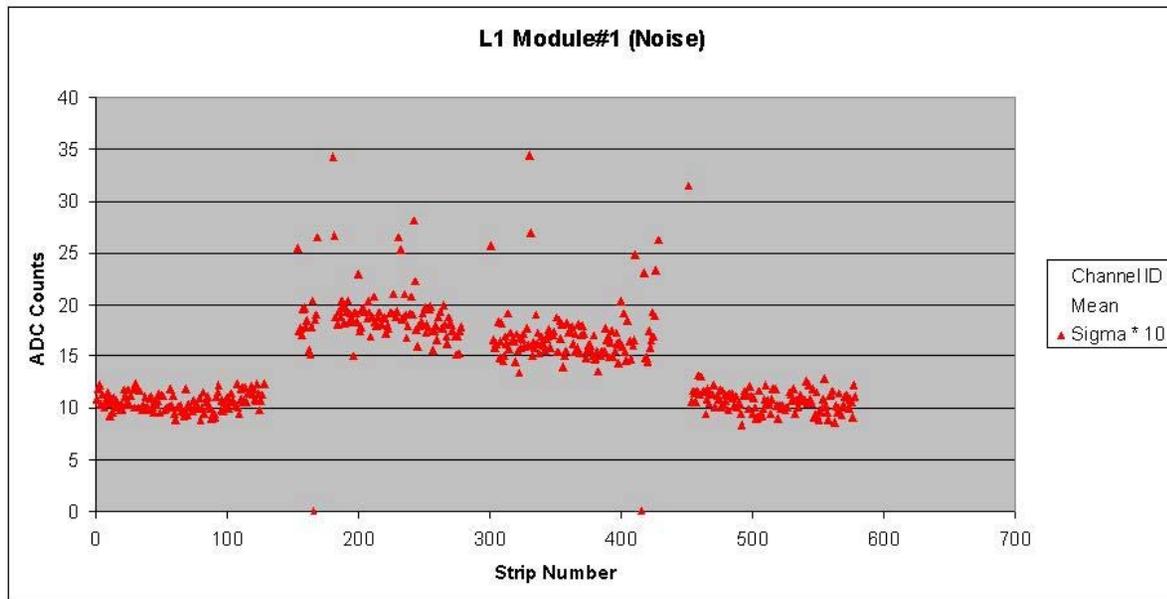
- ◆ Two L1 ELMA sensors
- ◆ L1 prototype hybrid





L1 module prototype

- Noise performance (preliminary)
 - ◆ Bare SVX4 : $\sim 700 e$
 - ◆ SVX4 bonded to sensor : $\sim 1000 e \Rightarrow S/N \sim 22/1$

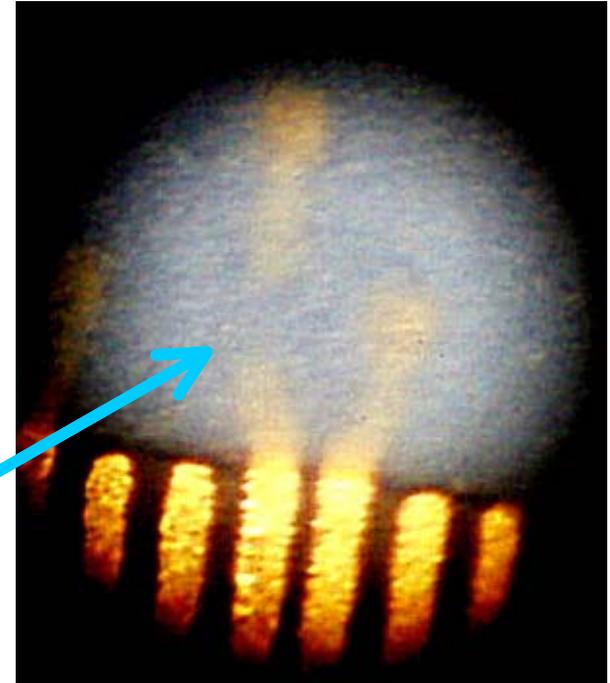


- L2A and L2S prototype hybrids
 - ◆ 25 L2A received from Amitron
 - ◆ 50 L2A and 50 L2S ordered from CTP (due 9/24/2002)



Hybrids

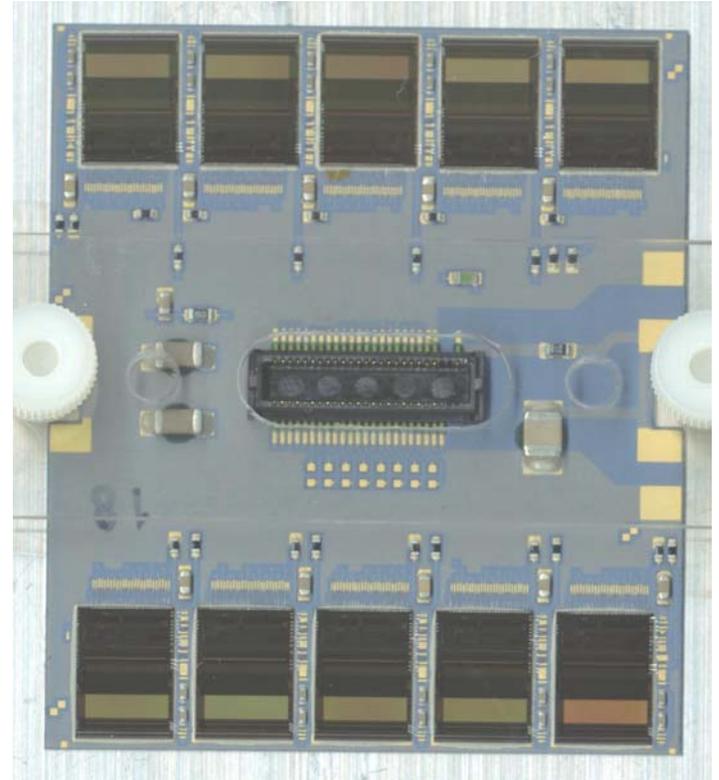
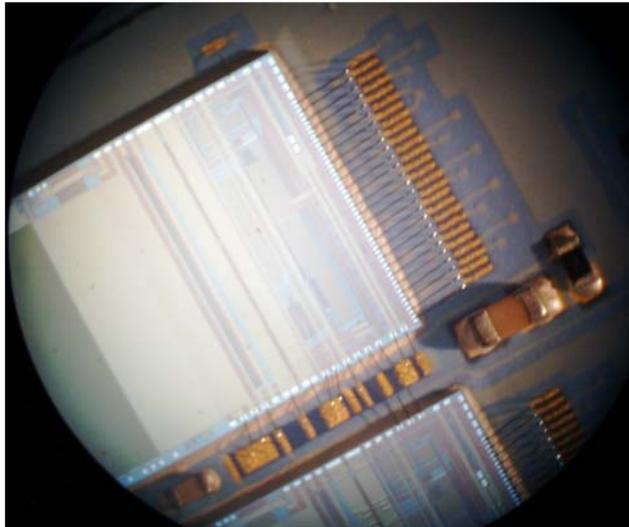
- L2A and L2s hybrid prototypes
 - ◆ Designed by Fermilab
 - ◆ Received 23 L2A hybrids from Amitron in August
 - ▲ Mechanical (thickness, flatness, dimensions, gluing)
 - Flatness ~150 um (spec 50 um)
 - Other dimensions OK
 - ▲ Electrical (done by U.Kansas, Fresno State U.)
 - 23 tested, 4 broken lines found
 - ▲ Stuffed 2 good hybrids at Meltronix
 - Encountered problem with soldering
 - Successfully bonded between chips : integrated finger design works ok
 - ◆ 50 L2A and 50 L2S from CPT ready in Sept-Oct 2002
- L0 hybrids ordered from CPT





Hybrid Assembly: Meltronix

- Two L2A hybrids assembled at Meltronix
 - ◆ Good workmanship
 - ◆ Used epoxy instead of solder
 - ◆ Bonding/stuffing in inter-chip area
 - ◆ Tests in progress

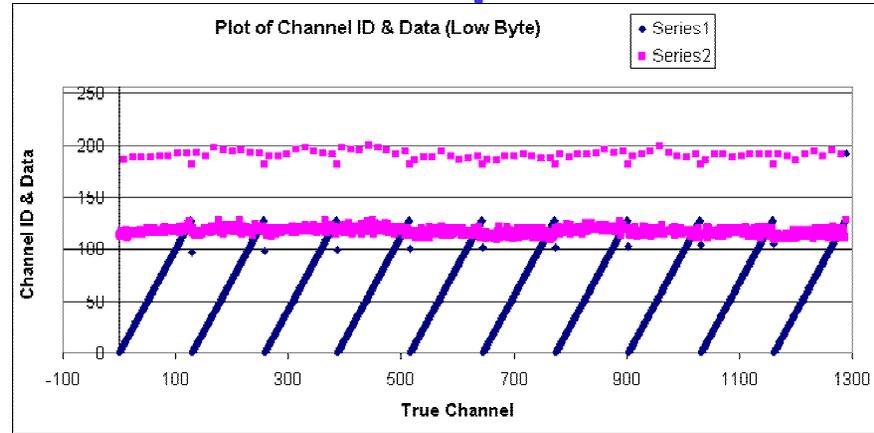




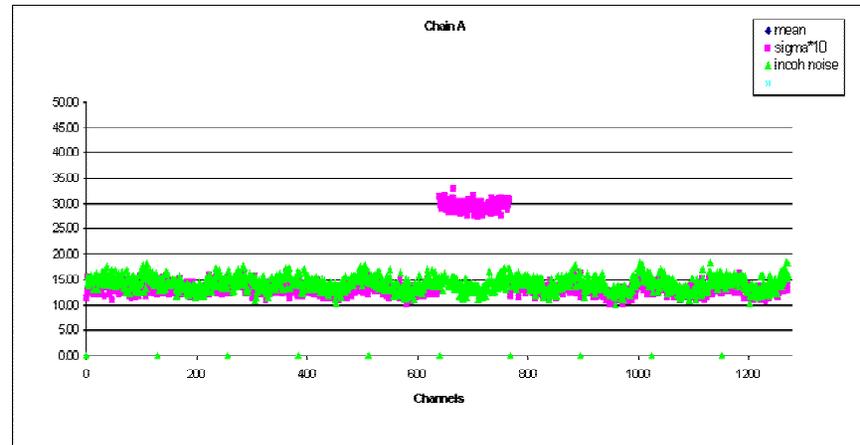
10-chip Hybrid

- Read out with Standalone Sequencer

◆ Calinjects



◆ Noise

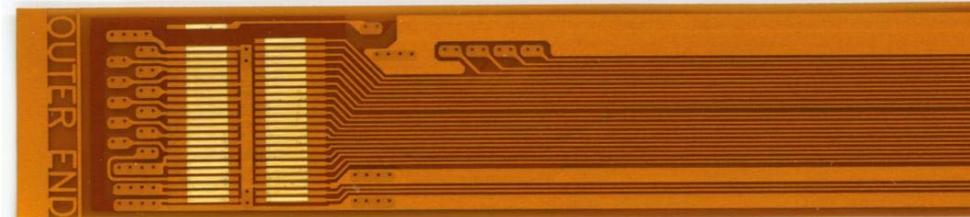
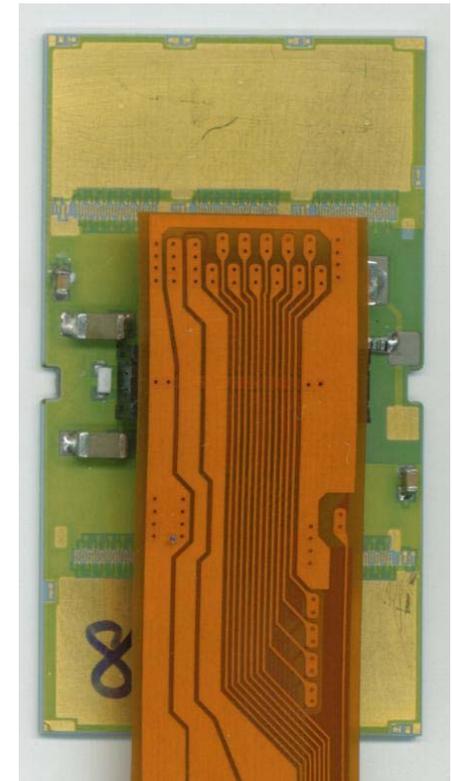




Digital Jumper Cable

Hybrid - **Jumper Cable** - Junction Card - Twisted Pair Cable – Adapter Card

- Designed by Kansas State
- Same design for all layers
 - 10-12 different lengths, max length ~ 1 m
 - Kapton substrate, total thickness 250 um for L0-1, 330 um for L2-5
 - HV on the same cable
 - AVX 50-pin connector on both sides
- Layout reviewed and prototypes ordered in January 2002
 - From Honeywell (Run2A low mass cables)
 - Back in March 2002
 - Electrical, mechanical tests OK
- Second vendor : Basic Electronics
 - Received 10 cables, tested OK





Junction Card

Hybrid - Jumper Cable - **Junction Card** - Twisted Pair Cable – Adapter Card

- L0-1 : 3 hybrids → junction card
- L2-5 : 2 hybrids → junction card
- 50-pin AVX connectors,
- Twisted pairs are soldered to JC, cards are extensions of cable bundles
- Dimensions 97 (70) mm x 25 mm
- Location : near present H-disks
- Designed by Kansas State
- Prototypes received in May 2002

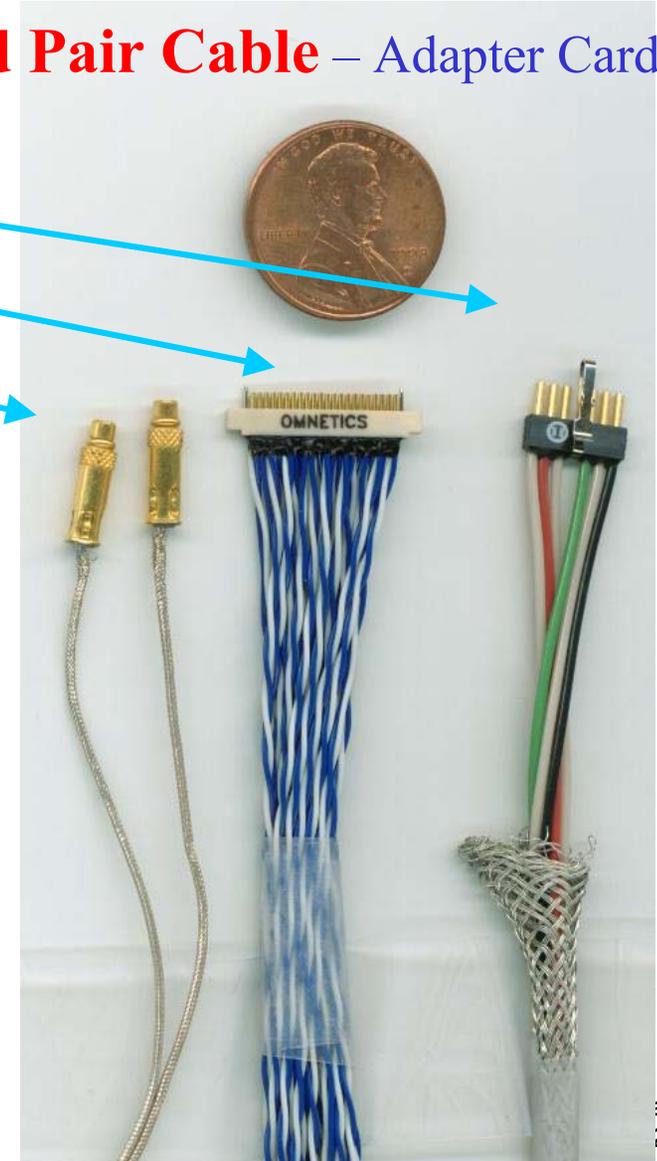




Twisted Pair Cable

Hybrid - Jumper Cable - Junction Card - **Twisted Pair Cable** – Adapter Card

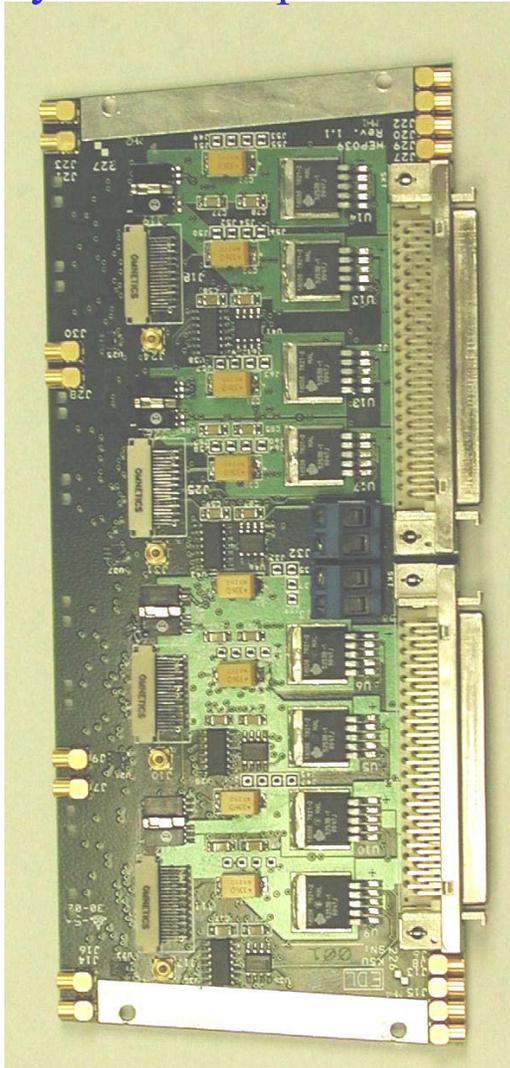
- Consists of
 - ◆ Power & HV lines : 6-pin Omnetics connector
 - ◆ Signal pairs : 44-pin Omnetics connector
 - ◆ Clock coaxes
- Designed by Fermilab
- All parts (connectors, pairs) received for prototype cables
- Prototypes ready





Adapter Card

Hybrid - Jumper Cable - Junction Card - Twisted Pair Cable – **Adapter Card**



- Adapter Card is active :
 - ◆ Two voltage regulators per hybrid: analog and digital voltages
 - ◆ Differential-to-Single-Ended 2.5-to-5 V translation for SVX4 Data
 - ◆ 5-to-2.5 V translation for SVX4 Controls
 - ◆ Routing of Clock and HV
- Four rings of Adapter Cards at two ends of calorimeter
- Designed by Kansas State
- Several iterations on design
- Prototypes ready

Top view of 4-channel Adapter Card



Interface Board & LV PS

- **Baseline** : retain Run 2A IB's, use in full functionality
 - ◆ Signal regeneration and termination
 - ◆ LV distribution
 - ◆ LV voltage/current monitoring
 - ◆ HV distribution for L2-5 (< 300 V)
 - ◆ Hybrid Enable/Disable
 - ◆ Hybrid temperature monitoring
 - ◆ Current & temperature protection
- Will need small modifications of IB inputs (terminations)
- **Note**: Present IB fixes several SVX2 "features"
 - ◆ Assumption : SVX4 will not have new "features" which cannot be recovered with present IB
- **LV power supplies**
 - ◆ Run2A supplies behave OK and are adequate : keep them
 - ◆ Working on mapping
 - ◆ New IB backplane for power & HV distribution



High Voltage

- Current caused by radiation damage

- ◆ Assume 15 fb-1, L0 @ -10 C, L1 @ -5 C, L2-5 @ 0 C

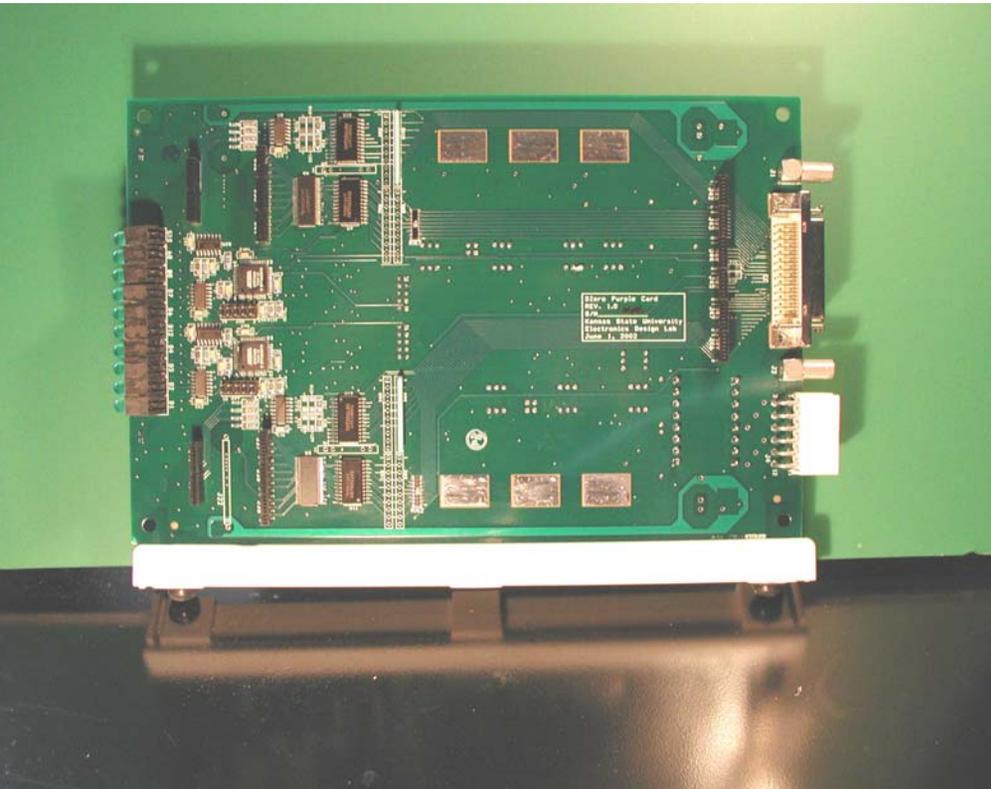
Layer	uA/strip	uA/hybrid	uA/stave	Hybrids/ HVchannel
0A	0.21	107	na	1
1A	0.13	200	na	1
2A	0.28	717	2151	1
3A	0.12	307	921	2
4A	0.07	179	537	4
5A	0.05	128	384	4

- ◆ Max current < 0.8 mA
- ◆ Total HV channel count of 492
- ◆ Will keep the present HV system : Bira 2000 V, 3.2 mA
- ◆ Currently have 10 crates, 440 HV channels (out of them 248 are positive)
- ◆ Will have 11 crates; 528 positive channels
 - ▲ Mexican collaborators (CINVESTAV) are buying the balance between Run2A and Run2B in 2002
- ◆ Will need partly new cable plant and distribution system



Production Test Stands

Hybrid - Jumper Cable - **Purple Card** - SASEQ



- ◆ Used for burn-in and test stands
- ◆ Designed by Kansas State
- ◆ Use same components and schematic solutions as Adapter Card
- ◆ One channel Purple Card + SASEq setup
 - ▲ Testing Hybrid + Jumper Cable
- ◆ Multi-channel Purple Card + SASEq setup
 - ▲ Max 6 channel setup - LO sector
 - ▲ Testing collective effects in modules and Jumper Cables
 - Groundings
 - Digital and analog crosstalk, data integrity

Top view of 2-channel Purple Card



Vertical slice tests

1. Hybrid - Jumper Cable - Purple card - Sequencer
 - ◆ Same as setup with SASeq.
 - ◆ Developing of firmware for Sequencers
2. Hybrid - Jumper Cable - Junction Card - Twisted Pair Cable - Adapter Card - 80-conductor cable - Interface Board - 50-conductor cable - Sequencer
 - ◆ Testing of performance for all components - anticipate most of the time will be spent here
 - ▲ Timing studies, verification of terminations, impedance matching etc.
3. Multi-channel readout test
 - ◆ Can have up to 10 boards of each type (80 readout channels), limited by the amount of spares
 - ◆ Data integrity, collective effects tests
4. Tests of Low Voltage Power Supplies
 - ◆ New backplane in IB crate
 - ◆ Need simulate full load on supply



Status

Component	Vendor	Design	First Prototype		Second Prototype		Final Order
			Ordered	Delivered	Ordered	Delivered	
SVX4	TSCM	✓	✓	✓			
Analogue Cable	Dycx	✓	✓	✓	✓	✓	
	Comp	✓	✓				
L0 Hybrid		✓					
L1 Hybrid		✓	✓	✓			
L2A Hybrid		✓	✓	✓			
L2S Hybrid		✓	✓				
Digital Cable	Honey	✓	✓	✓			
	Basic	✓	✓	✓			
Junction Card		✓	✓	✓			
Twisted Pr. Cable		✓	✓	✓			
Adapter Card		✓	✓	✓			
Test Stand Elctr.		✓	✓	✓			
High Voltage		✓	✓				



Summary

- Established a baseline for Run 2B Silicon Readout
- Good group of people (Zurich, UIC, NWU, LATech, KU, KSU, Fresno, Fermilab)
- Detailed design exist for (almost) all components
- Excellent progress last months
 - ◆ SVX4 works in D0 mode
 - ◆ L1 hybrid prototype works
 - ◆ L1 module prototype works
 - ◆ All prototype components for full readout chain test in hand
- Current focus on SVX4 and vertical slice tests