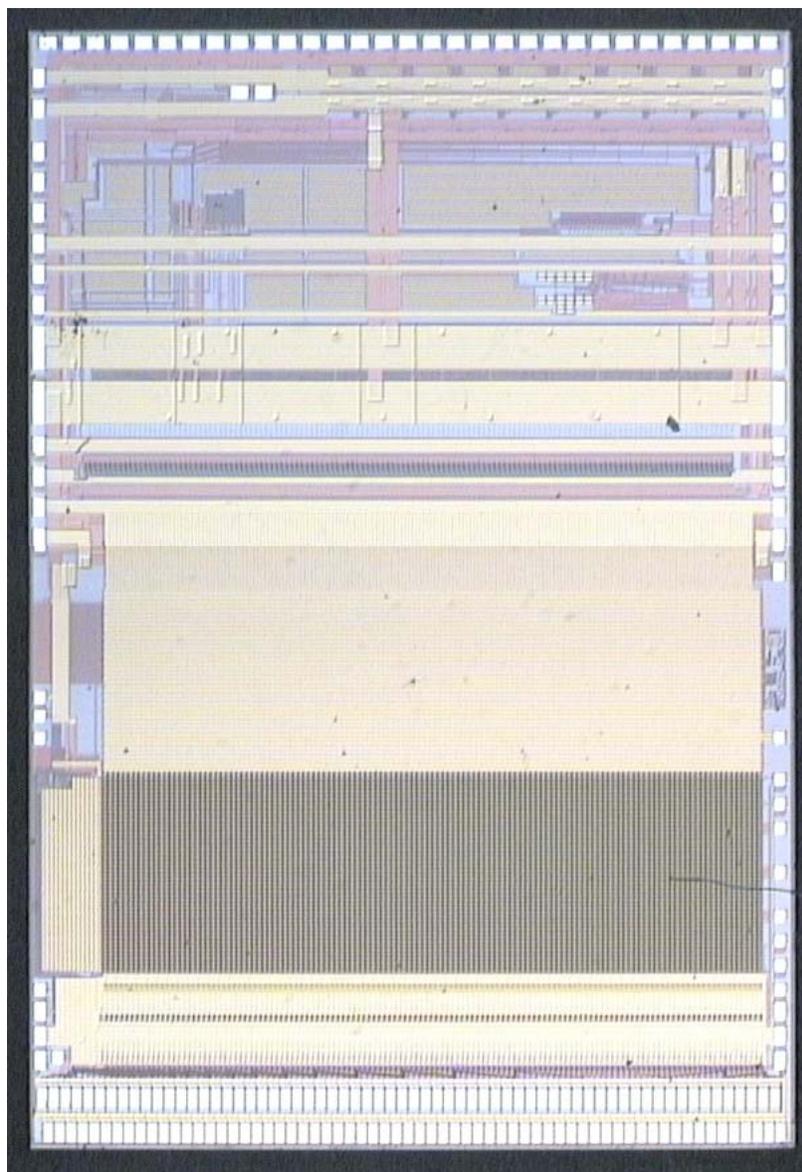


# **SVX4 User's Manual**

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Abstract: We present and describe the operation of the SVX4 chip.



**Figure 1** An actual picture of the SVX4 chip. The top of the picture is the back-end of the chip and the lower half is the front-end. The 128 input pads can be seen at the bottom of the picture.

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# 1. Introduction

The SVX4 is a custom 128-channel analog to digital converter chip used by DØ and CDF in Run IIb to read out their respective detectors. Each channel consists of an integrator (Front-End device, of FE) and a digitize/readout section (Back-End device, or BE). The input to each channel is sampled and temporarily stored in its own pipeline. Upon receiving a trigger signal, the relevant pipeline cell is reserved. Subsequent signals cause reserved cells to be digitized by a 128 parallel channel Wilkinson type 8-bit ADC, and then readout in byte-serial mode with optional zero suppression (sparsification). Salient features include (1) operation in either DØ mode or CDF mode (CDF mode features “deadtimeless operation” or continued acquisition during digitization and readout), (2) adjustable, loadable control parameters, including the integrator bandwidth and ADC polarity (only one input charge polarity will be used for Run IIb, but this feature remains for diagnostic purposes), (3) sparsified readout with nearest neighbor logic, (4) built-in charge injection with the ability for external voltage overriding for testing and calibration, and (5) a channel mask that is used for either charge injection or pin hole masking during chip operation. This document is meant to familiarize the user with the functionality of the SVX4 and goes on to include specifications, pin outs, timings and electrical information.

## 1.1 Historical Development

In the late 1980's, several versions of a fully custom chip called the SVX were built and tested <sup>i ii</sup>. As part of the Run IIa upgrade for DØ the SVX2 and for CDF the SVX3 were designed to meet the needs of the experiments by a collaboration of engineers at Fermilab and Lawrence Berkeley Laboratory <sup>iii iv v vi</sup>. Requirements dictated that the devices should be capable of operating at an interaction rate as fast as 132 nsec, that it have optimal performance for detector capacitances between 10 and 35 pF, and that it have an analog pipeline with a maximum delay of about 4 µsec to allow time to form a trigger signal.

For the SVX2 chip, when a trigger signal is received, data acquisition stops until the chip is completely read out. As plans for Run IIa evolved, deadtime became an issue for CDF and the development of the SVX3 with a deadtimeless feature evolved. The SVX4 is a chip which can be used in either mode. Additionally, the SVX4 is based on the SVX3 design which carried over the benefits of SVX3 operational experience as the Run IIb detector designs were being proposed. A large effort and several iterations proved necessary to overcome digital-analog coupling issues in deadtimeless operation.

The main features and specifications of the SVX4 are given below:

1. 128 channels per chip
2. Maximum interaction rate equal to 132 nsecs
3. Optimized for capacitive loads from 10-35 pF
4. Channel mask with dual functionality: used for either charge injection or masking of pin holes in the detector
5. Operation in either DØ or CDF mode using an external pad
6. Selectable input bandwidth

7. Double correlated sampling
8. Large dynamic range on input integrator to minimize deadtime due to pre-amplifier resets
9. Programmable analog pipeline (47 cells, 42 cells maximum depth for pipeline, 4 cells for trigger buffer, 1 cell for write amplifier pedestal)
10. Digization of analog signals up to 8 bits of resolution using a modified Wilkenson type ADC
11. Dynamic pedestal subtraction
12. Data sparsification (zero suppression)
13. Neighbor channel readout selection (cluster readout)
14. Low noise (S/N=10:1 to 20:1 for input capacitances from 35 pF to 10 pF for an input charge equivalent to 1 MIP = 4 fC)
15. Low power (approximately 3 mW/channel) to minimize the cooling requirements
16. Operation compatible with single-sided AC coupled devices
17. Ability to inject charge for testing and calibration in each channel
18. Daisy chain operation capability
19. Parallel bus data readout
20. Integral Data Valid strobe signal in the data bus (OBDV)
21. Can be implemented in the TSCM 0.25 micron radiation hard process

The document is arranged as follows: Section 2 gives a detailed description of the chip's operation, including timing diagrams, Section 3 defines the initialization bits in detail. Issues on measuring the performance of the chip in Section 4. The electrical specifications are given in Section 5 and Section 6 describes how to connect and mount chips. Section 7 lists a number of miscellaneous considerations. The appendices compare settings and measurements of the chip on several different test stands with those from the prototype DAQ system.

## **1.2 Simplified Operation**

The SVX4 is comprised of 128 channels of identical electronics along with additional circuitry that is common to all channels. Figure 1 shows a simplified diagram of one of the identical channels of electronics and some of common circuitry. Charge is received from the silicon strip detector via the input bond wire and integrated on a 200fC feedback capacitor,  $C_f$ , which sets the DC gain of the input amplifier to be 5 mV/fC. In addition to the detector input, a separate 40fC test input capacitor,  $C_t$ , is connected to each integrator via a programmable switch. The capacitor allows each channel to be pulsed independently (synchronously with with a common control pulse) to study channel operation or provide simulated events to the SVX4 to the data acquisition system. The AC response of the front end electronics is determined primarily by the integrator response (there is no shaper). For different interaction times and input capacitances, the bandwidth of the preamplifier is adjusted by means of control registers to provide the optimal preamplifier output rise time and hence minimum noise.

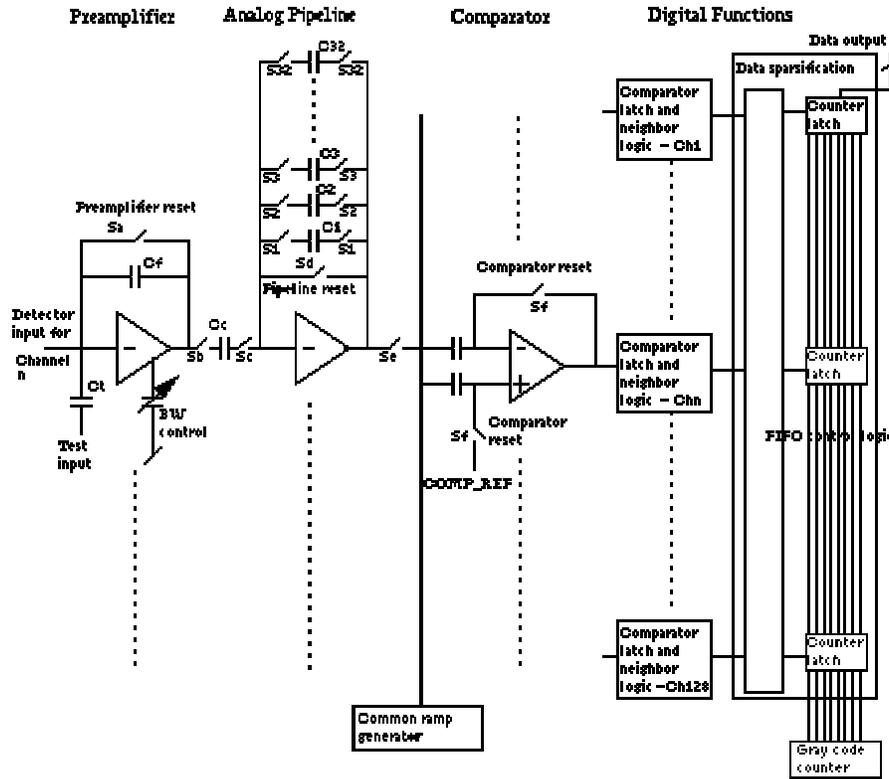


Figure 1 - Simplified Single Channel Block Diagram

Figure 2 Simplified single channel block diagram.

The output of the preamplifier (integrator) feeds the analog pipeline which has a length of 46 cells set by the minimum interaction time and maximum required time delay. The pipeline has a fixed voltage gain of three determined by the ratio of the value of the input coupling capacitor,  $C_c$ , and the storage capacitor,  $C_n$ . The effective depth of the pipeline is the same for all channels and can be set via digital control to have any value from 0 to 41 samples. The pipeline operates by sequentially sampling the output of the preamplifier on one of 46 storage capacitors. After each interaction period, switch  $S_d$  in the pipeline resets the next sampling capacitor causing the output of the preamplifier to be stored on the coupling capacitor,  $C_c$ , and thus performing a double correlated sample on the preamplifier output (this way the integrator baseline does not matter, only the change in level during a given beam crossing is stored in the pipeline). The integrator output is allowed to build until it can be reset by switch  $S_a$  at a convenient time as shown in Figure 2.



Figure 2 - Resetting Integrator Output During Large Beam Gap

Figure 3 Resetting integrator output during large beam gaps.

The voltage change indicated by VC6, VC14, and VC26 is stored on a sample capacitor for subsequent readout. Charge injection from opening Sd and the sample switches is stored on the sample capacitor along with the desired signal. These charge injection effects are compensated during the pipeline readout using a 47<sup>th</sup> pipeline cell reserved exclusively for this purpose. Resetting a storage capacitor can be done in 20 ns. However, the preamplifier requires a settling time of order 200 ns and is therefore reset during the major beam gaps in the main ring beam structure or during a readout. The dynamic range of the preamplifier is 240 fC.

Readout of the SVX4 begins when a Level 1 Accept control signal (derived from the system trigger) is sent to the chip. Depending on which mode the chip is configured, two things can occur: 1) in D0mode, pipeline acquisition should stop and pipeline readout of the appropriate storage capacitor should begin and 2) in CDF mode, pipeline acquisition continues and the appropriate pipeline is stored in a secondary pipeline where it awaits the readout and digitization process.

When the proper control signals are sent to the chip for pipeline read out, a pedestal correction is performed on the stored signal in the pipeline to correct for variations in switch charge injection and other errors. The output of each pipeline feeds a Wilkinson type 8 bit ADC. The ADC is formed by a separate analog comparator, analog delay (which is used for dynamical pedestal subtraction), a counter latch for each channel and common ramp generator and Gray Code counter which is used for all of the channels. A digital conversion is initiated by activating the analog comparator for each channel and then starting the ramp generator and then the Gray Code counter. The ramp is applied to the analog comparator along with the input signal to be digitized. When the comparator output changes, the counter latch is set (after passing through the analog delay) which stores the output of the Gray Code counter for that channel. The number stored in the digital latch is a measure of the amount of charge that was integrated by the preamplifier from a given interaction. When the number in the Gray Code latch exceeds a programmed threshold setting, that channel is considered to have a hit and it is tagged for readout.

The SVX4 is designed to work with single sided detectors, but is able to accept both positive and negative current input signals. The functionality discussed below is only used for diagnostic purposes. Several signal inversions take place inside the SVX4 chip. The output of the preamplifier is inverted as shown in Figure 1 (e.g. the output signal level is negative going for positive input current and positive going for negative input current). The pipeline inverts the preamplifier signal. The technique used to read out the pipeline causes a third signal inversion to occur. Thus during pipeline readout which occurs prior to digitization, the signal level to the analog comparator is negative going for positive input current or positive going for negative input current.

For proper operation, externally programmed polarity signals are used to choose either positive or negative input operation for the chip. Three bits (Pipeline Select, Ramp Polarity, Comparator Polarity) are provided for maximum flexibility to set levels inside the chip and establish the proper operation. The polarity signals perform three different functions inside the SVX4 chip. First Pipeline Select sets the reset point in the pipeline amplifier to one of two different values so that the output range of the pipeline can be maximized for a given polarity. The Ramp Polarity bit controls the direction (positive or negative) of the ramp generator to correspond to the polarity of the input signal. The third polarity bit, Comparator Polarity, is used to either pass or invert the comparator output so that the signal delivered to the following logic has the same meaning for both positive and negative current input signals.

As shown in Figure 1, the analog comparator feeds a latch and neighbor hit logic. The SVX4 data readout can take one of three different forms depending on the status of two control bits called Read Neighbors and Read All in the neighbor hit logic. If both of these bits are low, the channels to be read out are only those channels (i.e. hit channels) Whose digitized outputs exceed the threshold level which was digitally downloaded. If the Read Neighbor bit is set high, then hit channels *and* the channel immediately on each side of the hit channel are also read out. When chips are daisy chained together, neighbor information is passed from one chip to another so that if an end channel is hit, a neighbor channel on the adjacent chip is read out. Readout of neighbor channel amplitudes allows interpolation to obtain higher hit location accuracy. Under some situations such as testing, all channels on a chip can be read out regardless of signal level by setting the Read All bit high.

The hit threshold level for an SVX4 chip is set digitally and is the same for all channels on that chip. Normally the threshold is set at some fraction of a MIP which results in a relatively coarse threshold resolution (e. g. 2000 e). To overcome this problem, control of the A/D ramp start voltage is provided which allows fine tuning of the noise hit rate. An internal adjustment of the ramp start voltage (RAMP-PED) effectively allows the threshold to be adjusted with 400 e resolution.

The output of the neighbor logic circuit from all the channels form an ordered array of the channels to be read out. Before the chip is read out, the address and data for each channel to be read is stacked in FIFO that uses a token system for readout. When readout does begin, channels are read out sequentially beginning with the lowest address channel.

Channel 1 is at the top for a chip which has his detector inputs on the left hand side of the chip.

Control of the SVX4 and data readout is handled by digital and bias pads in the I/O section of the right hand side of the chip. There are three pads called FEMODE, BEMODE, and CHMODE which are used to select one of the four possible operating cycles (Initialize, Acquire, Digitize, and Readout) for the SVX4. Sixteen pads, called BUS0-7 and BUS0-7 bar, are used to output address and data information from the SVXII during the Readout Mode. The same sixteen pads are used for real time control of internal switches in the other three operating modes (only for D0 operation, CDF operation uses control lines independent of the bus lines). For these three modes, the last information on the pads prior to a mode change is held on internal latches before switching to the next mode. Two other pins, Bottom Neighbor and Top Neighbor, are used to communicate with adjacent chips on neighbor readout. Priority In and Priority Out are used to communicate with adjacent chips. These two pins carry different information for each of the four different operating modes.

## 2 Functional Description

In this Section the function of the SVX4 is described. Section 2.1 gives a brief overview, Section 2.2 describes the operation of the chip in detail, and Section 2.3 gives detailed timing diagrams. Items in the initialization bit stream are described as they relate to operation; a concise list is deferred to Section 3. Section 2.4 gives the physical layout of the chip, including tables of all the input and output pads.

### 2.1 Overview

The SVX4 consists of 128 identical channels. Each channel has two parts, a Front-End and a Back-End. The Front-End contains the integrator and storage pipeline. The Back-End contains the ADC for digitization and the readout logic and drivers. The major cycles of operation for these parts are Initialization (both), Acquisition (Front-End), Digitization (Back-End), and Readout (Back-End). The initialization cycle usually is performed once, followed by repeated data acquisition, digitization, and readout cycles. The Acquisition cycle occurs simultaneously with the Digitize and Readout cycles in CDF mode, but operated exclusively in DØ mode. Three input signals, FEMODE, BEMODE, and CHMODE, are used to change the modes as summarized Table 1.

FE Mode	BE Mode	CDF chip state	DØ chip state
0	0	Initialize	Initialize
0	1	--	Acquire
1	0	Acquire & Readout	Readout
1	1	Acquire & Digitize	Digitize

**Table 1 Table showing the various states of the chip in either CDF mode or DØ mode depending on the various conditions of the mode lines.**

To change the state of the front or back-end, the mode bits are changed, and then the CHMODE pad is pulsed high to complete the transition to the new state of operation. Mode signals are internally latched whenever CHMODE is low. Timing specifications and the appropriate levels for FEMODE and BEMODE for each of the three cycles (initialization, acquire, and readout) are given in Section 2.3.

It is also important to realize that depending on which mode (D0 or CDF) has been configured, the bus lines will operate as control for the ADC only (CDF mode) or will operate as control lines for operation in acquire or digitize (D0 mode). The function of the control lines is shown in Table 2. Depending on the mode of the chip, the bus lines could have different functions.

Pin name, Readout mode function	Digitize mode function	Acquire mode function in D0 mode only
Bus0	Comp_rst	--
Bus1	Ramp_rst	--
Bus2	--	PRD2
Bus3	Rref_sel	--
Bus4	--	PARST
Bus5	--	L1A
Bus6	--	PRD1
Bus7	--	CalSR

**Table 2 Bus pin multiplexing table. Calsr is ored with the CALSR pad in the Acquire cycle and ored with WrSEU in the Initialize cycle.**

## 2.2 Detailed Operation

### 2.2.1 The Front-End

The SVX4 front end was designed at Fermilab and mates with the SVX4 back end, designed at LBL, to produce a complete SVX4 128 channel silicon detector readout chip. The front end contains 128 identical channels of integrating charge preamp and a 46 cell analog pipeline which is cycled by the beam crossing clock. Hit cells are temporarily removed from the pipeline for readout to the back end, where the data is digitized, sparsified, and read out. SVX4 is “deadtimeless,” so that front end signal acquisition can continue uninterrupted while back end digitization and readout is occurring. Operation of the front end requires only a 2.5V supply, a front end clock, and a few digital control lines. The front end has two modes of operation: **Initialize** and **Acquire**.

In **Initialize** mode, the front end clock signal (FEClk) is routed to control a 148 bit shift register, which is downloaded with program bits. 20 of these bits set programmable parameters such as trigger delay, bandwidth, bias current, etc. The remaining 128 bits

form a mask register which is used to selectively enable or disable reception of a calibration test charge to each of the 128 preamp inputs. The serial program bit stream line, Srin, actually comes from the back end chip which also has a programmable register. The serial data is clocked into the registers on the rising edge of FEClk. After downloading of the shift register is complete, application of a strobe pulse (via the CalStrobe control line) transfers the 20 programmable parameter bits to a SEU tolerant shadow register. The strobe also resets the pipeline cell position to cell0. Initialization must be performed after power up and before acquisition begins. Although theoretically not necessary, it may be desirable to periodically repeat initialization to insure that the chip remains in a known operating condition.

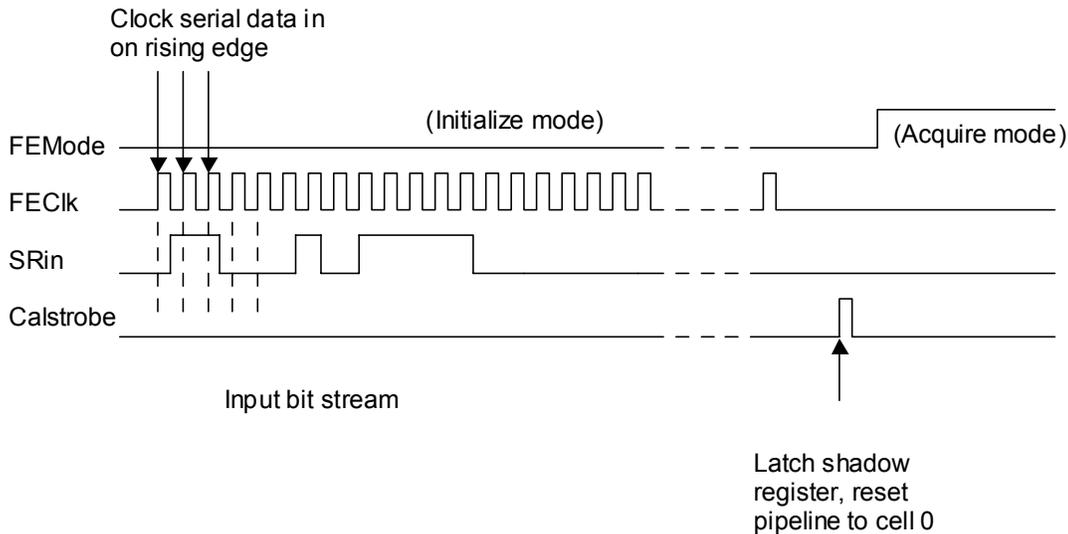


Figure 4 Timing diagram for the initialization of the SVX4.

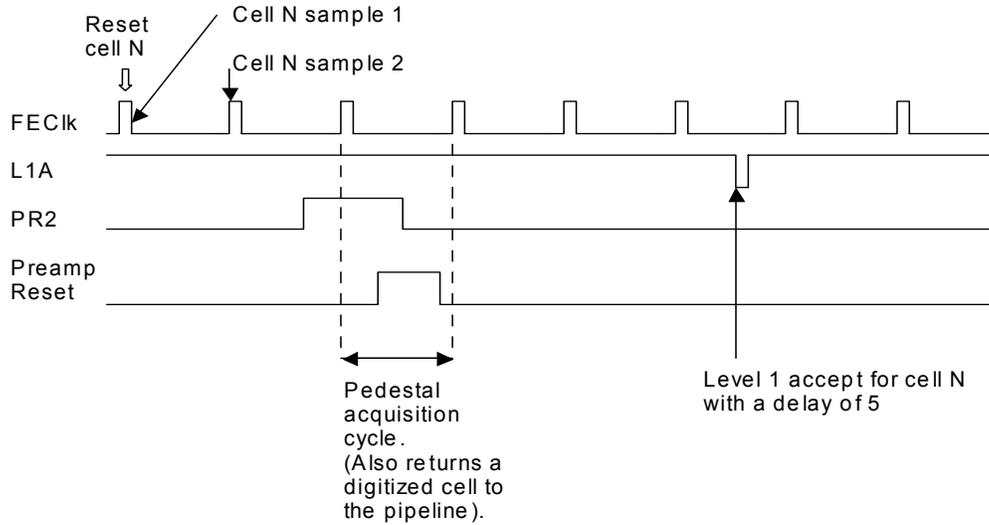
In **Acquire** mode, the front end clock (FEClk) is routed to the analog pipeline and is used to advance the 46 cells in round robin fashion at the beam crossing rate. At each of the 128 channel inputs, an integrating charge preamp accepts a positive input charge from the detector, and the preamp output feeds the pipeline. The system charge transfer gain is 15 mV/fC. As the pipeline cells are advanced with the front end clock, they perform correlated double samples on the preamp output. A given cell is reset while the front end clock is high, takes a first sample of the preamp output when the clock goes low, and takes the second sample when the clock goes back high, which also advances the pipeline to the next cell. The voltage difference between the two samples, representing the preamp charge integrated during that time, is thus stored in the cell. The duty cycle of the clock obviously controls the amount of time spent resetting and acquiring on a cell. Typically, the front end clock should have a low duty cycle so that only a small portion of the clock cycle time (minimum 20 ns) is spent resetting, and most is used for acquiring the preamp output. This is desirable since the slower the preamp risetime, the lower is its series noise.

The dynamic range of the preamp (200 fC) is larger than the dynamic range of the pipeline (40 fC), so that many signal charges can be integrated and sampled without saturating the preamp. However, the preamp must periodically be reset via an external control line (PreampReset) in order to prevent eventual saturation. PreampReset is active high, with a minimum required width of 80 ns to achieve complete reset. It is typically performed during beam gaps in order to avoid incurring any downtime. The timing of PreampReset is not critical, but after reset, one beam crossing time should be allowed for the preamps to settle before inputs can be accurately acquired.

The Level 1 Accept (L1A) control input is used to remove a “hit” cell from the pipeline, with a delay of from 1 to 42 beam crossings, and temporarily store it in a FIFO so that it is queued for readout to the back end. The delay is determined by the value programmed in the shift register during Initialize mode. L1A is normally high during acquisition, and pulsed low to store a cell. L1A must go low and return high between front end clocks, i.e., while FEClk is low. Up to four cells can be stored in the FIFO and queued for readout. If four cells are stored, additional L1As are simply ignored.

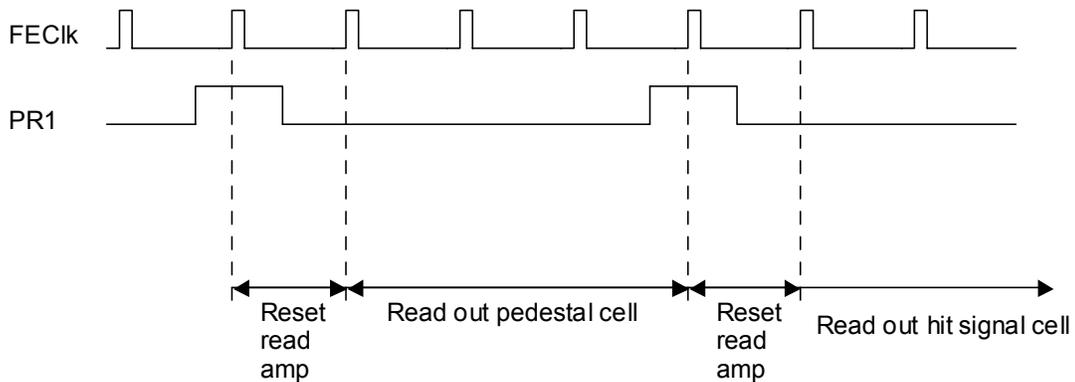
A special pipeline cell, the “pedestal cell,” is reserved for acquiring pedestal only. It is used during readout along with a stored cell. The back end essentially digitizes the difference between the hit cell and the pedestal cell. The pedestal cell is not part of the normal round robin of acquisition cells, and so must be explicitly refreshed periodically. This is one of the functions of the PR2 control line. If PR2 is high when FEClk transitions from low to high, then normal acquisition is inhibited for that clock cycle. The normally intended pipeline acquisition cell is skipped over and the pedestal cell instead is placed in the pipeline for acquisition of the pedestal. Thus one cycle of downtime is incurred by refreshing the pedestal cell. If this is done during a beam gap, downtime can be avoided.

Operation of SVX4 is “downtimeless,” so that the readout and digitization process can occur in parallel with normal acquisition. Front end cell readout is accomplished by asserting the PR1 control line in conjunction with FEClk (which continues to control normal acquisition). If PR1 is high at the low to high transition of FEClk (PR1 should then subsequently be lowered), the pedestal cell readout is then initiated. The read amp is reset during the first clock cycle, then the pedestal cell is held in the read amp at the start of the second clock cycle. The read amp output feeds the back end, which uses the pedestal voltage to autozero the ADC. When PR1 is raised a second time, the next FEClk low to high transition removes the pedestal cap from the read amp and initiates readout of the stored hit cell, which is read out in a manner similar to the pedestal cell. The hit cell voltage can then be digitized by the back end. If desired, the effective signal polarity which is digitized can be reversed by setting the PB parameter bit in Initialize mode. This reverses the readout order to (signal – pedestal) instead of (pedestal – signal). After digitization is complete, the readout cell needs to be removed from the FIFO and placed back into the pipeline. This is accomplished by doing a PR2, which has the dual function of digitally restoring the cell to the pipeline and of retaking the analog pedestal on the pedestal cell capacitor.



PreampReset shown during pedestal acquisition cycle, but this can occur any time.

**Figure 5 Timing diagram for the acquire cycle of the SVX4.**



**Figure 6 Timing diagram for the pipeline readout of the SVX4.**

In order to facilitate testing, a small charge injection capacitor (25 fF) can be switched in from each preamp input to a common bus line. A 128 bit programmable channel register (downloaded in Initialize mode) can function as a mask register, and determines whether or not an injection capacitor is switched in for each channel. When in Acquire mode, the common bus voltage is determined by the state of the CalStrobe control line. When CalStrobe is low, the common bus is grounded. When CalStrobe goes high, the common

bus is connected to the VCAL pad. Thus, raising CalStrobe injects a charge of magnitude  $(VCAL)(25fF)$  to each channel which has a mask setting of 0.

Usually it is desirable for all channels on a chip to be functional. However, sometimes “black hole” effects are present in detectors, which result in a DC current being applied to a preamp input. This can effect neighboring channels by turning on input diode protection circuits, which can activate parasitic current paths. Therefore, a provision has been included which allows a selected channel's preamp reset to be held high, which harmlessly sinks any positive input current to ground without affecting any other channels. This feature is enabled by setting the programmable Mask/Disable bit during Initialize. If Mask/Enable is high, then the 128 bit channel register is used not as a charge injection mask register, but as a channel disable register. Any channel which has its mask bit set high will have its preamp reset held always high.

Powering the SVX4 Front End is very straightforward. An analog power supply, **AVDD**, of 2.5V must be provided for the preamp and the analog sections of the pipeline. This supply is bypassed on chip with an integrated 0.012 uF capacitor. Best deadtimeless performance is obtained if an external 0.1 uF bypass capacitor is added close to the chip (within an inch or so). The front end analog ground is NOT supplied through a pad, but through the low resistance back side of the die. Thus, the die must be connectively attached to a ground plane. A digital supply (DVDD and DGND) is required to drive the pipeline digital logic. This supply is not derived from front end pads, but is routed in from the back end chip digital supply. For deadtimeless operation, AVDD and DVDD should come from two physically separate power supplies. If, however, front end acquisition will not be occurring simultaneously with back end digitization and readout, it may be possible to derive AVDD and DVDD from the same external power supply.

There is an internal master bias circuit on the front end chip which supplies the bias reference for both preamp and pipeline. Preamp and pipeline bias currents can be adjusted via programmable shift register bits. The on-chip bias reference voltage is connected to the **Bias** pad. Under normal conditions, no external bias current reference needs to be provided. Since the bias circuit is referenced to AVDD, an on-chip Bias to AVDD bypass capacitor is included. An external bypass capacitor from Bias to ground can be provided in order to improve the integrator PSRR. The optimal value of this bypass will depend on the value of the integrator input capacitance to ground (not to neighbor channels).

Two preamp diagnostic bias pads are included on the prototype so that they can be forced if necessary. (Ncas) supplies an internal preamp cascode voltage, and Vrset controls the placement of the DC reset point of the preamp. Under normal conditions, no connection to these pads is necessary.

Several other diagnostic pads are available for chip testing, including (P127), (R127), and (W127). These are buffered versions of the Ch. 127 preamp output, pipeline read amp output, and pipeline write amp output. The buffers are simple PMOS followers which

require external bias (a pullup resistor). Without an external pullup, a buffer will be inactive.

### 2.2.2 The Back-End

The pipeline read/ADC timing consists of two sets of interdependent signal sequences. One is the *ADC Ramp Setup* (**BECLK/Ramp\_rst/Rref\_sel**), and the other *Pipeline Read* (**PRD1/FECLK/Comp\_rst**). The *ADC Ramp Setup* controls the ADC ramp generator, the selection of the ADC ramp reference voltage (fixed) or the ADC ramp pedestal (programmable), and start of the ADC counter when not in Real-Time Pedestal Subtraction mode (RTPS). The *Pipeline Read* sequence controls the signal/pedestal CDS of the pipeline read amplifier on one terminal of the ADC input comparator, as well as the ADC ramp sampling on the other. Significant features of the sequences are described below.

#### *ADC Ramp Setup*

- 1) Pipeline read and signal digitization is initiated by entering DIGITIZE mode, that is, by asserting (**FEMODE=1 + BEMODE=1**) under **CHMODE=1** [①]. If **CHMODE=0**, DIGITIZE will instead be entered at  $\uparrow$ **CHMODE** when (**FEMODE=1 + BEMODE=1**). This behavior is the result of the MODE pins being processed through a transparent D-latch, which is controlled by **CHMODE**. MODE changes must occur on or about  $\uparrow$ **BECLK**, or while **BECLK=0**. Upon entering DIGITIZE, the I/O pins **BUS\_0**, **BUS\_1**, **BUS\_3**, change function to **Comp\_rst**, **Ramp\_rst**, **RRef\_sel**, respectively.
- 2) Asserting **RRef\_sel=0** while **Ramp\_rst=1** resets the ADC ramp to the fixed ADC ramp reference voltage level [②], which is above the programmable ramp pedestal voltage level. **RRef\_sel=0** while **Ramp\_rst=1** must then be asserted in concert with **Comp\_rst**, as described below, in order to subtract the programmed pedestal value from the ramp reference voltage. Asserting **Ramp\_rst=1** also asserts the internal counter reset signal **Cntr\_Rst** when RTPS mode is off.
- 3) When **Ramp\_rst** is de-asserted the ADC ramp commences in the programmed direction [③]. If RTPS mode is off, the internal signal **Cntr\_Rst** will also be de-asserted. If RTPS mode is selected, **Cntr\_Rst** is controlled by the dynamic threshold comparator circuit. In this case, the counter will be held in reset until the dynamic threshold comparator fires, sometime after the ADC ramp is initiated.

#### *Pipeline Read*

- 4) The pipeline signal/pedestal sampling sequence is initiated by  $\uparrow$ **FECLK** under **PRD1=1**. The relationship of **PRD1** and **FECLK** is fixed in terms of the state of **PRD1** during the phases of **FECLK**, as specified above. The 1<sup>st</sup>  $\uparrow$ **FECLK** under **PRD1** begins the cycle [④]. In the above example, the programmed order ("PB" config bit) is pedestal/signal.
- 5) During time **adc.T6**, the pipeline pedestal values are sampled onto the ADC input capacitors while the ADC comparator inputs (the other terminal of the input capacitors) are reset to a fixed internal reference level. Concurrently, during time **adc.W5** the ramp reference level is being sampled onto identical comparator input capacitors on the other comparator input terminal. It can be seen on the internal

- signal **adcin\_3** (no-hit channel) that the pipeline pedestal value is available to the ADC at the 2<sup>nd</sup>  $\downarrow$ **FECLK** [5].
- 6) When **Comp\_rst** is de-asserted the ADC comparators are un-reset [6]. The ADC input sampling capacitors are now pre-charged to the pipeline pedestal values. From this time on, the ADC input is reading the difference of the pipeline output and the sampled pipeline pedestal, thus the CDS cycle is complete. However, the correct pipeline signal value will not be applied until the 2<sup>nd</sup>  $\downarrow$ **PRD1**.
  - 7)  $\uparrow$ **RRef\_sel** applies the desired offset to the other ADC comparator input capacitor [7]. This action must take place after  $\downarrow$ **Comp\_rst** (**adc.T7**) in order to achieve the desired CDS operation (rampref-ramped) on the ramp. Note that the effect of this CDS operation is to pre-charge a small offset across the ramp capacitor, which the ramp must “make-up” before it achieves zero-crossing of the original ramp reference level value. The purpose of this process is to allow the ramp to slew for a small period into its linear region, so that the ADC comparators will fire within the linear region of the ramp for small input signals. This is especially important for accurate noise measurement.
  - 8) On the 3<sup>rd</sup>  $\uparrow$ **FECLK**, under the 2<sup>nd</sup> **PRD1**=1, the pipeline pedestal value is de-asserted by the pipeline read amp [8]. On the 2<sup>nd</sup>  $\downarrow$ **PRD1** the signal values are asserted by the pipeline read amp [9] *{I am not sure if this is correct—the simulation shows this is the case, but Tom’s measurements on the pipeline test chip indicate that it comes on falling FECLK just like the pedestal values—Brad}*. This can be clearly seen on the internal signal **adcin\_4** (hit channel) above. Time **adc.T8** is required to allow the pipeline read amp to settle (and hence the signal-pedestal value at the ADC input) before starting the conversion.

Timing Spec	Description	Min	Nom	Max
<b>adc.T1</b>	1 <sup>st</sup> $\uparrow$ <b>BECLK</b> to $\downarrow$ <b>Ramp_rst</b>	4* <b>BECLK</b>	900 nS	--
<b>adc.W1</b>	Width of <b>Ramp_rst</b> in DIGITIZE mode	600 nS	900 nS	--
<b>adc.W2</b>	Width of <b>RRef_sel</b> low under <b>Ramp_rst</b>	500 nS	600 nS	--
<b>adc.T2</b>	$\uparrow$ <b>RRef_sel</b> to $\downarrow$ <b>Ramp_rst</b>	200 nS	300 nS	--
<b>adc.T3</b>	$\uparrow$ <b>PRD1</b> to 1 <sup>st</sup> $\uparrow$ <b>FECLK</b> of pipeline read	5 nS	54 nS	--
<b>adc.W3</b>	Width of a <b>PRD1</b>	30 nS	1* <b>FECLK</b>	--
<b>adc.W4</b>	Width of <b>FECLK</b> high	20 nS	25 nS	--
<b>adc.T4</b>	Period of <b>FECLK</b>	65 nS	132 nS	--
<b>adc.T5</b>	Time between two $\uparrow$ <b>PRD1</b> for pipeline read	3* <b>FECLK</b>	4* <b>FECLK</b>	--
<b>adc.T6</b>	2 <sup>nd</sup> $\downarrow$ <b>FECLK</b> of pipeline read to $\downarrow$ <b>Comp_rst</b>	55 nS	132 nS	--
<b>adc.T7</b>	$\downarrow$ <b>Comp_rst</b> to $\uparrow$ <b>RRef_sel</b>	50 nS	50 nS	--
<b>adc.W5</b>	Width of <b>Comp_rst</b>	100 nS	455 nS	--
<b>adc.T8</b>	2 <sup>nd</sup> $\downarrow$ <b>PRD1</b> to $\downarrow$ <b>Ramp_rst</b>	100 nS	132 nS	--

Table 3 Timing for the various signals for pipeline readout and ADC setup.

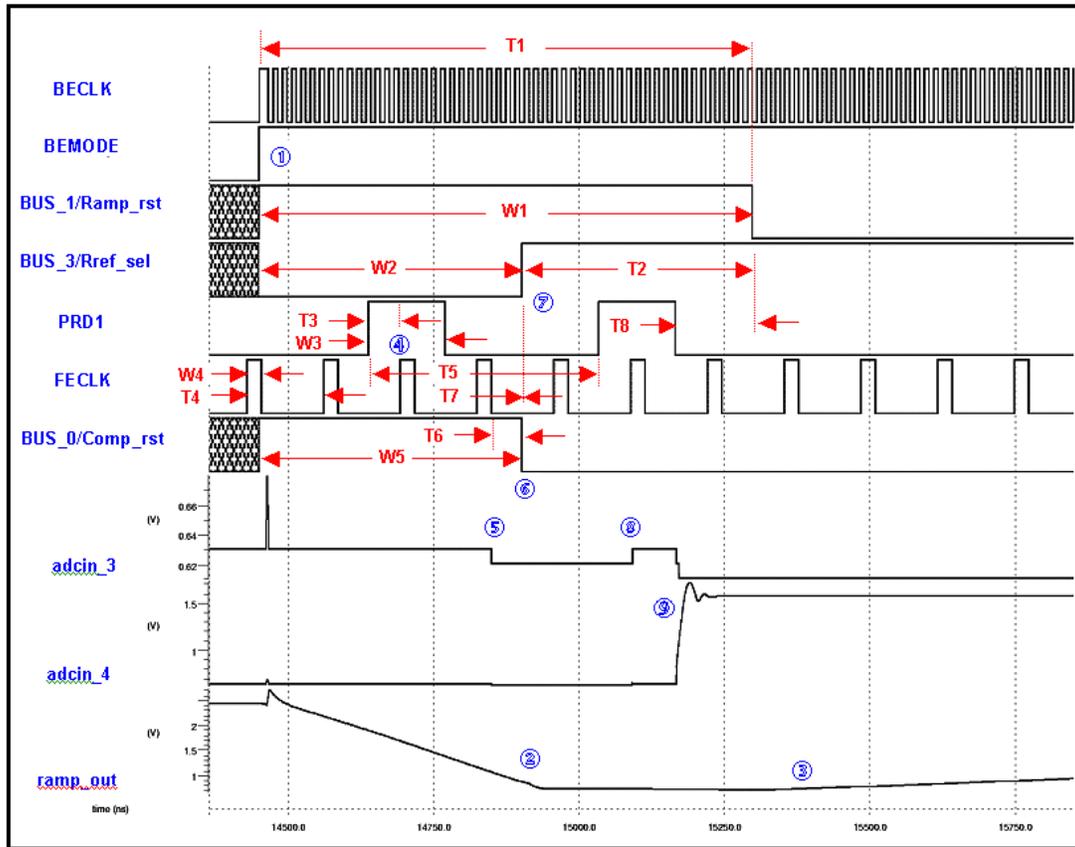


Figure 7 Timing diagram for pipeline read and ADC.

### 3 Initialization Bit Stream

#### 3.1.1 SVX4 Configuration Register Table

Bit Number	Bit Name	Description	Values	Nominal Setting
<b>— Frontend Bit Assignments —</b>				
0:127	Mask [127:0]	Cal mask or channel disable register (see next bit assignment)	0 = mask/enable 1 = unmask/disable	0 .. 0
128	Disable	Select whether mask reg acts as a channel disable reg or a cal mask reg	0 = cal mask 1 = channel disable	0
129:132	BW [0:3]	Preamp risetime adjustment (depends on input capacitance), binary weighted	For $C_{in}=10$ pF: $T_r \approx 25$ nS + (BW * 4 nS) For $C_{in}=50$ pF: $T_r \approx 60$ nS + (BW * 10 nS)	0010
133:136	Isel [0:3]		Bias current $\approx 164$ uA + (Isel * 32 uA)	0010
137:138	IWsel [0:1]	Pipeline write amp bias current adjustment, NOT binary weighted	Bias current $\approx 26$ uA + (IWsel0 * 26 uA) + (IWsel1 * 26 uA)	10
139:140	IRsel [0:1]			
141:146	PickDel [0:5]	Trigger latency; select system L1A delay as a number of FEClk periods	0 .. 42	TBD
147	PB	Pipeline readout order	0 = pedestal, signal 1 = signal, pedestal	0
<b>— Backend Bit Assignments —</b>				
148:154	ID [6:0]	Chip ID assignment	0 .. 127	TBD
155	RTPS	Real Time Pedestal Subtraction disable	0 = RTPS on 1 = RTPS off	0
156	Rd127	Always readout channel 127 regardless of hit status	0=Rd127 off 1 = Rd127 on	0
157	Rd63	Always readout channel 63 regardless of hit status	0=Rd63 off 1 = Rd63 on	0
158	RdAll	Always readout all channels	0=RdAll off 1 = RdAll on	0
159	RdNeigh	Readout hit channels and their neighbors	0=RdNeigh off 1 = RdNeigh on	1

Bit Number	Bit Name	Description	Values	Nominal Setting
160:163	RampPed [0:3]	ADC ramp pedestal setting, binary weighted	RampDir=0: Ped $\approx$ 480 mV +(RampPed * 23 mV) RampDir=1: Ped $\approx$ 1.8 V -(RampPed * 23 mV)	0001
164	RampDir	ADC ramp direction, ramp up or ramp down	0 = ramp up 1 = ramp down	0
165	CompPol	Comparator polarity; sets comparator and delay input for 0 $\rightarrow$ 1 or 1 $\rightarrow$ 0 transition	0 = 0 $\rightarrow$ 1 (for RampDir=0) 1 = 1 $\rightarrow$ 0 (for RampDir=1)	0
166:168	RampRng [0:2]	ADC ramp range, adjusts slope of ramp	Slope $\approx$ 0.5 mV/nS * [1+(4*r0)+(3*r1)+(1*r2)] <sup>-1</sup>	000
169:176	Thresh [7:0]	ADC digital threshold setting, Gray code	0 .. 255	TBD
177:184	CntrMod [7:0]	Counter Modulo, sets counter value at which overflow occurs, Gray code	0 .. 255	TBD
185	FC	First Chip flag; enables the first chip to drive OBDV before readout begins	1 = this is the first chip	0
186	LC	Last Chip flag; enables the last chip to drive OBDV after readout ends	1 = this is the last chip	0
187:189	DriverI [2:0]	Output driver current select; selects output series resistance; the resistance selected appears in series on EACH output pin (plus and minus)	$R \approx [(d2/43) + (d1/86) + (d0/172)]^{-1}$ Drivers off if DriverI = 0	111

### 3.2 SVX4 Configuration Register Exposition

Below we give an extended discussion of the bits that are downloaded into the configuration register.

0: PB (pipeline readout polarity bit). 0 = pedestal – signal, 1 = signal – pedestal.

1-6: Pipeline level 1 trigger delay. Bit 1 is MSB, bit 6 is LSB. Valid range is 1-42.

7-8: IRSel1-0 (pipeline read amp bias current select). Read amp bias current = 13  $\mu$ A + (IRSel0)\*(13  $\mu$ A) + (IRSel1)\*(26  $\mu$ A). Increasing the read amp bias current simply speeds up the risetime. The lowest current is probably acceptable.

9-10: IWSel1-0 (pipeline write amp bias current select). Write amp bias current =  $26 \text{ uA} + (\text{IRSel0}) * (26 \text{ uA}) + (\text{IRSel1}) * (26 \text{ uA})$ . Increasing the write amp bias current speeds up the pipeline reset speed and the pipeline risetime. Nominal bias current =  $52 \text{ uA}$ .

11-14: Isel3-0 (preamp input transistor bias current select). Bias current =  $164 \text{ uA} + (\text{Isel3}) * (256 \text{ uA}) + (\text{Isel2}) * (128 \text{ uA}) + (\text{Isel1}) * (64 \text{ uA}) + (\text{Isel0}) * (32 \text{ uA})$ .

15-18: BW3-0 (preamp bandwidth). Used to adjust preamp risetime. Risetime will depend on input capacitance, bias current, and bandwidth setting. The bits are binary weighted:  $\text{BW0} = \text{LSB}$ ,  $\text{BW3} = \text{MSB}$ .

19: Mask/Disable. If Mask/Disable = low, then the 128 bit channel register functions as a mask register for test charge injection (register bit = high to enable charge injection). If Mask/Disable = high, then the 128 bit channel register functions as a channel disable register (register bit = high to disable channel).

20-147: Channel register <0:127>

## 4 Mechanical and Electrical Specifications

We went through and measure all the specifications of the SVX4 chip and they are listed below. Various data was collected by the designers of the chip and that data is listed in tabular format.

### 4.1 Pad layout

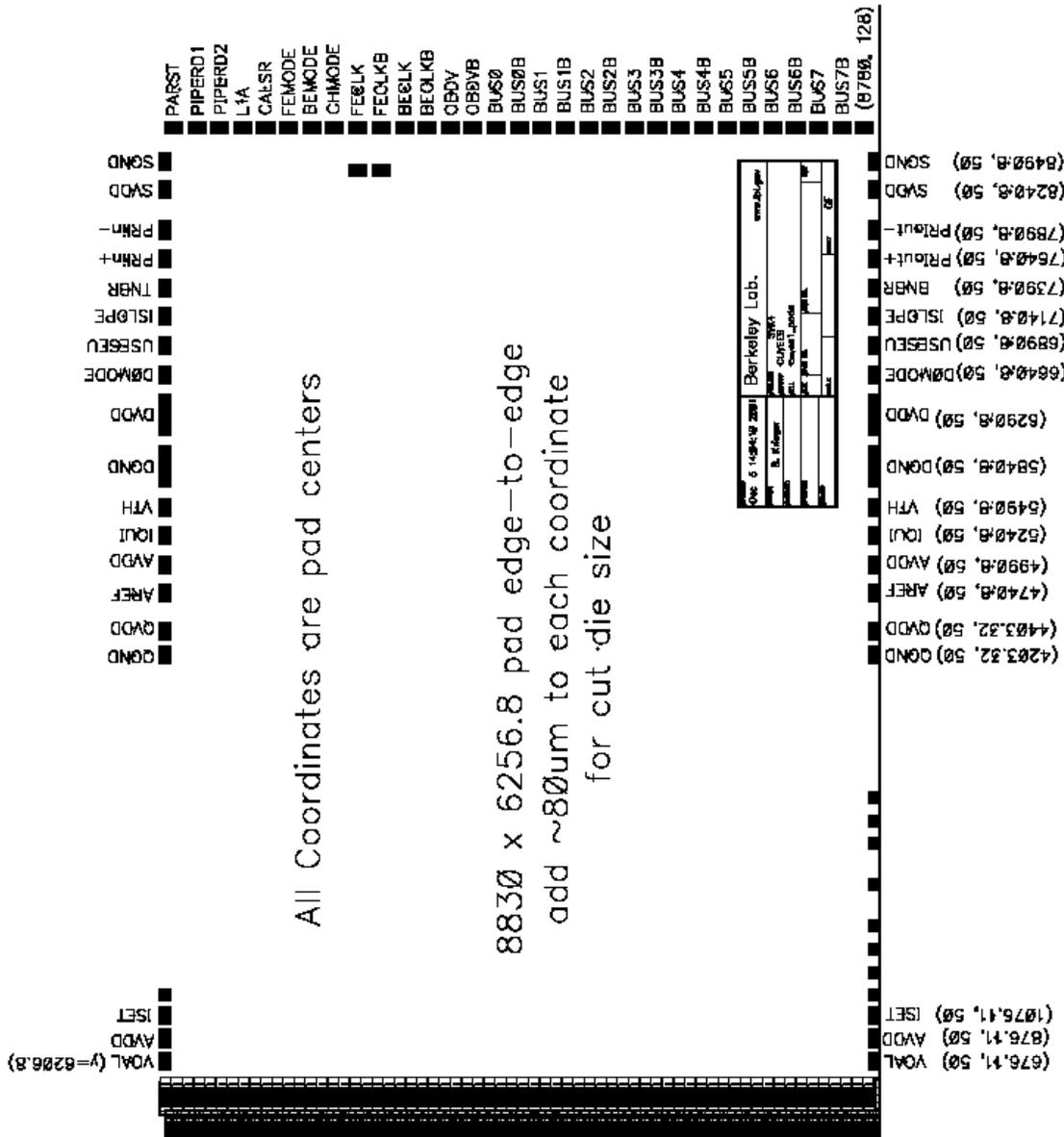


Figure 8 Pad layout on the SVX4

## 4.2 Pin List for the SVX4

Pin Number	Pin Name	Type Analog Digital	Type Input Output	Nom. Voltage	Wire Bonded	Description & External Components Required
1, 79	VCAL	A	I	AVDD <sub>fe</sub> ÷ 4	Either	Calibration charge setting
2, 15, 71, 78	AVDD	A	I	2.5	Either	Analog power supply—decouple to gnd! w/0.1 uF
3, 77	Bias	A	I	0.8	Either	Frontend master bias reference—decouple to AVDD <sub>fe</sub> w/10 nF
4, 76	VRset	A	I	1.0	No	Frontend reset level reference voltage
5	PreampBuf127	A	O	--	No	Ch127 preamp buffered output; requires ext resistor
6	Ncas	A	O	0.6	No	
7, 8, 9, 12, 13, 75, 210	gnd!	A	I	0	No	Analog ground, substrate
10	ReadBuf127	A	O	--	No	Ch127 Pipeline Read amplifier output; requires ext. resistor
11	WriteBuf127	A	O	--	No	Ch127 Pipeline Write amplifier output; requires external resistor
14, 72	AREF	A	I	2.5	Either	ADC ramp pedestal DAC reference
16, 70	IQUI	A	I	0.6	Either	ADC and data receiver bias current setting—7.7k resistor to AVDD <sub>dac</sub>
17, 69	VTH	A	I	0.9	Either	Dynamic Pedestal Subtraction threshold voltage setting
18, 68, 74	gndd!	A	I	0	Either 19 or 69	Digital ground
19, 67, 73	vddd!	A	I	2.5	Either 20 or 68	Digital Vdd
20, 66	D0MODE	D	I	0/2.5	Either	Connect to vddd! for D0, gndd! For CDF mode
21, 65	USESEU	D	I	0/2.5	Either	Connect to vddd! to select SEU register for configuration, or gndd! for shift register output

Pin Number	Pin Name	Analog Digital Diff	Input Output I/O	Nom. Voltage	Wire Bonded	Description & External Components Required
22, 64	ISLOPE	A	I	1.5	Either	ADC ramp slope bias— 36k resistor to gnd!
23	BNBR	D	I/O	0/2.5	Yes	Bottom Neighbor; open drain w/2k internal pull-up
24	PRIOUT	Diff	O	0-2.5	Yes	Priority Out plus
25	PRIOUTB	Diff	O	0-2.5	Yes	Priority Out minus
26, 60	SVDD	A	I	2.5	Either	Output Driver supply
27, 59	SGND	A	I	0	Either	Output Driver ground
28	EXTRA	--	--	--	No	Spare pad
29, 31, 33, 35, 37, 39, 41, 43	BUS<7>, ..., BUS<0>	Diff	I/O	0-2.5	Yes	Data bus 7—0 minus (see “Bus Pin Multiplexing Table” for secondary pin function by mode)
30, 32, 34, 36, 38, 40, 42, 44	BUS<7>, ..., BUS<0>	Diff	I/O	0-2.5	Yes	Data bus 7—0 plus (see “Bus Pin Multiplexing Table” for secondary pin function by mode)
45	OBDVB	Diff	I/O	0-2.5	Yes	Odd Byte Data Valid minus
46	OBDV	Diff	I/O	0-2.5	Yes	Odd Byte Data Valid plus
47, 208	BECLKB	Diff	I	0-2.5	Either	Backend Clock minus
48, 209	BECLK	Diff	I	0-2.5	Either	Backend Clock plus
49	FECLKB	Diff	I	0-2.5	Either	Frontend Clock minus
50	FECLK	Diff	I	0-2.5	Either	Frontend Clock plus
51	CHMODE	D	I	0/2.5	Yes	Change Mode
52	BEMODE	D	I	0/2.5	Yes	Backend Mode (Mode 1)
53	FEMODE	D	I	0/2.5	Yes	Frontend Mode (Mode 0)
54	CALSR	D	I	0/2.5	Yes*	Cal Strobe (Acquire mode) Write SEU reg (Initialize)
55	L1A	D	I	0/2.5	Yes*	Level 1 Accept
56	PIPERD2	D	I	0/2.5	Yes*	Pipeline Read 2
57	PIPERD1	D	I	0/2.5	Yes*	Pipeline Read 1
58	PARST	D	I	0/2.5	Yes*	Preamplifier Reset
61	PRIINB	Diff	O	0-2.5	Yes	Priority In minus
62	PRIIN	Diff	O	0-2.5	Yes	Priority In plus
63	TNBR	D	I/O	0/2.5	Yes	Top Neighbor; open drain w/2k internal pull-up
80-207	In<0—127>	A	I	0.45	Yes	Detector Inputs

### 4.3 External Components and Power

#### SVX4A EXTERNAL COMPONENTS AND POWER 4/3/02

(NOTE: SVX4B should also work with these connections, but may also work equally well with fewer bypass capacitors and/or power supplies)

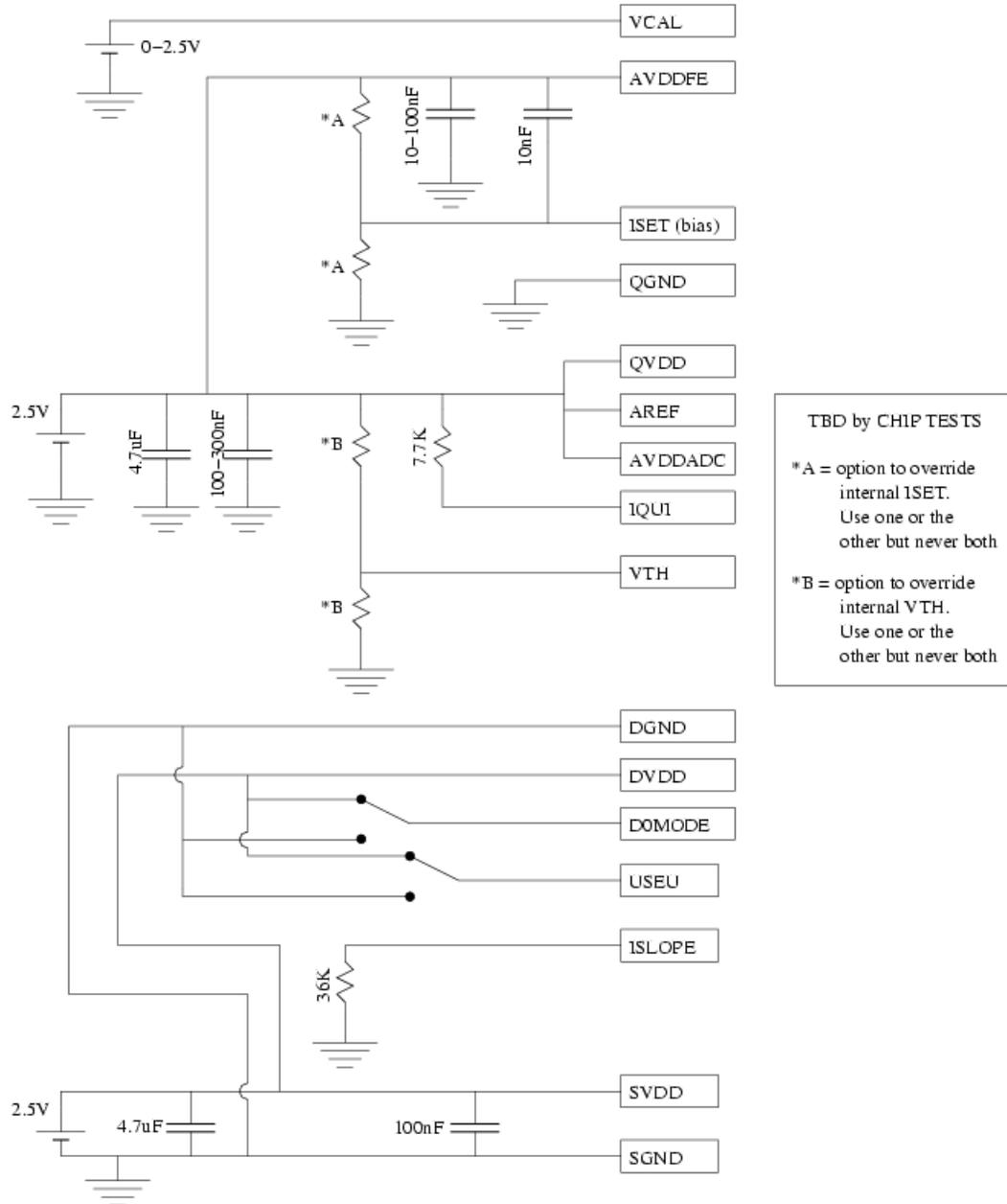


Figure 9 Diagram showing the external components that are needed for proper operation of the SVX4 chip.

### 4.3.1 ESD Protection

The ESD protection for SVX4 uses both diodes and active clamp circuits to ensure a low impedance conductive path between any two external connections on the chip in case of an ESD discharge through the chip during handling, assembly or installation. Diodes generally implement the conduction between signal pads and supply pads, while the positive supply pads themselves are actively clamped to the substrate for positive-going discharges. The clamp time-constant is  $\sim 150$  ns (designed for protection against 1.5 kV human body model discharge). Since this period is much shorter than the ramp-up rate of a decoupled system power supply, it should not interfere with normal operation.

A set of figures below depict the ESD protection scheme. Since there are no signal pads that are diode-protected to either the QVDD or SVDD power busses, the supply pads for these busses are missing a low impedance path for negative discharges relative to the substrate. Therefore, bare die could potentially be damaged by such events. This oversight should be corrected in subsequent versions.

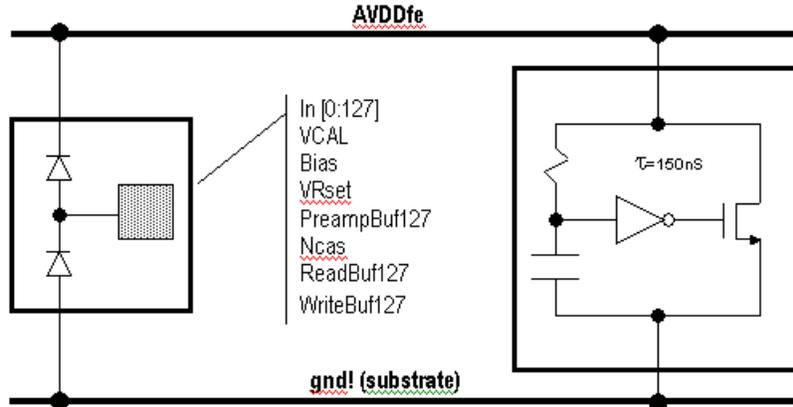


Figure 10 Front end analog power.

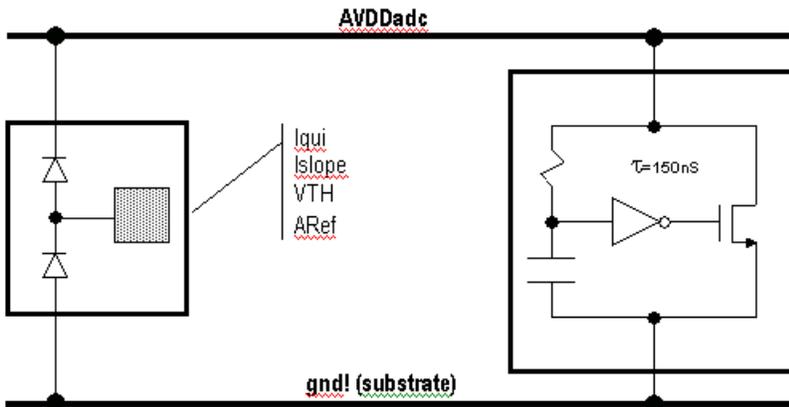


Figure 11 Pipeline QVDD power diagram.

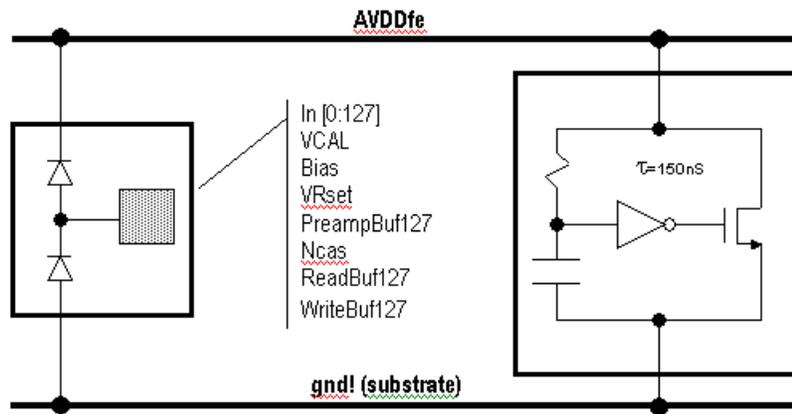


Figure 12 Back end ADC analog power diagram.

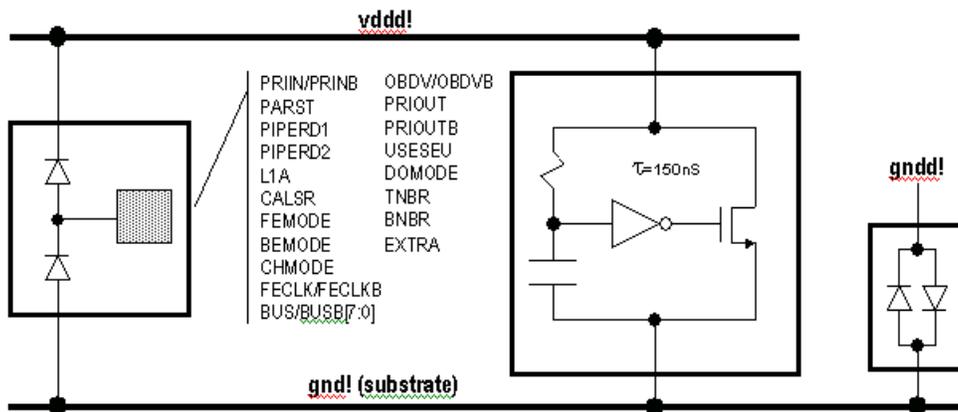


Figure 13 Digital analog power diagram.

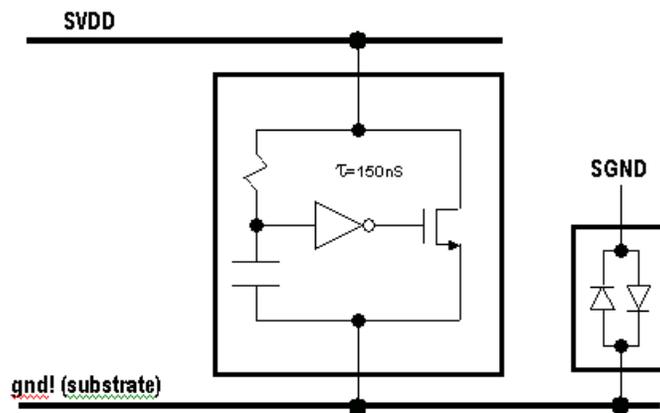


Figure 14 Output driver power diagram.

### 4.3.2 Latch up

The probability of inducing and maintaining latch-up is greatly reduced by the epitaxial layer/low-resistance substrate fabrication process used for SVX4. Theoretically, latch-up could still occur if transient voltages in excess of  $(xVDD + 0.3 \text{ v})$  or  $(xGND - 0.3 \text{ v})$  are applied to I/O pins. Such conditions could also initiate conduction of the ESD protection diodes, which could be damaged. It should be stressed that these classic latch-up trigger mechanisms, as depicted in Figure 1, are very unlikely to occur due to the low  $R_{psub}$ . It would take much more than 200 mA to induce latch-up of the NMOS devices because of the low substrate resistance. This current compliance value meets the generally accepted requirement for latch-up immunity on I/O pins. A less obvious mechanism that could lead to DVDD latch-up is described below.

There are five separate power busses on SVX4\_V1 and three on SVX4\_V2. In either case, all busses are connected to one of two supplies off-chip, AVDD/AGND or DVDD/DGND. The impedance between DGND and AGND should be kept low in order to prevent a potential difference developing between DGND and AGND ( $V_{ad}$  in Figure 2b) of more than 0.3 v, which could induce latch-up of the digital section. Such conditions could also initiate conduction of the ESD protection diodes, which could be damaged. This potential latch-up mechanism is depicted in Figure 2a below. In this case the low substrate resistance is not a factor in killing the forward bias on the parasitic NPN, which is instead dependent on external impedances. Furthermore, the typical NWELL resistance remains relatively high compared to the substrate resistance, creating the possibility for latch-up to be induced. Should this situation occur, the resulting large current conducted through  $Z_{\text{hybrid}+\text{bond}}$  would likely kill the forward bias at the parasitic NPN emitter. In any event, it is recommended that the AVDD power supply be energized before DVDD in order to avoid a transient condition that might violate the above requirement.

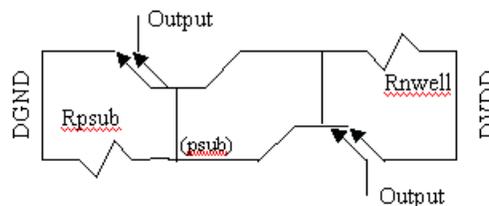


Figure 15 Classic parasitic bipolar latch up circuit.

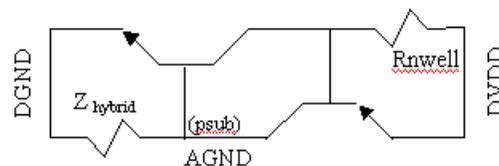


Figure 16 Dual supply latch up mechanism.

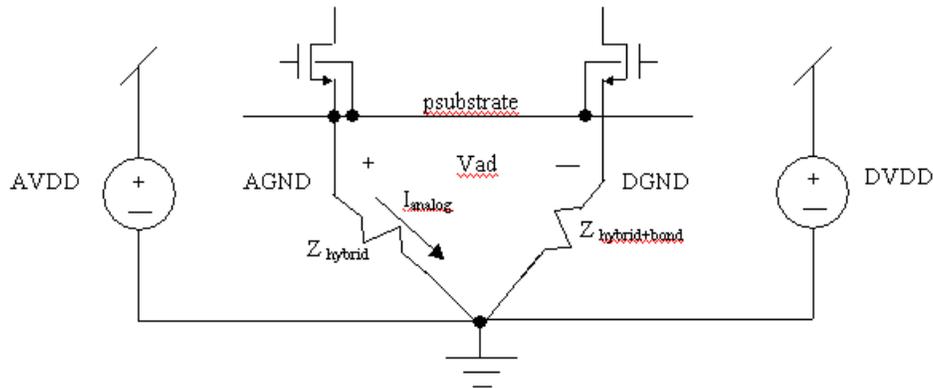


Figure 17 Equivalent circuit.

## 5 Operating the Chip

The SVX4 chip is a monolithic chip incorporating a “front-end” section and a “back-end”. In earlier versions these were on separate chips, and it is still common practice to refer to the “front-end” and “back-end” areas. Thus, the following nomenclature is used:

- BE → “BE” is for “back-end”. This area has the digitization, FIFO and readout logic.
- FE → “FE” is for “front-end”. This area has the analog amplifier, pipeline, and deadtimeless skip-logic
- Hybrid → the ceramic circuit layout that holds 2 to 10 SVX4 chips and services either r-φ side of the r-z side of the silicon sensors.

### 5.1 Guide for Single Chip Operation

- Ideally there should be one very large bypass capacitor (greater than 1 μF) per hybrid for AVDD and DVDD.
- There should be one common ground plane for the chip sets on the hybrid. An exposed section of this ground plane is where the back face of the SVX4 chip rests. The digital power feed should have its own return line, connected to the ground plane at one point per hybrid.
- IQUSCIENT should be biased with a 7.7 kΩ resistor to AVDD. ISLOPE should be biased with a kΩ resistor.
- FECLK and BECLK should be wired bonded together.

### 5.2 Guide for Daisy Chain Operation

The SVX4 is designed for daisy chained operation to minimize the number of bus and control lines required to operate the device. Fewer control lines means less space on the high density interconnect and less mass in the system. A group of daisy chained chips is shown in Figure 18. All the chips share a common communication bus (BUS0-7) and a common differential clock (FE-CLK, BE-CLK).

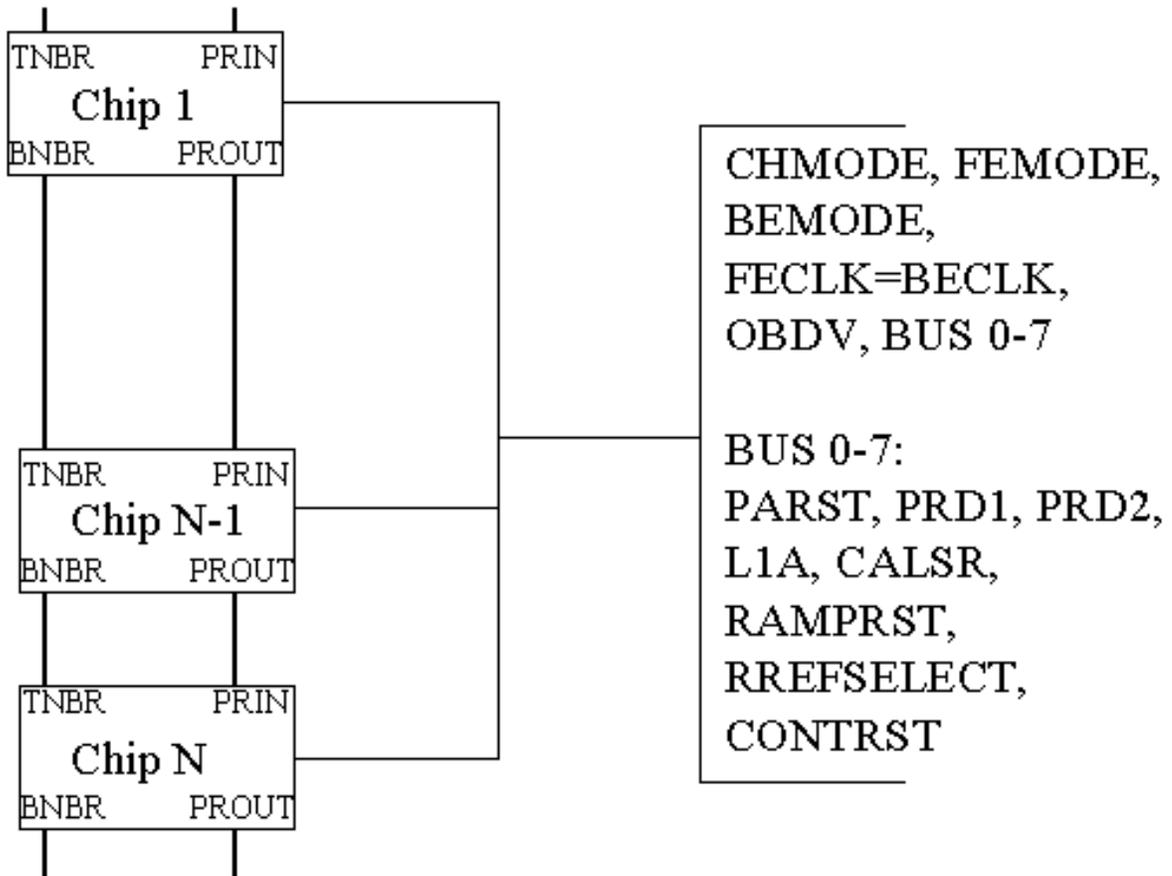


Figure 18 Daisy chained readout chips.

In addition, each chip has two pads call TNBR and BNBR which are used for communication between adjoining chips. After powering up the SVX4, the chip parameters listed in Section 3 must be downloaded before useful operation of the readout chips can begin. For each SVX4 chip, 198 bits must be downloaded into internal registers. In the Initialization Cycle, the signal lines PRIIN and PRIOU are used as a serial data link to form a very long shift register for downloading parameters to the string of daisy chained SVX4s. Parameters for each chips are loaded in sequential order with the data for chip 1 loaded first via PRIOU on the last chip of the daisy chain. Data is clocked between cells in the shift register using the common differential clock pads. If there were 10 chips, exactly 1980 bits would have to be downloaded in the Initialize Cycle. Downloaded parameters may be checked by shifting the bits out through PRIIN of the first chip while reloading the chips with the same data. To identify each chip in the daisy chain, a separate chip ID number (bits - ) is downloaded into each chip during the Initialize Cycle. The seven bit chip ID number allows chips to be tagged with numbers from 0 to 127.

In Acquire Cycle, the Bus 0-7 and clock pads provide simultaneous real time control of all the chips in the daisy chain. PRININ, PRIOUT, TNBR, and BNBR have no function in Acquire Cycle.

In Digitize Cycle, the Bus -0-7 and differential clock pads provide real time control of all the chips in the daisy chain. The TNBR and BNBR pads are used only in READ NEIGHBOR mode to notify the corresponding chip to read out the extrema strip. The pads PRIIN and PRIOUT are used to pass a token in between chips to control when each chip should put data onto the bus and when readout is complete.

In Readout Cycle, the Bus 0-7 lines are changes from input lines to output lines. During readout, data from each SVX4 chip is placed on the common bus beginning with the top chip in the daisy chain and proceeding sequentially through the remaining chips. Information is placed on the bus in 8 bit bytes. First the chip ID and then the pipeline cell is read out. Then the address and data information for that chip is read out beginning with the channel nearest the top of the chip, channel 1, and proceeding downward. Priority for the output is passed from the PRIOUT of the first chip to the PRIIN pad of the next chip after the first chip has been completely readout. The top chip will have PRIIN first since the PRIIN pad is internally pulled weakly low to initiate readout. Information is readout using both the high and low transitions of the differential clock. Thus, the channel readout rate is approximately equal to the BECLK clock frequency.

## 6 Measuring the Performance of the SVX4

This section explores the subtleties of determining the bandwidth and choosing the best setting. It begins with a discussion of expectations of bandwidths, integration time, and setting the bandwidth. Effects of external capacitive load are examined and use of the calibration voltage and gain measurements to obtain a standard for presenting results follows. After this discussion there are warnings about testing with unloaded channels, a likely event when one is just looking at a chip on a hybrid, as well as robustness of the measurement including a word on common mode and control using differential noise measurements. A final word of warning on comparing the results to simulation concludes this section.

## 7 Miscellaneous Considerations

## 8 Appendix A

### 8.1 Measurements of Timing on Various Test Stands

#### 8.1.1 Systems in use

- **The Stimulus Test Stand.** This system is based on a general pattern generator that is quite expensive and rather delicate to program. It is however an off-the-shelf item. It has not been setup in any triggerable manner.
- **The Stand Alone Test Chain.** This used the full test chain for DØ.

- **The PATT Test Stand.** This test stand was used at LBL and the wafer probing station. It uses a text file to download the initialization stream.

## 8.2 Measurements of the Basic Sequence

Analysis of the basic sequence of signals going to and coming from the SVX4 involves studying the Digitization and Readout Cycles while Acquisition is occurring. Items of interest to observer are the changes that occur at each of the cycle boundaries, the acceptance of a trigger and its handling, and the return of the pipeline cell after readout. For the systems that do not run continuous sequences, it is useful to examine the start and end of the sequence chain and to compare the state of the various lines before the start and after the end of a sequence burst.

This suggests the following measurements be made:

- **Basic Clock Rate.** A measurement of the clock speed used to drive the sequence of signals going to/coming from the chip is useful in each of the systems. Systems may be able to only change states at a one-half their basic clock rates. This has consequences for the rate at which the FECLK or BECLK may be run in comparison to basic clock rate.
- **Full Sequence.** A snapshot of the full sequence starting with the beginning of the burst of signals going to the SVX4 and ending with the end of the burst gives an overview of which lines make transitions at which points. Detailed timing relationships cannot be easily observed.
- **Preamp Reset.** The reset of the preamp should occur between bunches. This is handled differently on various systems and may affect the results they produce. Measurements of where these transitions occurs have been made.
- **Start of Sequence.** The disposition of the various signal lines at the start of the sequence is relevant for systems that do not run continuously.
- **Level 1 Accept.** The level 1 accept causes the pipeline cell to be put aside.
- **Digitization.** Resetting of the Wilkinson ramp, the counter, the threshold comparators and the interaction with the PRD1 signals which place the pedestal and then the signal capacitor in place for measurement are critical portions of the SVX4 operation and are hence interesting to measure.
- **End of Digitization.** The signaling of the end of the digitization and the observation of the operation of the top and bottom neighbor logic in action are interesting to document.
- **End of Digitization/Beginning of Readout.** The transition from the end of the digitization to the readout, noting the modification of the BEMODE line over this boundary is of interest to document.
- **Beginning of Readout.** Examination of the data lines and correlation of the data with that which are eventually seen in computer memory of the device used to store that data are interesting to study.
- **End of Readout.** The final data words, together with observation of how the data stream to the computer is terminated, are correlated with the data as they appear on the computer.

- **End of Sequence.** The end of the commands sent to the chip for systems which send only bursts of sequences are useful measurements so that the quiescent state of the lines between bursts can be studied.

### **8.3 The D0 Sequence**

The following pictures show the simulation waveforms that were used to test the schematic level design of the SVX4. Both D0 and CDF agreed to choose waveforms that would test most of the features of the SVX4 and to be complementary to each other. One waveform testing one set of features and the other waveform testing orthogonal features.

The parameters used for the D0 sequence were as follows:

- Injection mask : 125 injected on only
- Mask disable is off
- Bandwidth settings: 0000
- Bias controls: 0010
- Trigger latency: 13
- Pipeline readout order: signal cell first, then pedestal cell 47
- Chip id: 0
- DPS setting: on
- Channel 127 readout: not read out
- Channel 63 readout: read out
- Sparsify mode: on
- Read neighbors: on
- Ramp pedestal: 0000
- Ramp direction, comparator polarity: both 0
- Ramp range: 000
- Threshold: 20
- Counter modulo: 255

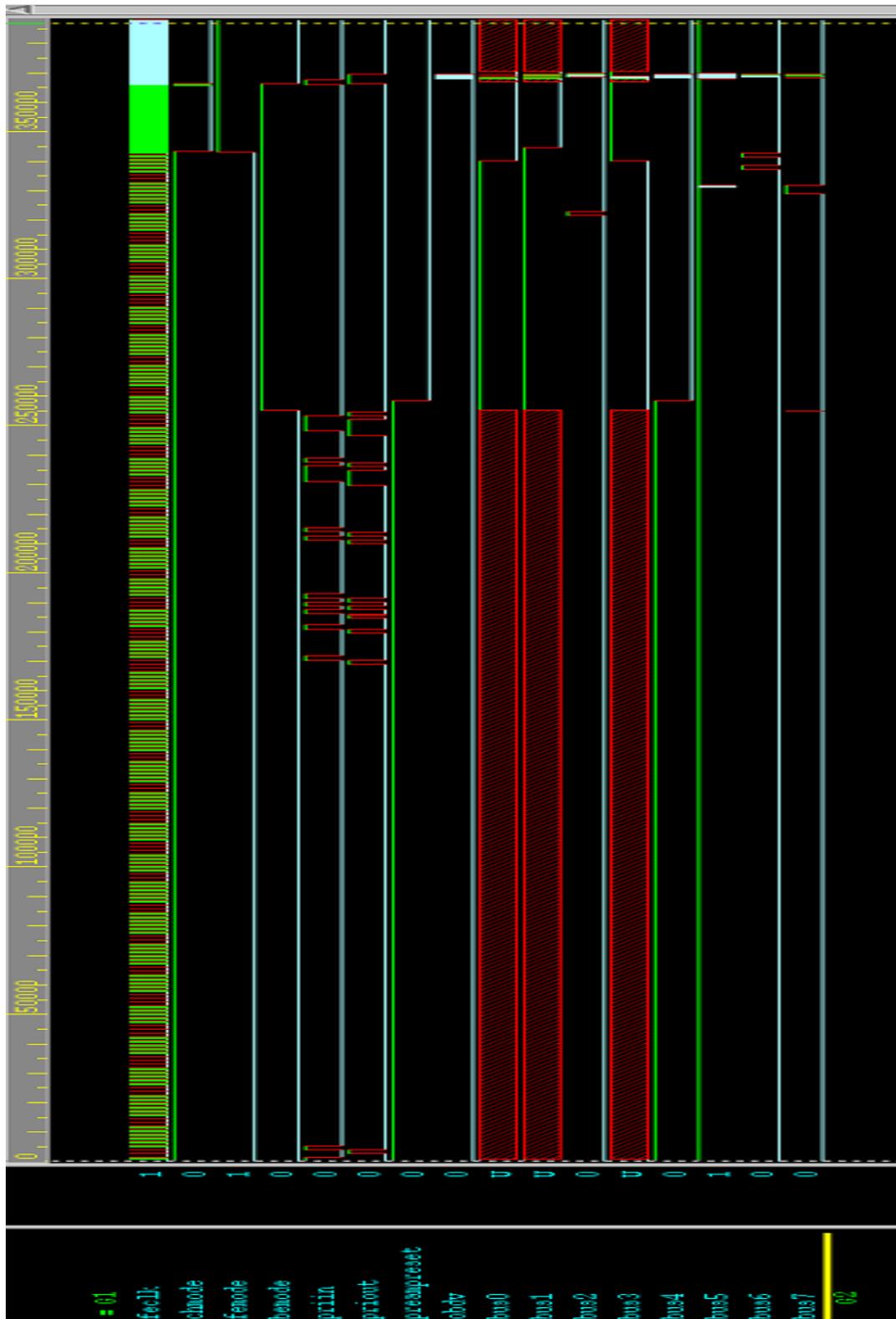


Figure 19 The full D0 waveform using a sparsified setting for readout.

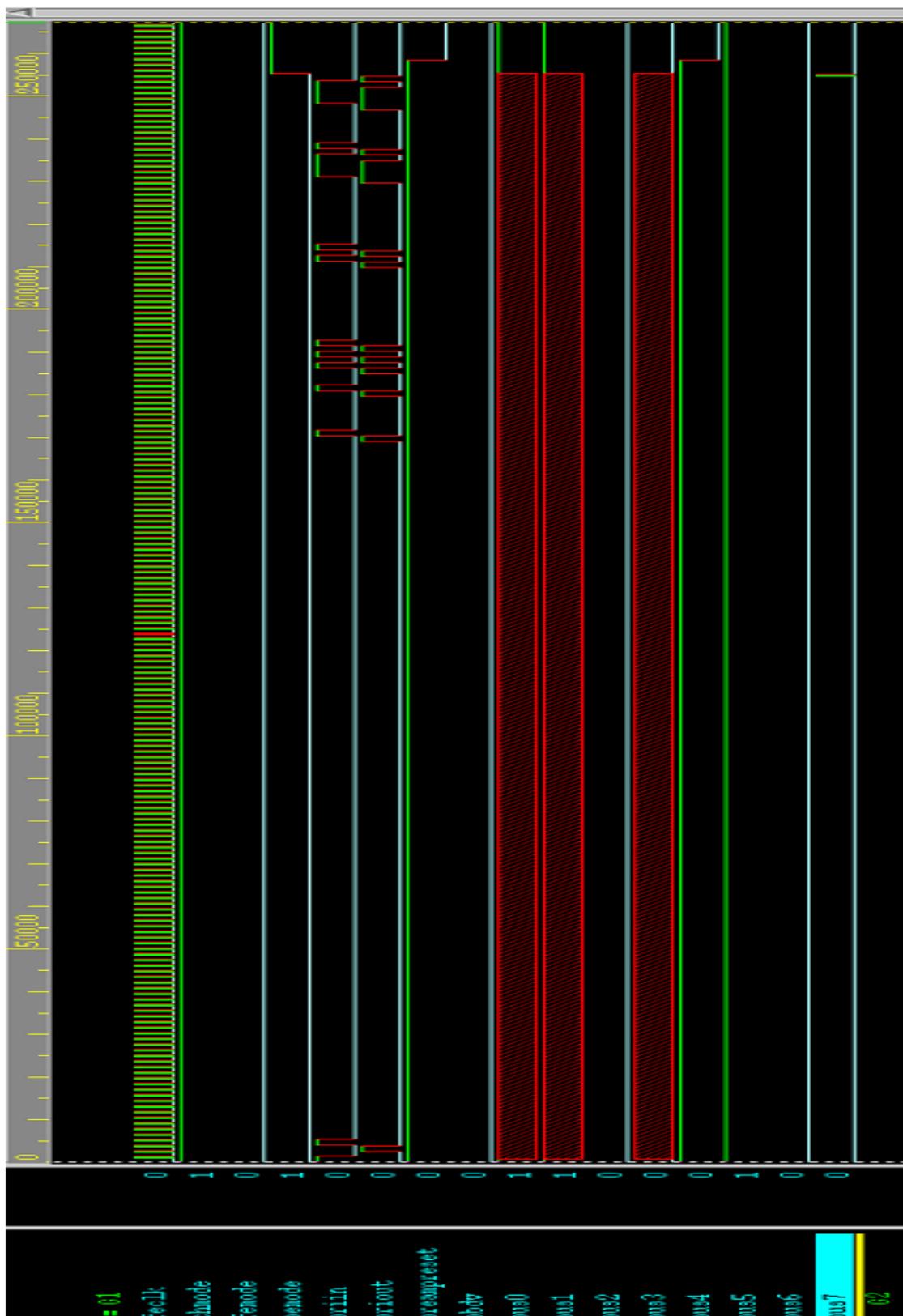


Figure 20 The initialization sequence for D0.

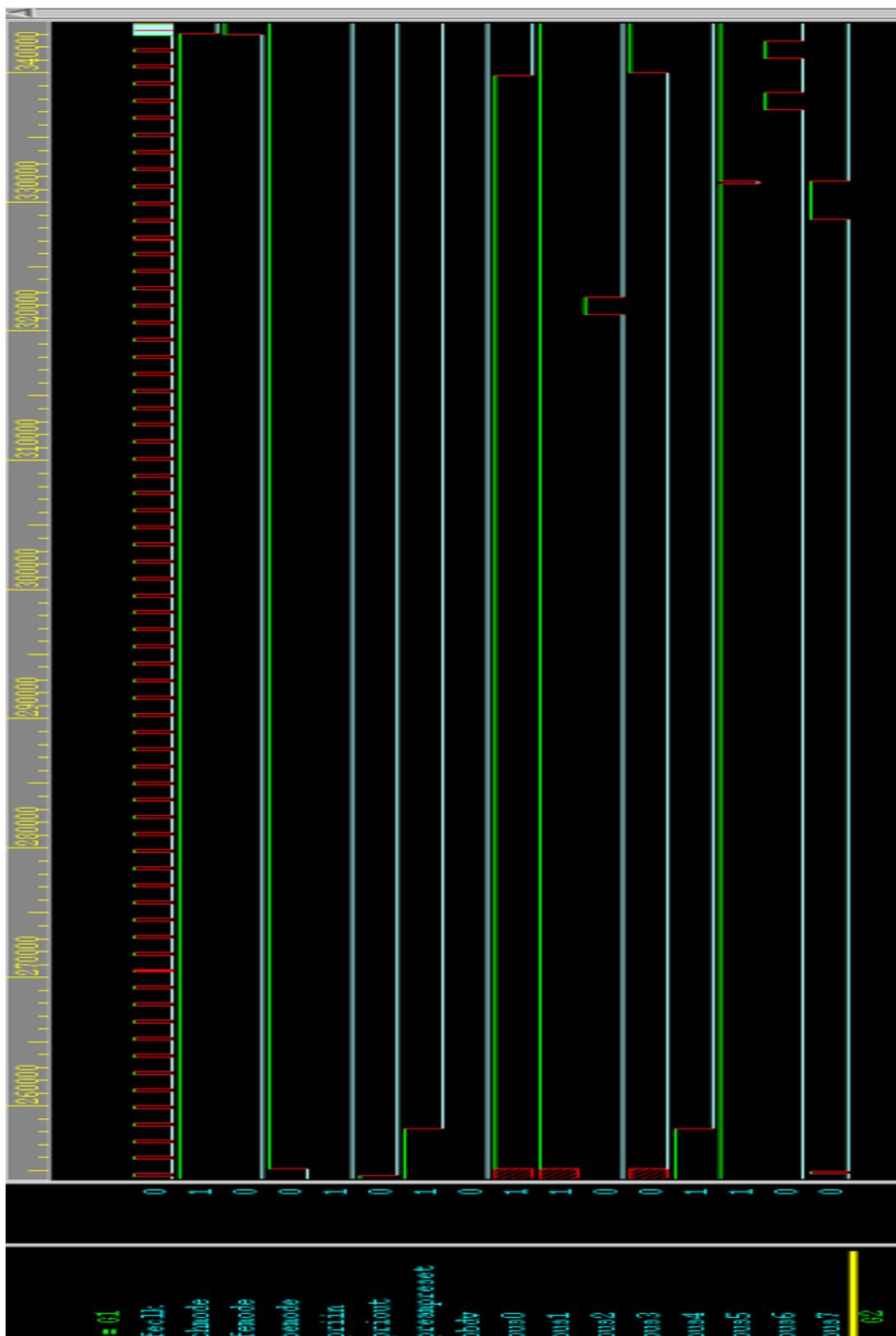


Figure 21 An enlargement of the setup sequence in the front-end in D0mode.

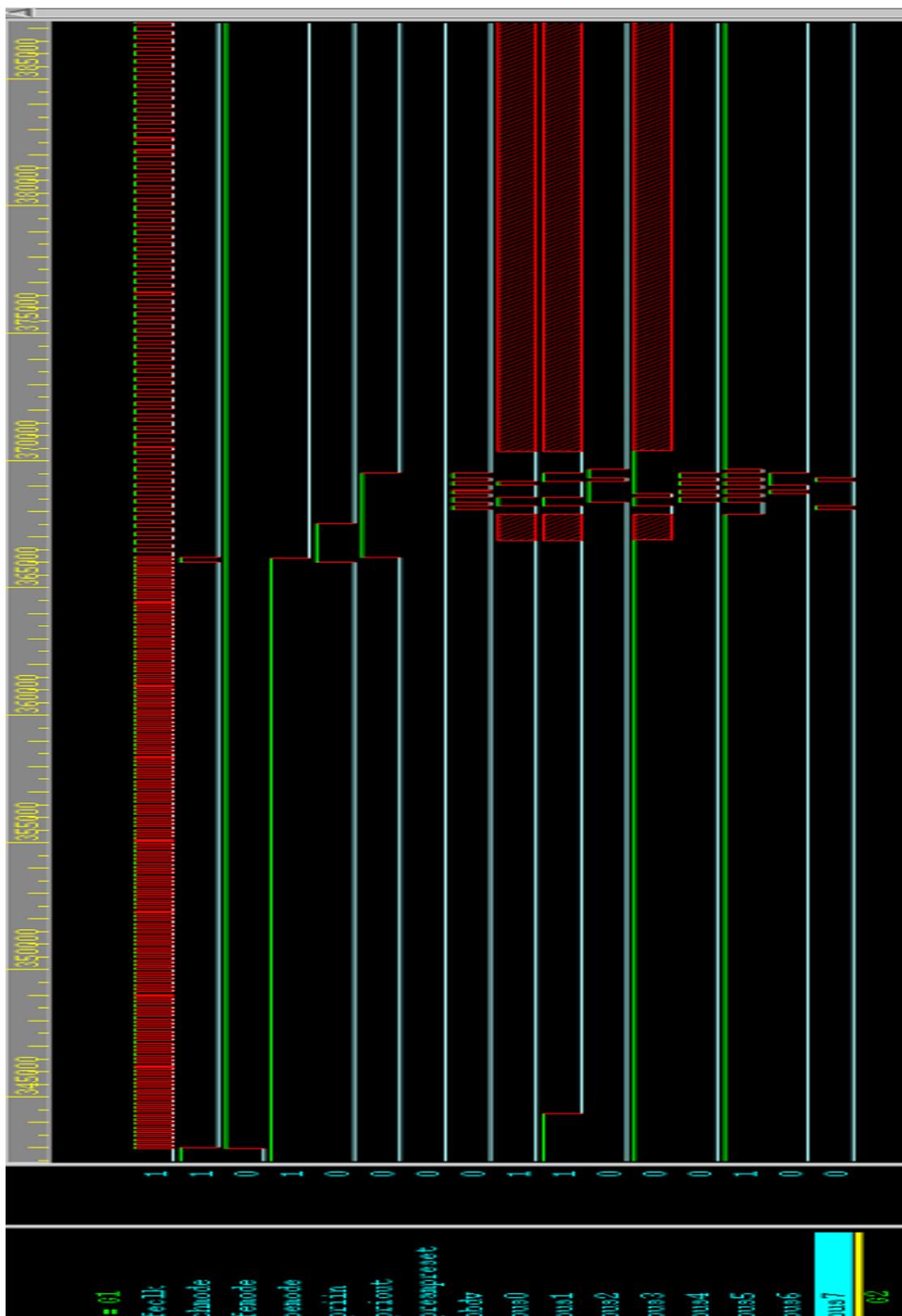


Figure 22 A enlargement of the digitization and readout in sparsify mode for D0.

## 8.4 The CDF Sequence

The following pictures show the simulation waveforms that were used to test the schematic level design of the SVX4. Both D0 and CDF agreed to choose waveforms that would test most of the features of the SVX4 and to be complementary to each other. One waveform testing one set of features and the other waveform testing orthogonal features.

The parameters used for the D0 sequence were as follows:

- Injection mask : every 8<sup>th</sup> channel
- Mask disable is off
- Bandwidth settings: 1000
- Bias controls: 0010
- Trigger latency: 5
- Pipeline readout order: signal cell first, then pedestal cell 47
- Chip id: 24
- DPS setting: off
- Channel 127 readout: read out
- Channel 63 readout: not read out
- Sparsify mode: on
- Read neighbors: off
- Ramp pedestal: 1000
- Ramp direction, comparator polarity: both 0
- Ramp range: 000
- Threshold: 150
- Counter modulo: 240

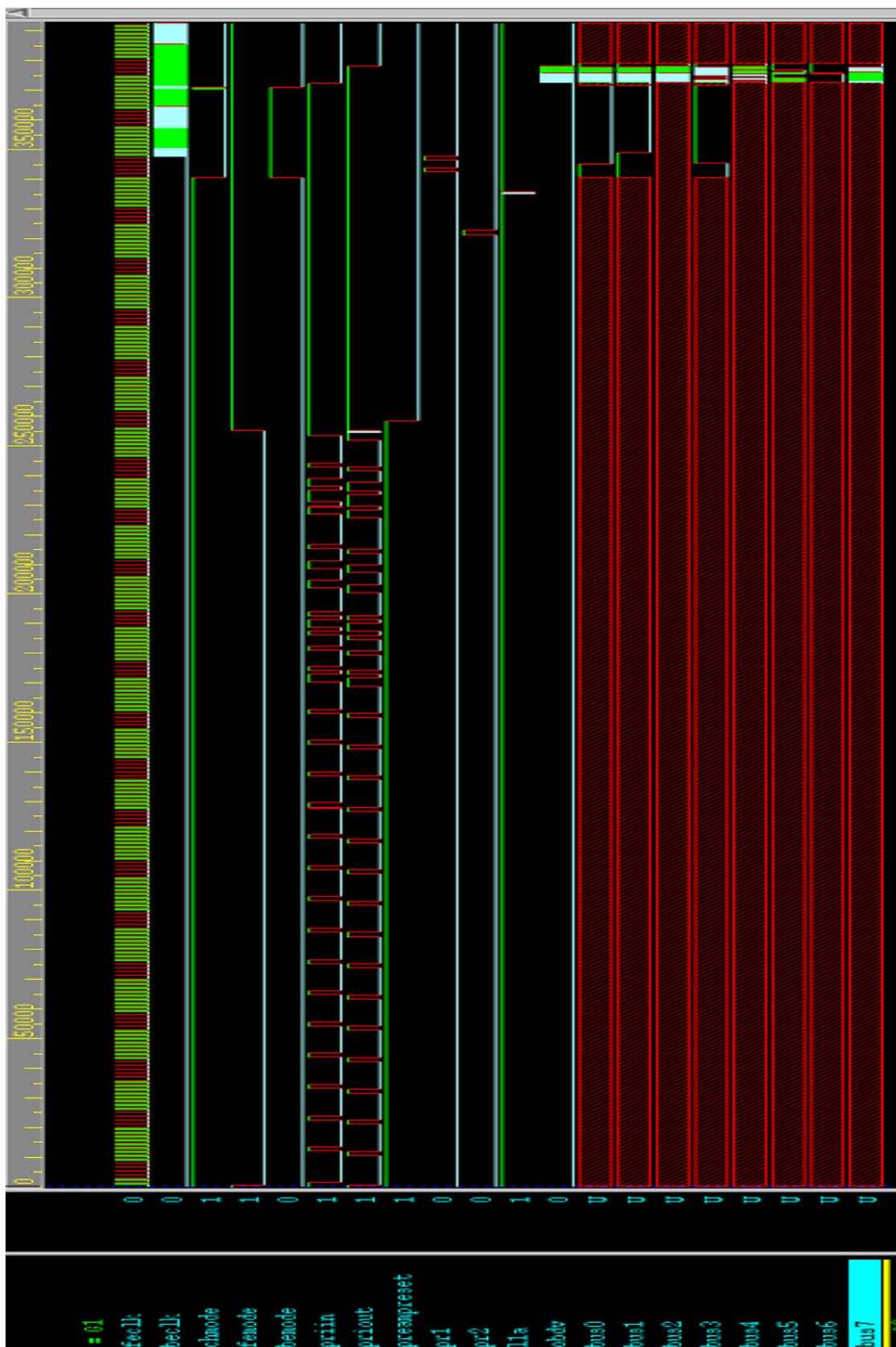


Figure 23 The full CDF sequence in sparsify mode.

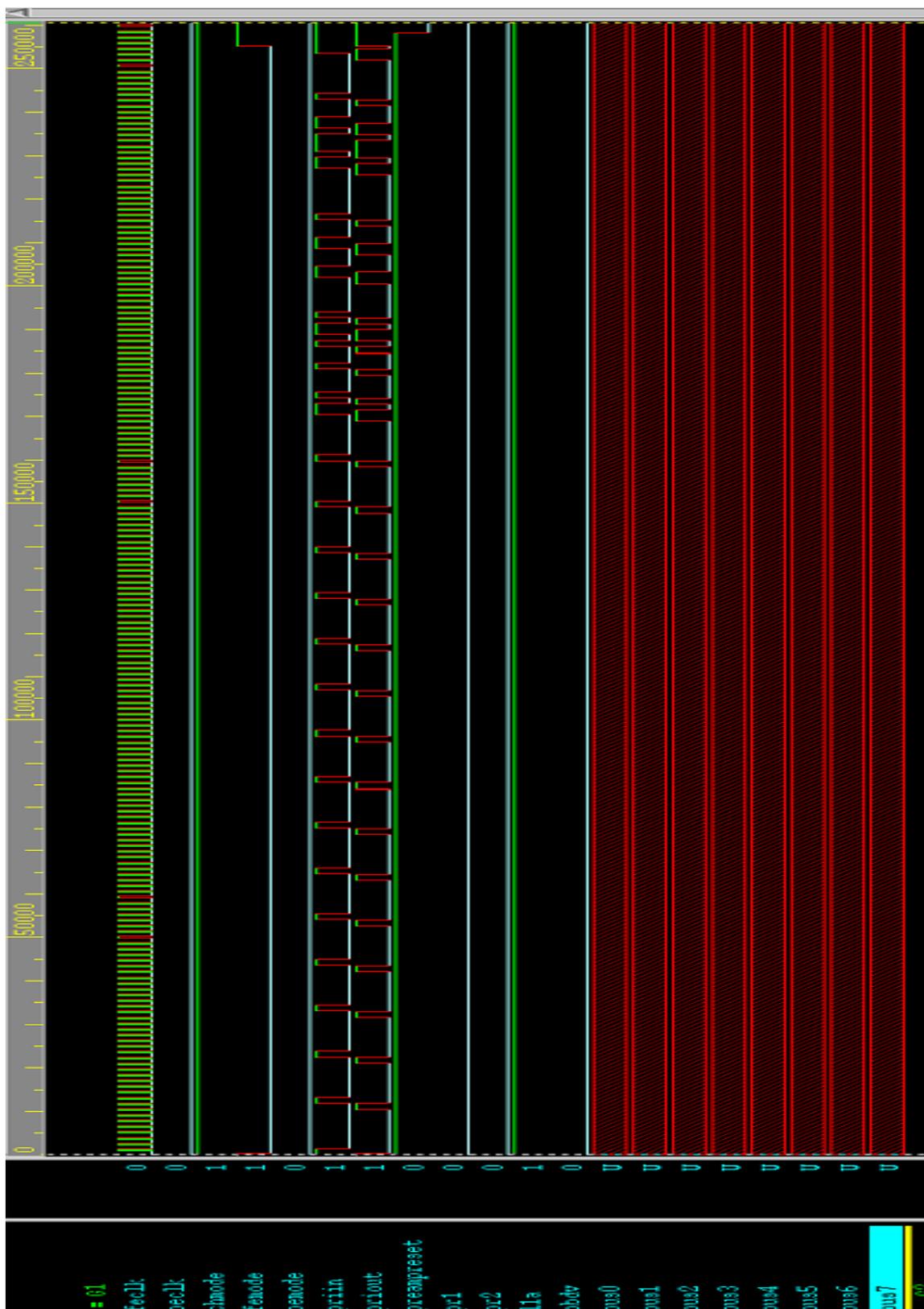


Figure 24 The initialization sequence for CDF mode.

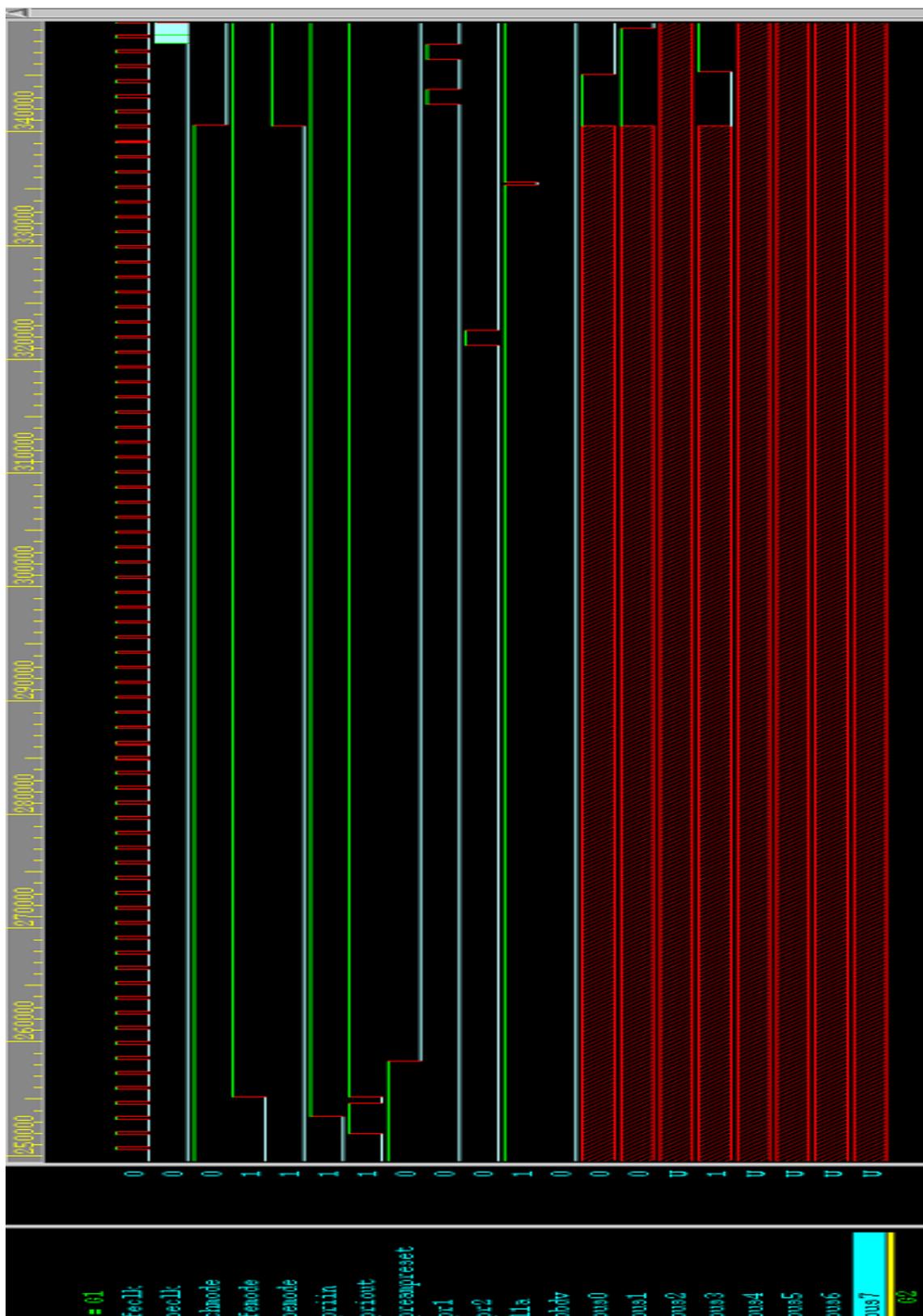


Figure 25 The acquire waveform for CDF.

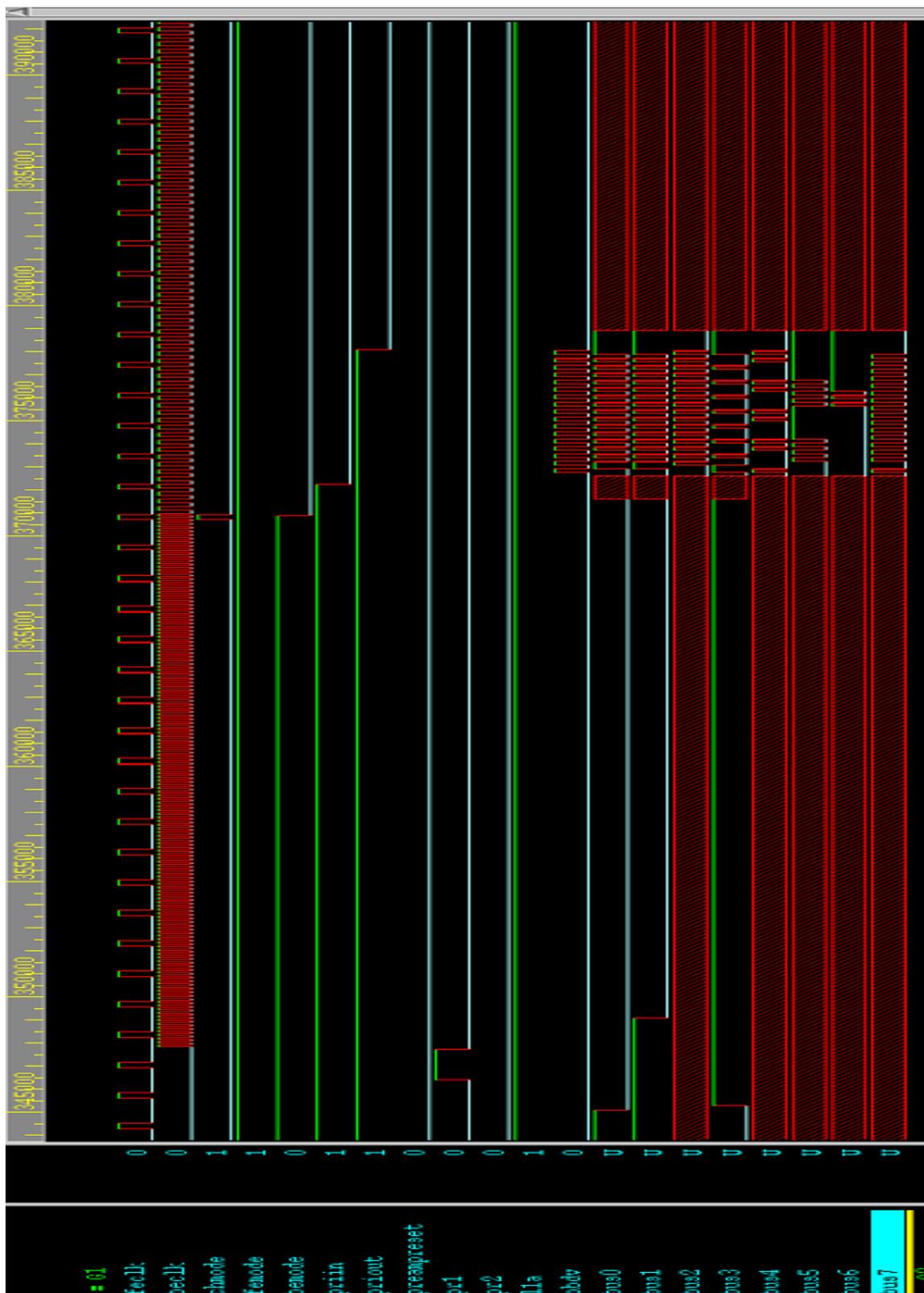


Figure 26 Digitization and readout for CDF mode.

## 9 The SVX4 Specifications

### A. General:

1. Input bonding pad pitch: 48 $\mu$ m
2. Overall Width: 6.250mm active area. Dicing streets as close as allowed by design rules.
3. Overall length: < 11.925mm
4. Supply voltages: 2.25-2.75V analog, 2.25-2.75V digital.
5. Versions: A version is the basic "conservative" version.  
B version adds on-chip bypassing and front to back combined power routing,
6. Bond pad layout: Both version have same bond pad layout with some pads used only by CDF and others used only by D0.
7. Bond pads: Except Front End inputs, no wirebond pad is to be smaller than 150x150um (cover layer opening). Probe pads not meant for wirebonding are exempt.
8. Maximum Supply Voltage: 3.5V

### B. Preamp:

1. Input pulse polarity: Positive
2. Gain (feedback capacitor): 3mV/fC
3. Gain uniformity (ch-to-ch): 5% or better
4. External load capacitance: 10pF to 50pF
5. Risetime 0-90%: adjustable in a range that includes 60-100ns  
for any allowed load
6. Risetime adjustment: 4 bits minimum
7. Noise (ENC): 2000e or less for a 40pF load using double correlated sampling with 100ns integration t.
8. DC open loop gain: >2500 (>95% charge collection from 40pF)
9. Linearity: Linear response for pulses up to 20fC non-linearity < 0.25mV at output >200fC
10. Dynamic range: >200fC
11. Reset + settling time: <1 $\mu$ s for any initial condition
12. Reset offset voltage: Internally set to a value TBD by designers, with external override capability.
13. Input protection diodes: 2uA DC capability to either rail. Current must not go to substrate.
14. Calibration injection: 40fF internal cap switched to input
15. Calibration charge control: 1 external analog reference voltage

- (other voltage is AVDD, not ground)
17. Input disable switch: control of calibration mask switch is disabled
18. Input Device Current: in SVX3
19. Bypass capacitors: maintained closer than
- 2 Config. Register bits. #1 disables reset switch for channel with bit set. #2 determines whether reset always closed or always open for channels.
- Adjustable with configuration bits as but with wider range (factor of 2). Performance in SVX-II mode should be with no external bypass capacitors 10mm.

#### C. Pipeline:

1. Input Pulse polarity: Negative
2. Voltage gain: 3 to 5
3. Gain uniformity: 5% channel to channel
4. Risetime, 0-90%: 10ns to 40ns (in that range, fixed)
5. Noise (ENC at preamp input) <500e
6. Linearity: linear response up to 20fC at preamp input
7. Dynamic Range: To Be Confirmed: >40fC at preamp input
8. Reset Time: <20ns for any allowed initial condition
9. Pedestal uniformity: channel to channel <500e at preamp input channel to <1000e at preamp input cell to cell
10. Bias: Internally set with override bonding pad.

#### D. ADC:

1. Type: Wilkinson with real time pedestal subtraction.
2. Voltage Ramp: Rate adjustable with external resistor.
3. Ramp rate "trim" bits: 3 Bits, adding binary weighted capacitors to the op-amp feedback. Largest capacitor is 4x the fixed feedback capacitor. These capacitors provide a range adjustment- no fine adjustment needed.
4. Ramp Linearity: 0.25% for rates between 0.1 and 1 V/us.
5. Ramp dynamic range: 1V
6. Ramp pedestal: Same as in SVX3.
7. Counter: 8-bit Gray code, 106MHz rate.

8. Differential nonlinearity: <0.5 LSB.  
 9. Bias: Internally set with override bonding pad

E. Data output drivers:

1. Type: Complementary with "resistor current sources"  
 2. Current source range: 2.5mA to 17.5mA in 2.5mA steps (3 bit adjust).  
 3. Rise and fall times: >2ns and <4ns with nominal load.  
 4. Common mode: VDD/2 nominal with T termination.  
 5. Load capability: 70ohm and 20pF.  
 7. Tri-state: Outputs tristated in initialize (except if SR copy pad is bonded- see H7) and digitize modes.  
 8. Single ended use: No additional requirements  
 9. Bi-directional: All Bus pads will be bi-directional. Only some will be used of input as well as output by CDF, but all of them will be I/O for D0.  
 10. Output data skew: >3ns between OBDV and any bus line and between any two bus lines.

F. TN/BN Pins:

1. Functions TN/BN pads The multiplexed functions of the SVX3 will be separated in SVX4 to TN/BN and Priority in/out dedicated sets of pads.  
 2. Type, BN/TN: "Open collector" I/O with internal pull-up.  
 3. Type, Priority in: Differential receiver (2 bond pads) same as clock receivers, with added high Z common mode reference voltage (center tap of large resistance between power and ground).  
 4. Type, Priority out: Differential driver (2 bond pads) same as data bus outputs.  
 5. BN/TN Internal pull-up: >500 ohm  
 6. BN/TN Pull-down current: >10mA  
 7. BN/TN Modes: only active in digitize mode  
 8. Priority in/out Modes: Configuration register input/output during initialize mode. Priority passing during readout mode. Priority out high during digitize mode.

9. Bonding pads: This increases the number of bonding pads per chip by 4 (2 next to TN and 2 next to BN).

#### G. Configuration Register:

1. Type: Bit serial shift register.  
 2. Cell type: SEU tolerant shadow register.  
 3. Shadow register: Keep for SEU tolerance.  
 4. Clock: Register advanced with FE clock in initialize mode.  
 5. Length: no limit.  
 6. Preset: no preset.  
 7. layout rule: Do not place configuration register cells within 75um of a wirebond pad (they tend to be destroyed by missed wirebonds).  
 8. Bit order: LSB loads first on all fields.  
 9. Bit Assignment: Numbers are for illustration. Designers may add bias adjust or other system bits as needed.

0-127: Calibration Mask  
 128: Cal-inject signal polarity  
 129: Input disable  
 130: Disable mode (reset always on or off)  
 140-144: Bandwidth bits (left room for 5)  
 145-147: Input transistor current  
 148-153: Pipeline depth  
 154: Pipeline readout order  
 155-161: Chip ID  
 162: Real time pedestal subtraction  
 Enable  
 163: Last channel latch  
 164: Channel 63 latch  
 165: Read all  
 166: Read Neighbors  
 167-170: Ramp pedestal  
 171: Ramp direction  
 172: Comparator polarity  
 173-175: Ramp range selection  
 176-183: Sparsification threshold  
 184-191: Counter Modulo  
 192: First chip flag (see H.9)  
 193: Last chip flag (see H.9)  
 192-194: Output driver resistor select

#### H. Control Functions:

(\*) Denotes desirable feature but not strictly required

1. Signal Functions: All control signals same function as SVX3 except as noted here.

- 2. Ramp and Counter Reset: Remove Counter Reset as an independent signal. In normal mode Counter Reset is to be tied to Ramp Reset. In Dynamic Pedestal Subtraction mode Counter Reset is internally generated as in SVX3.
- 3. Preamp Reset & Fe Clock: Preamp Reset should always function independently of FE Clock state. In SVX3 Preamp Reset can only go high while FE Clock is high.
- 4. PRD2 (\*): It is desirable that PRD2 control only the acquisition of the reference capacitor pedestal, and that the action of returning a cell to the pipeline be automatically triggered by the end of digitization (The falling edge of DIGITIZE MODE is used to drive the MOVE DATA pipeline input)
- 5. Last channel SR bit: on=always latch chan. 127 (same "last chip flag" in SVX3).
- 6. Chan. 63 latch SR bit (\*): on=always latch chan. 63 (doubles read out speed)
- 7. Bus 3 SR copy bond pad: copy Priority out in initialize mode to Bus 3 output if pad is bonded to ground (and enable output bus in init. mode)
- 8. extra L1A: Additional L1A pulses (beyond 4) should be ignored by the pipeline logic.
- 9. OBDV (data valid) control (\*): OBDV must be driven by 1 chip per daisy chain at all times to prevent data transmission errors. This can be accomplished in SVX4 with 2 configuration register bits: First Chip (FC) and Last Chip (Different from item 5). OBDV control is given by the following logic table

Pri. In	Pri. Out	FC	LC	OBDV
H	H	L	L	
	disabled			
H	L	L	L	
	disabled			
L	H	L	L	
	ENABLED			
L	L	L	L	
	disabled*			
X	H	H	L	
	ENABLED			

X	L	H	L
	disabled*		
H	X	L	H
	disabled		
L	X	L	H
	ENABLED		

\*OBDV is to be disabled one BE\_CLOCK cycle after Pri. Out is lowered (same as in SVX3). [In the present CDF silicon system it was necessary to add logic to the port cards to implement this function, because the SVX3 does not have the FC and LC bits.]

10. Readout Mode Pad:

Add an output pad to make the "Readout Mode" internal signal available

11. D0 Mode pad:

A special bond pad, if left un-bonded will set the chip in D0 mode. This will multiplex I/O signals onto all Bus lines and gate the Pipeline Clock off during digitize and readout operations.

12. Test outputs:  
one

Buffered preamp and pipeline outputs for one channel, Comparator output for 1 channel, Ramp probe point, RTPS comparator

buffered input

And output- all as in SVX3. Additional

probe

points as needed to fully test

performance.

<sup>i</sup> S. Kleinfelder, *et. al.*, "A Flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout." IEEE Transactions on Nuclear Science, Vol. 35, No. 1, February 1988, pp. 171-175.

<sup>ii</sup> S. Kleinfelder, "The LBL Silicon Vertex Detector Readout Integrated Circuit: An Introduction." Lawrence Berkeley Laboratory, November 16, 1986.

<sup>iii</sup> T. Zimmerman, *et. al.*, "Design of an Advanced Readout Chip for Silicon Strip Detectors." IEEE Transactions on Nuclear Science, Vol. 40, No. 4, August 1993, pp. 736-739.

<sup>iv</sup> T. Zimmerman, *et. al.*, "SVXII Analog Pipeline Signals and Operation." Fermi National Accelerator Laboratory, April 4, 1993.

<sup>v</sup> T. Zimmerman, "SVX3: A Deadtimeless Readout Chip for Silicon Strip Detectors: The Use of Low Resistivity Substrates for Optimal Noise Reduction, Ground Referencing, and Current Conduction in Mixed Signal ASICs." Fermilab TM, TM-2035.

<sup>vi</sup> T. Zimmerman, *et. al.*, "SVX3: A Deadtimeless Readout Chip for Silicon Strip Detectors," Nuclear Instruments and Methods in Physics Research, A 409 (1998) 369-374.