

Status



■ ADC analysis

- Study of the ch-ch variation was completed on schedule on 10/23
- Study of the bow scheduled for 11/13

■ Backend

- Started set list of digital modifications to FIFO and IO cells on time
- After 2 weeks, all layout modifications are done
- LVS of FIFO passed, LVS of IO passed
- Verification to be completed:
 - LVS/DRC of digital core
 - Run verilog test vectors on digital core
- Looks good for completing digital work on schedule next week

Review fix list



■ Fix list

- Previously Agreed Upon (completed items checked)
 - ✓ 0) choose SVX4_V2 as the basic design
 - ✓ 1) add pullup or pulldown on D0Mode (this is now a pulldown)
 - ✓ 2) add pullup on USESEU
 - ✓ 3) pullup bit7 of chipid
 - ✓ 4) pulldown bit 6&7 of cellid
 - ✓ 5) hardwire PRIOUT driver strength bits
 - ✓ 9) change ADC control signal latching scheme to (not(readout))
 - 12) add 2 bits to SR
 - 13) add VCAL switch
 - 14) add on-chip decoupling caps to BIAS (desired, but not crucial?)
- TBD:
 - 10) layout/design change for ADC pedestal variation(?)
 - 11) pipe cell pedestal variation (?)
 - 15) ADC comparator design
 - 16) Receiver (?)

Versions



- A 2-version submission has been generally accepted to this point
 - To make this strategy truly effective, I suggest the following recipe:

- Version 4.2a—*minimum changes, “back-up solution”*
 - 1) add pullup or pulldown on D0Mode
 - 2) add pullup on USESEU
 - 3) pullup bit7 of chipid
 - 4) pulldown bit 6&7 of cellid
 - 5) hardwire PRIOUT driver strength bits
 - 9) change ADC control signal latching scheme to not(readout)
 - 12) add 2 bits to SR
 - 13) add VCAL switch
 - 15) ADC comparator design LEVEL I—LBL changes in bias circuit, comprst driver

- Version 4.2b—*better performance, planned “pre-production” chip*
 - Same as 4.2a, but:
 - 11) pipe cell pedestal variation—widen metal lines
 - 14) add on-chip decoupling caps to BIAS
 - 15) ADC comparator design LEVEL II—FNAL changes in bias, output stage, input caps, local comprst buffer, for better performance

Outlook



- Based on the 4.2a/4.2b proposal, at this time it looks like:
 - 4.2a
 - Backend digital done next week [(1)-(9) + (12), *Brad*]
 - ADC bow study Nov 13-20 [*Brad*]
 - Frontend and LBL ADC changes done by Nov 27th [(15), *Brad*]
 - 4.2b
 - Insert FNAL ADC Nov 27th [(15), *Tom*]
 - Insert BIAS caps and pipeline metal Nov 27th [(11) + (14), *Tom*]
- Both versions:
 - Incorporate receiver fix (?) Dec 2nd [(16), *Jim Hoff*]
 - Fullchip sim and ADC Monte-Carlo sim starts Dec 2nd [*Brad*]
 - 1-month verification starts Dec 12th, on-schedule [*Brad*]