SVX4 Chip Test

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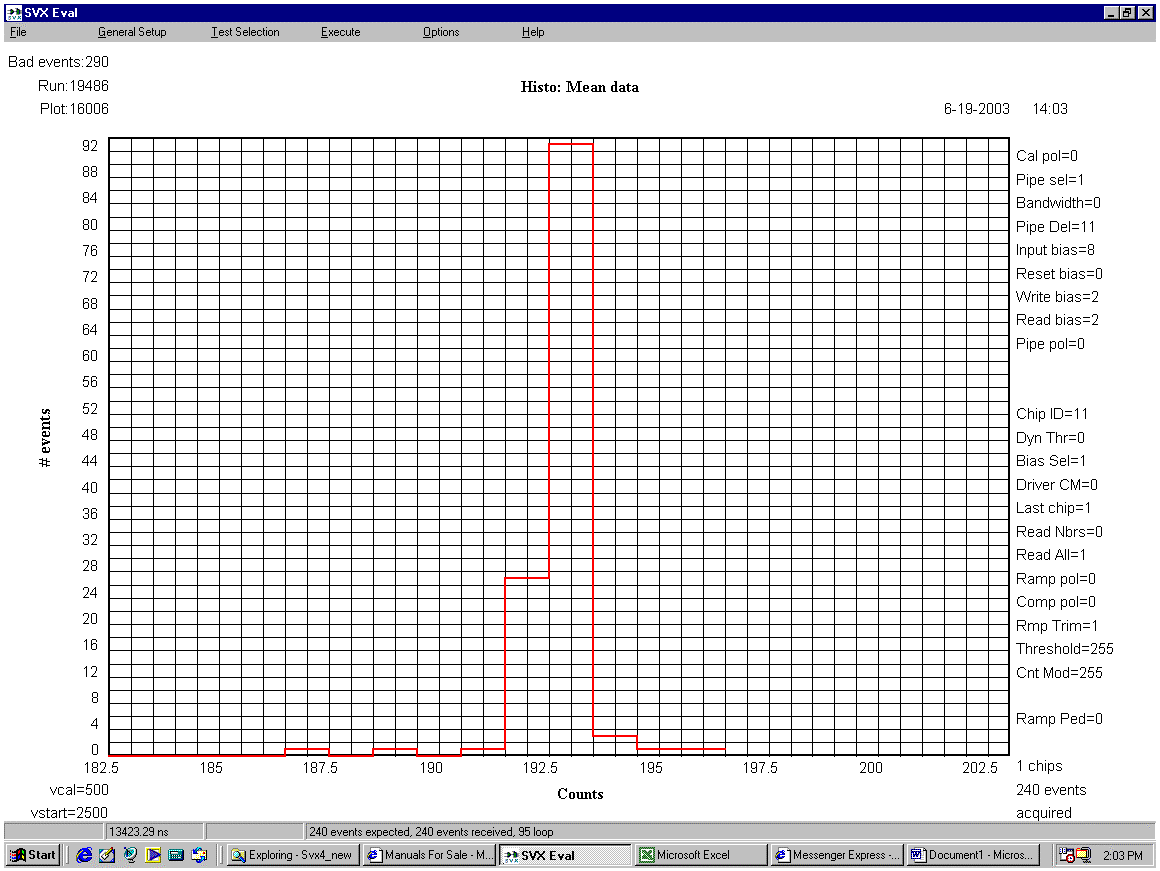
- Pedestal Studies
- Ramp range scans
- Gain Studies
- Noise Studies
- Bandwidth Studies
- Voltage Studies

Note

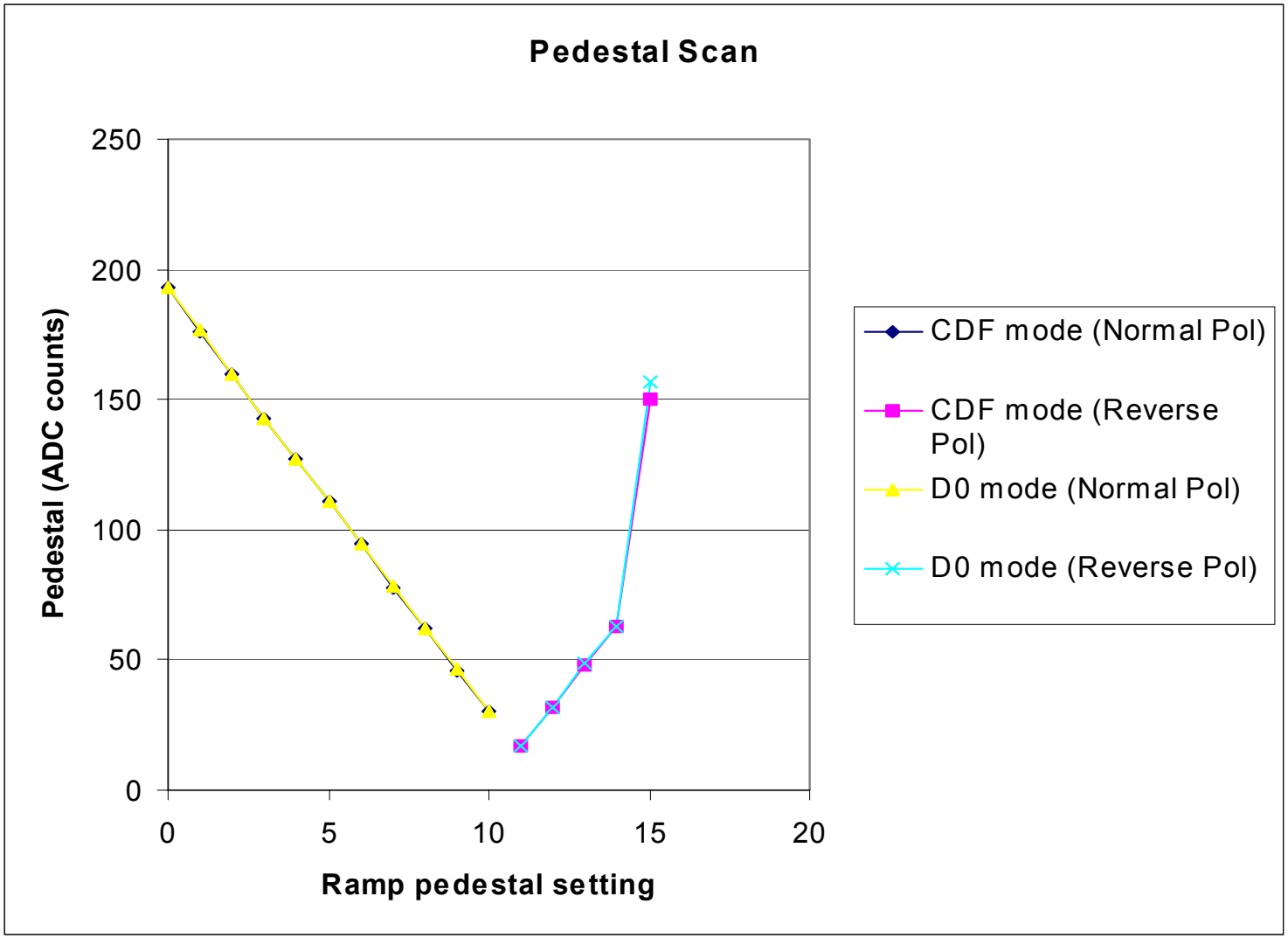
We did these studies at the nominal AVDD=DVDD=2.5V unless otherwise stated. Also, the results come from a version B (192 bits) chip labeled June03:02 on the chip carrier.

Pedestal Studies



Pedestal Studies

Ramp ped	Pedestal (CDF mode)	Pedestal (D0 mode)
0	193	193
1	176	176.5
2	160	160
3	143	143
4	127	127
5	111	111
6	94.5	95
7	78	78.5
8	62.5	62.5
9	46	46.5
10	30.5	30.5
11	17	17
12	32	32
13	48	48.5
14	63	63
15	150	157


Pedestal Scan
Pedestal (ADC counts)
250
200
150
100
50
0
0
5
10
15
20
Ramp pedestal setting
CDF mode (Normal Pol)
CDF mode (Reverse Pol)
D0 mode (Normal Pol)
D0 mode (Reverse Pol)

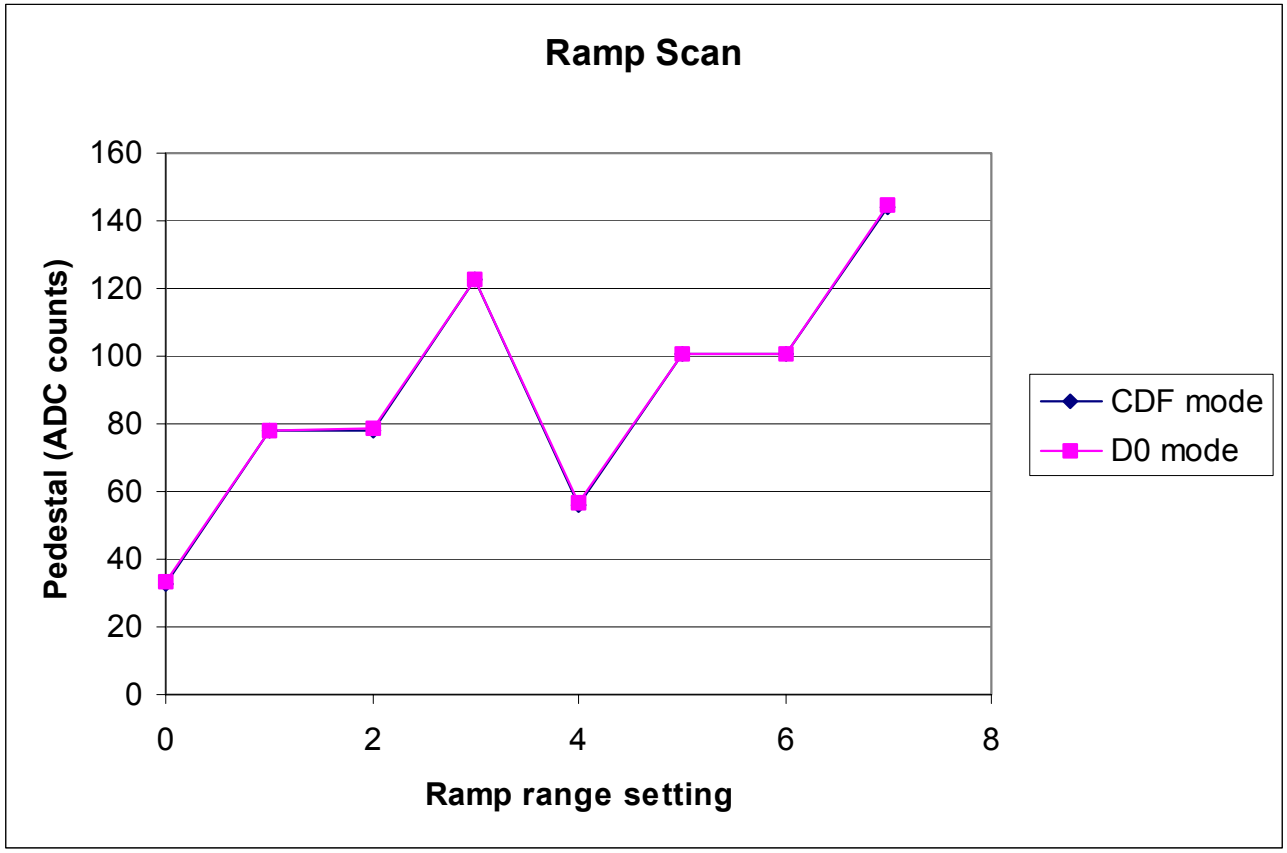
Ramp pedestal	Voltage difference from reset (-279 mV)
0	17 mV
1	15
2	13
3	12
4	9
5	8
6	7
7	6
8	4.5
9	3
10	2
11	2
12	2
13	3
14	4
15	13

Ramp range scans

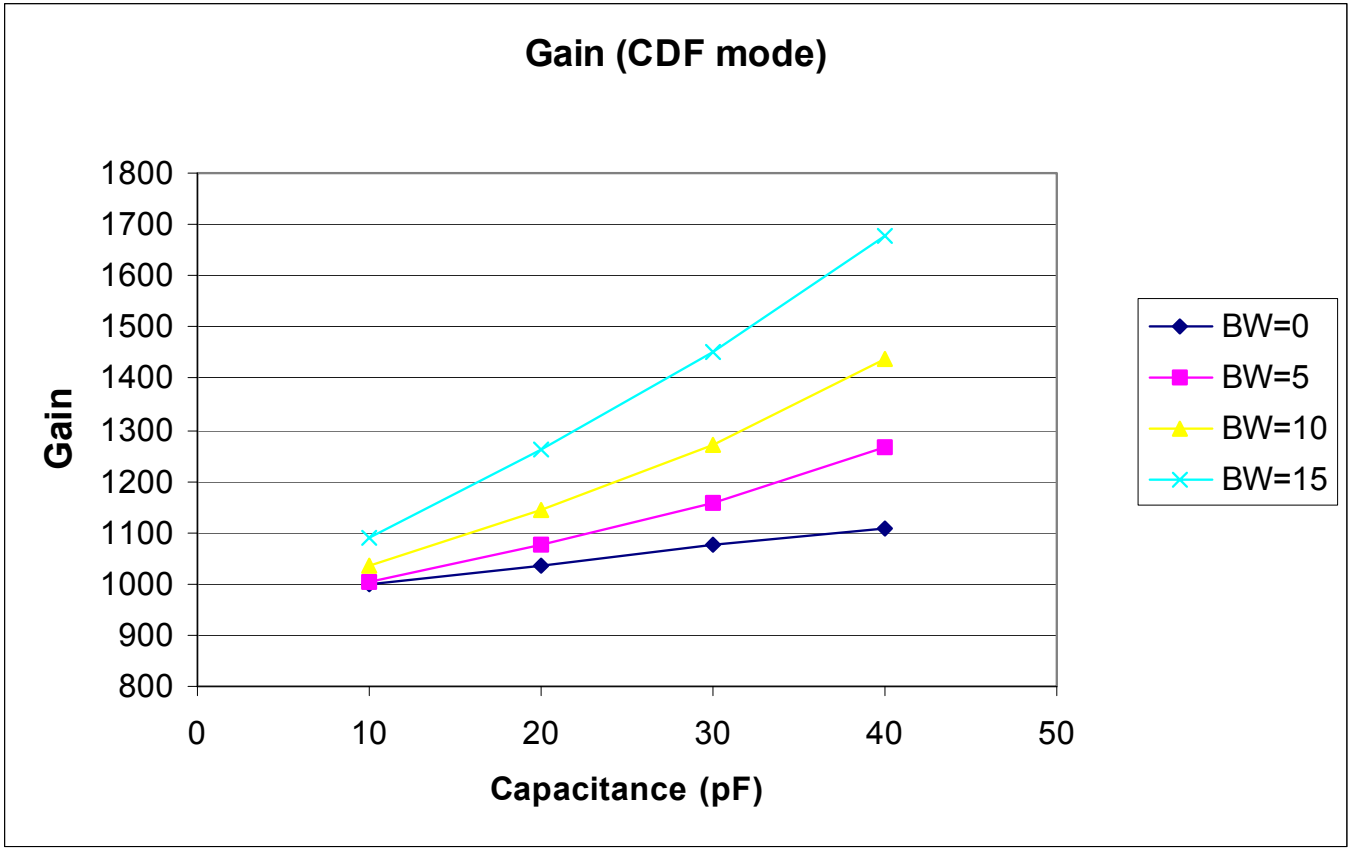
We used a ramp pedestal setting of 7 to do this study. We basically choose it randomly

Ramp range	Pedestal (CDF mode)	Pedestal (D0 mode)
0	33	33.5
1	78	78
2	78	78.5
3	123	123
4	56	56.5
5	101	101
6	101	101
7	144	145

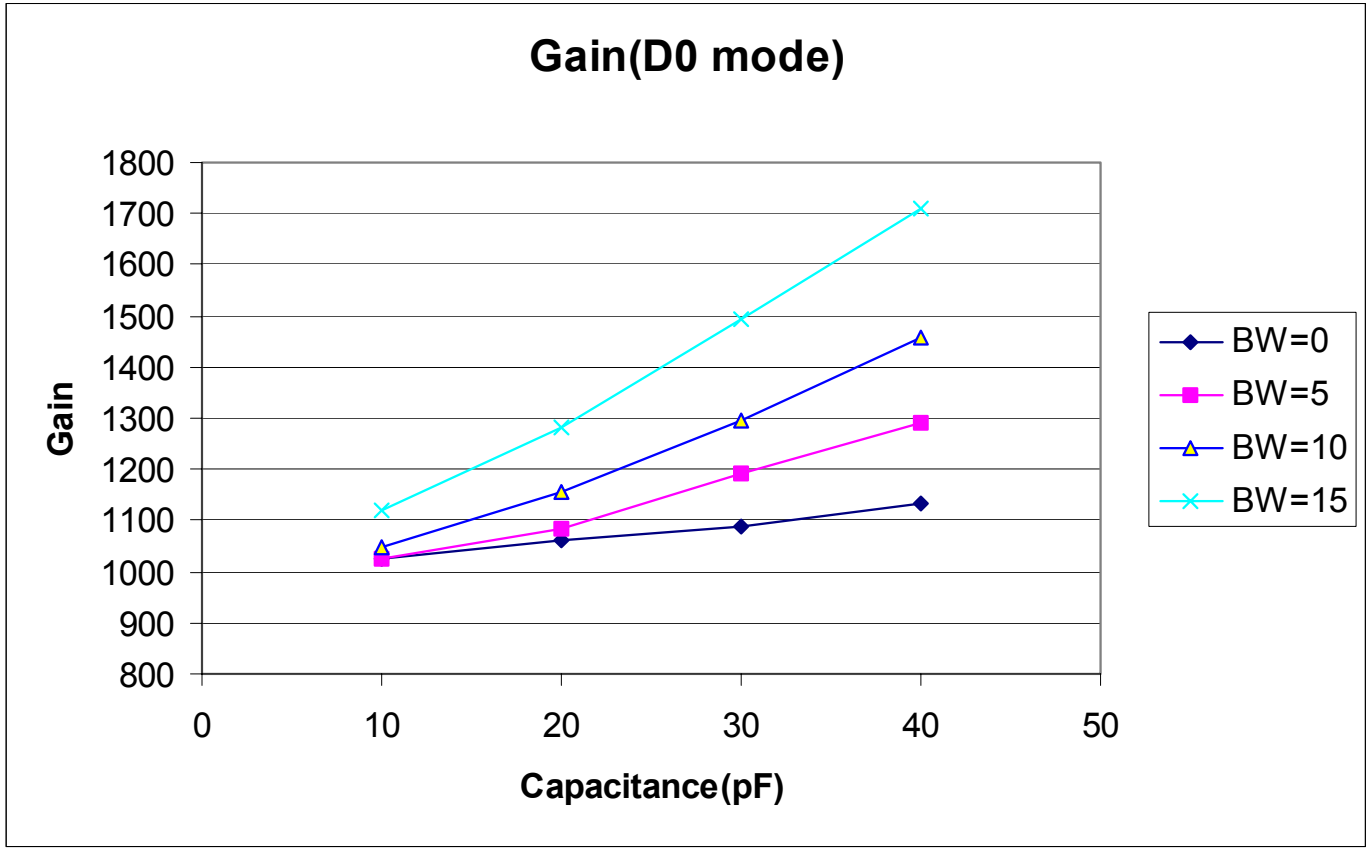
Ramp range scans



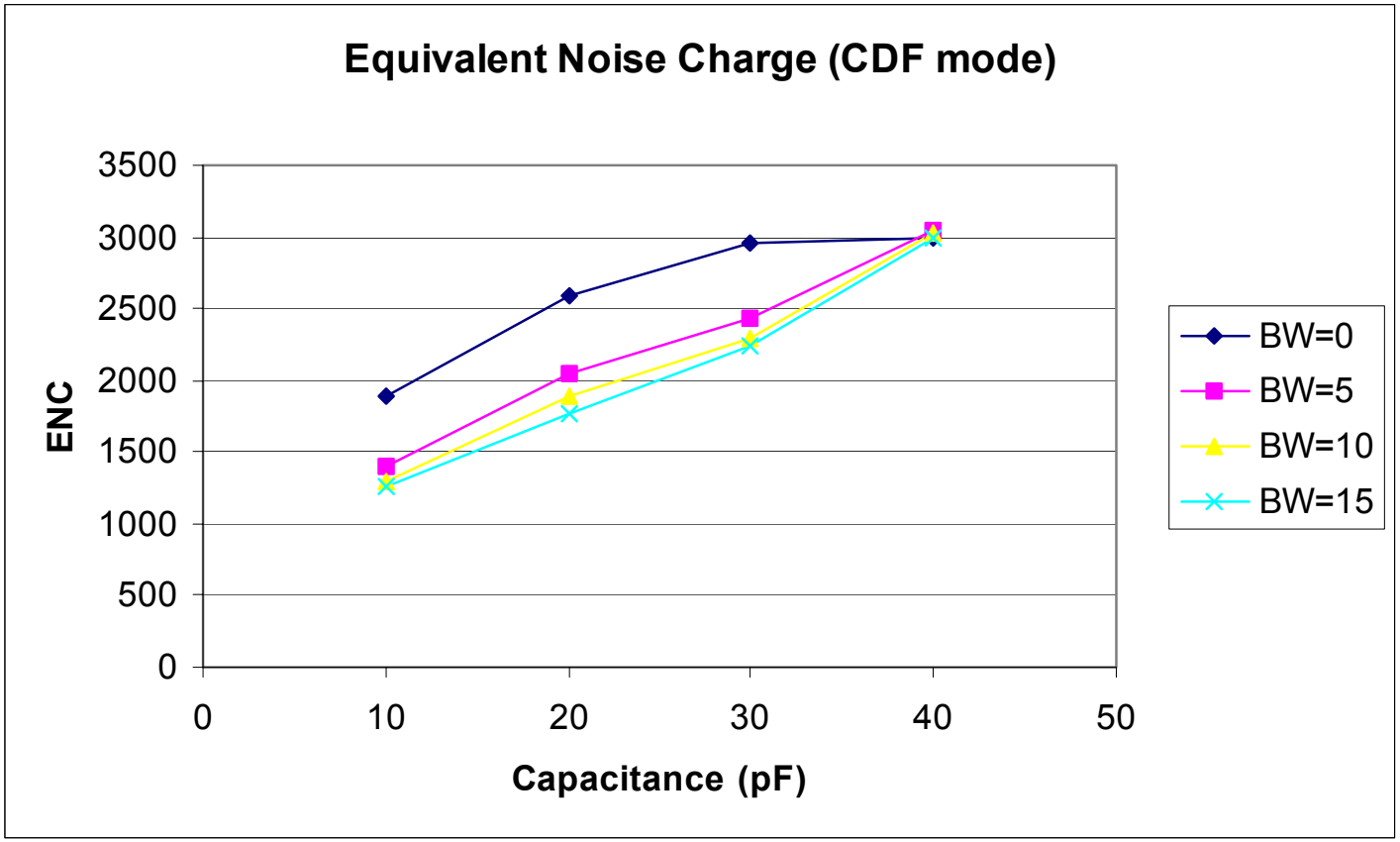
Gain Studies



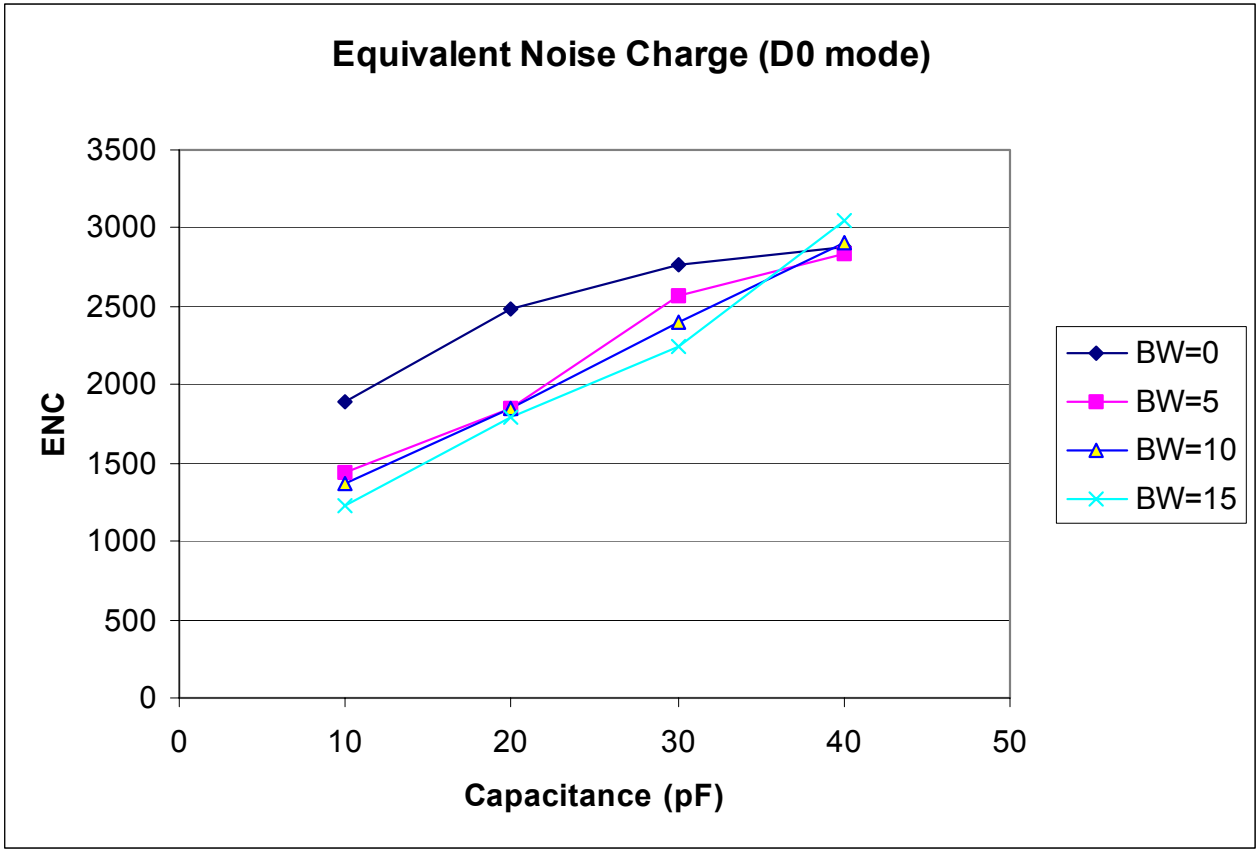
Gain Studies



Noise Studies

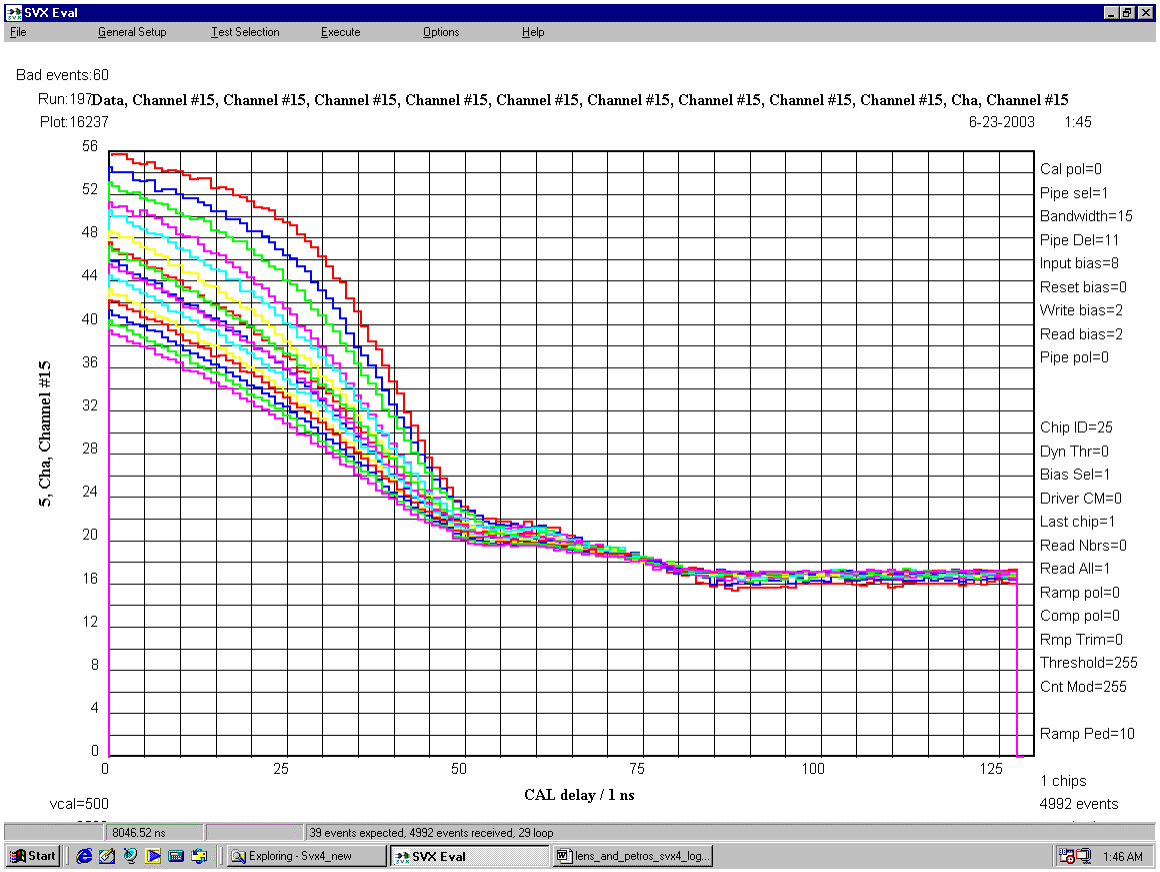


Noise Studies



Bandwidth Studies

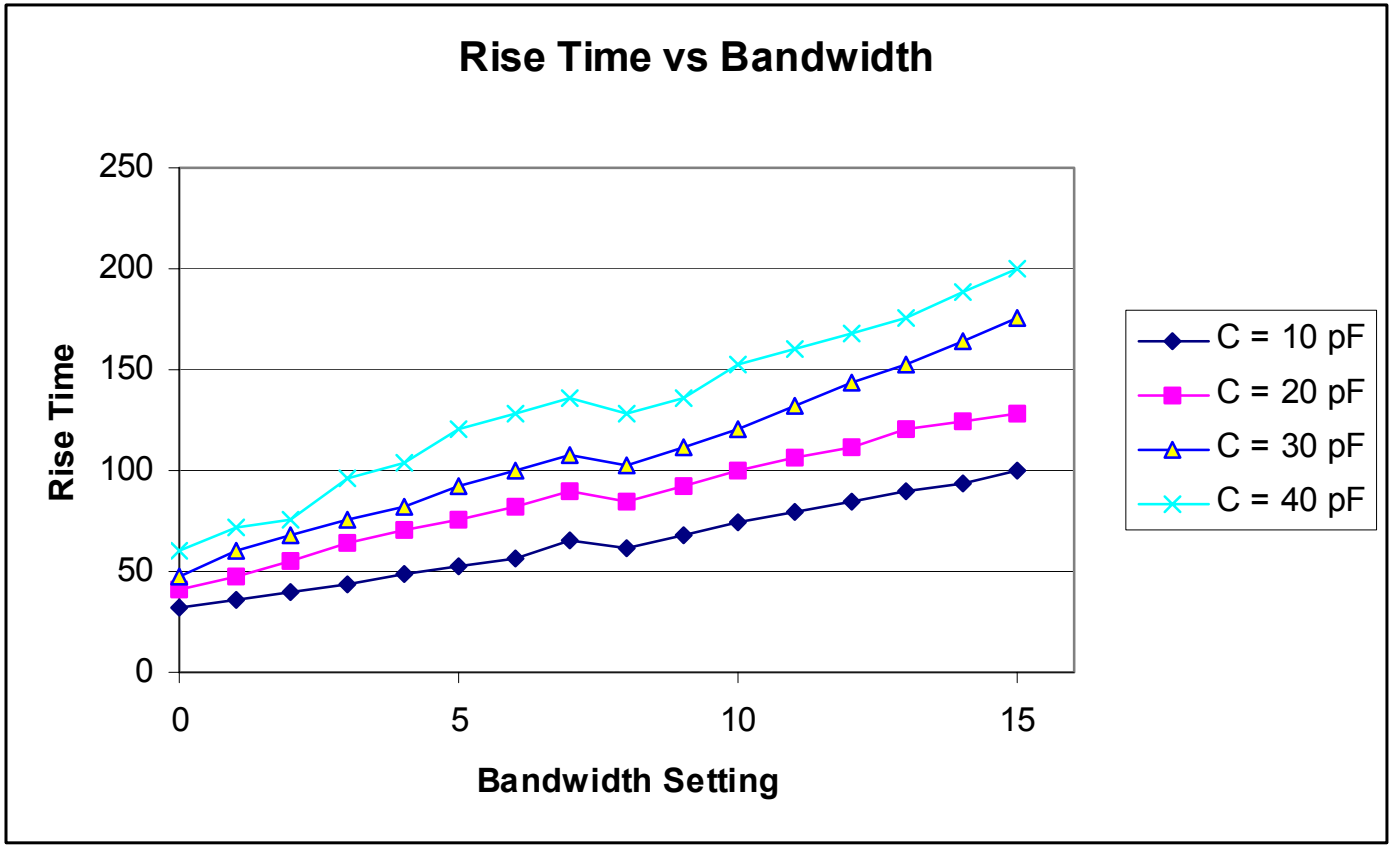
This picture is for all BW (0-15)



Bandwidth Studies

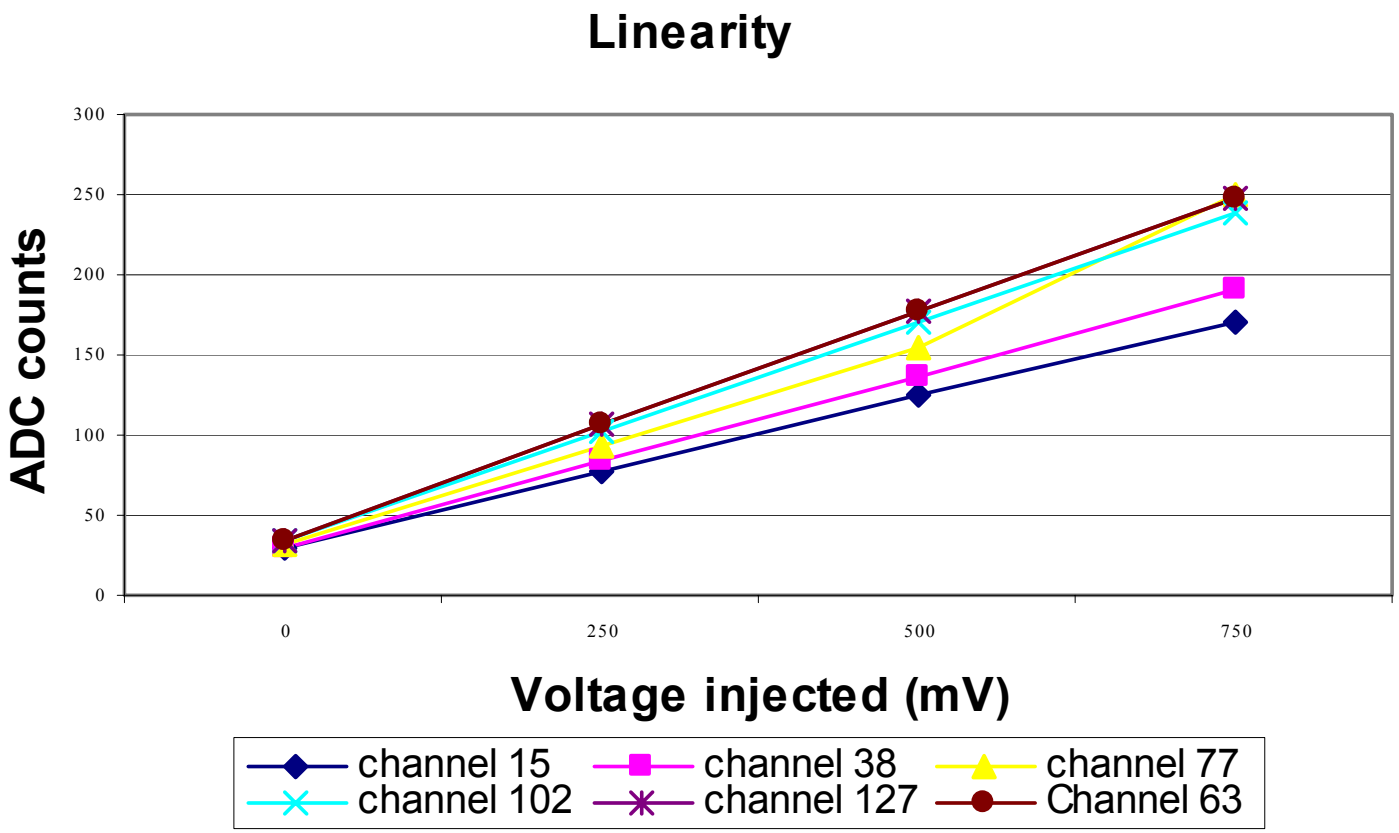
BW\C	10 pF	20 pF	30 pF	40 pF
0	32	41	48	60
1	36	48	60	72
2	40	55	68	76
3	44	64	76	96
4	49	70	82	104
5	53	76	92	120
6	57	82	100	128
7	66	90	108	136
8	62	84	102	128
9	68	92	112	136
10	74	100	120	152
11	80	106	132	160
12	84	112	144	168
13	90	120	152	176
14	94	124	164	188
15	100	128	176	200

Bandwidth Studies



Voltage Studies Using Linearity Plots

V = 2.25 V on board (chip carrier)



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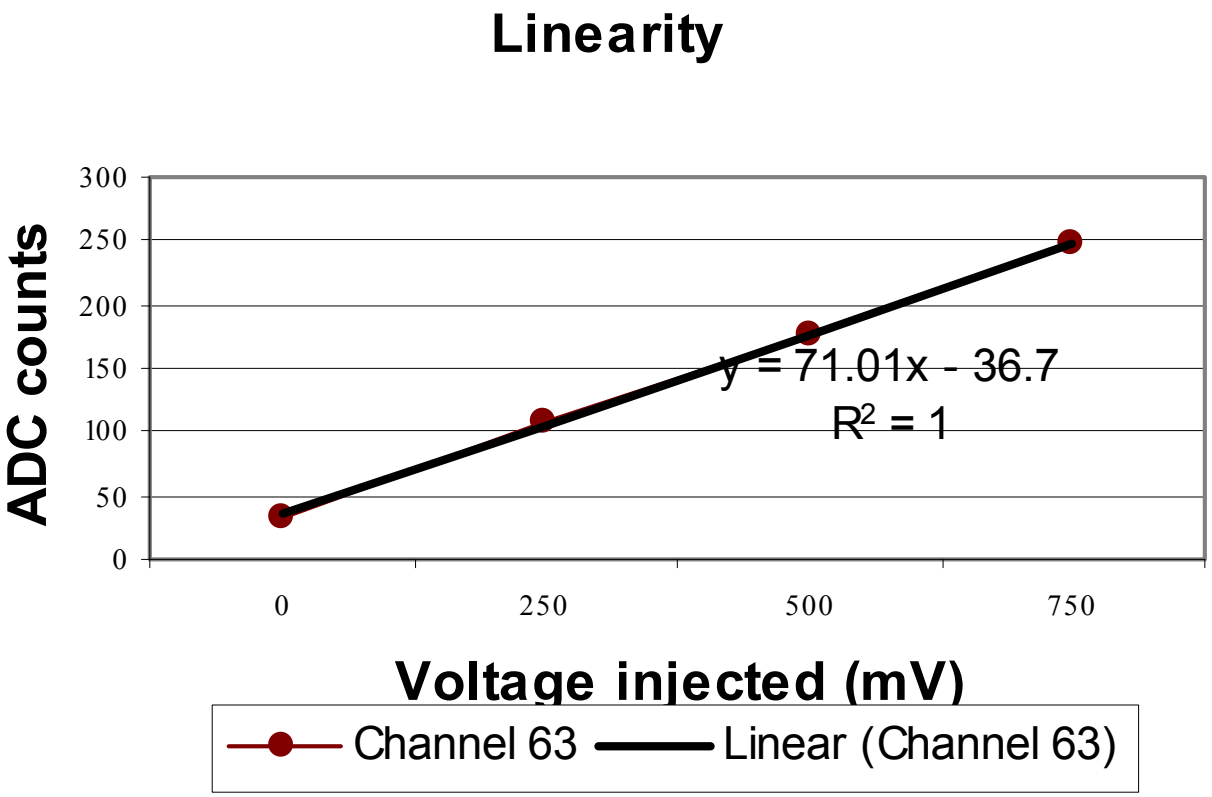

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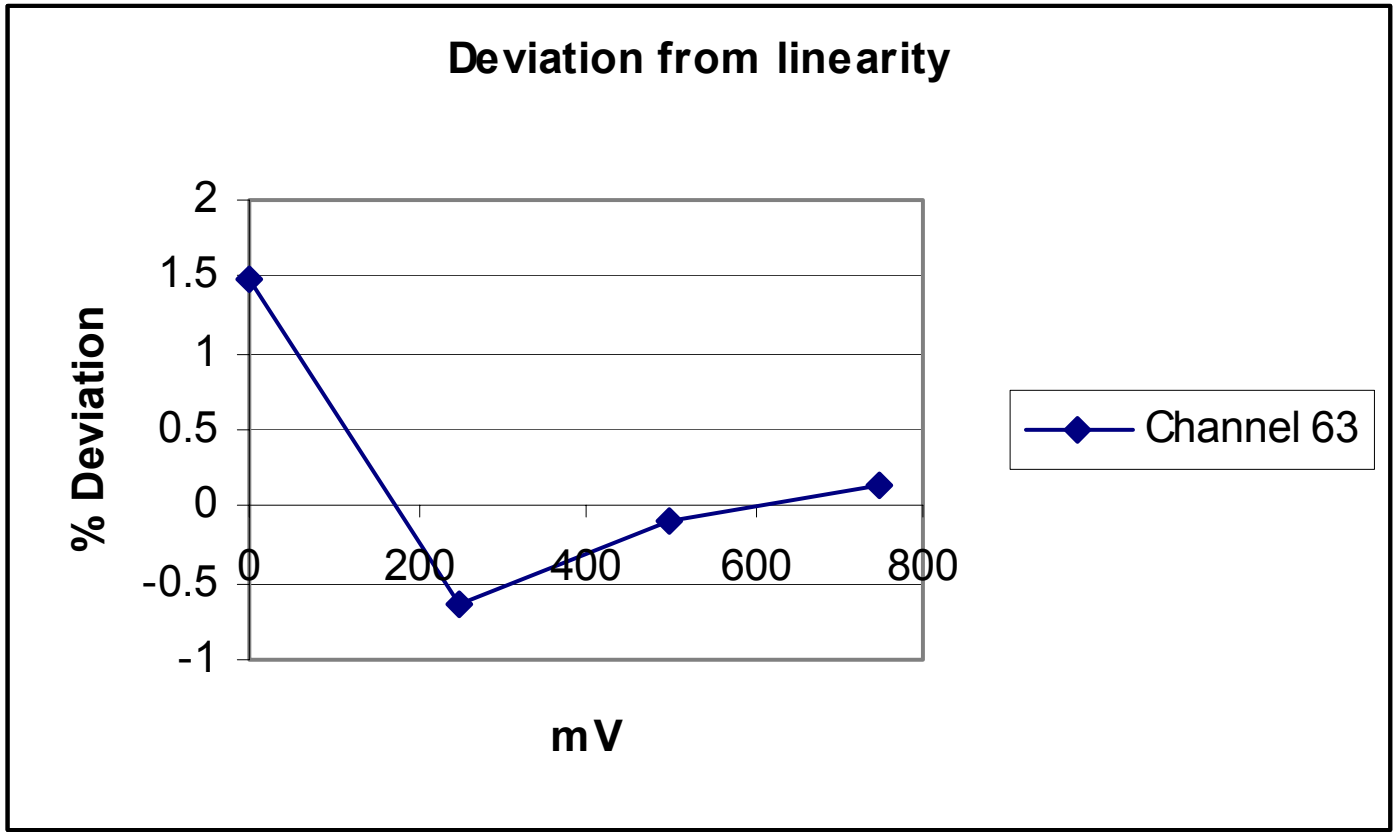
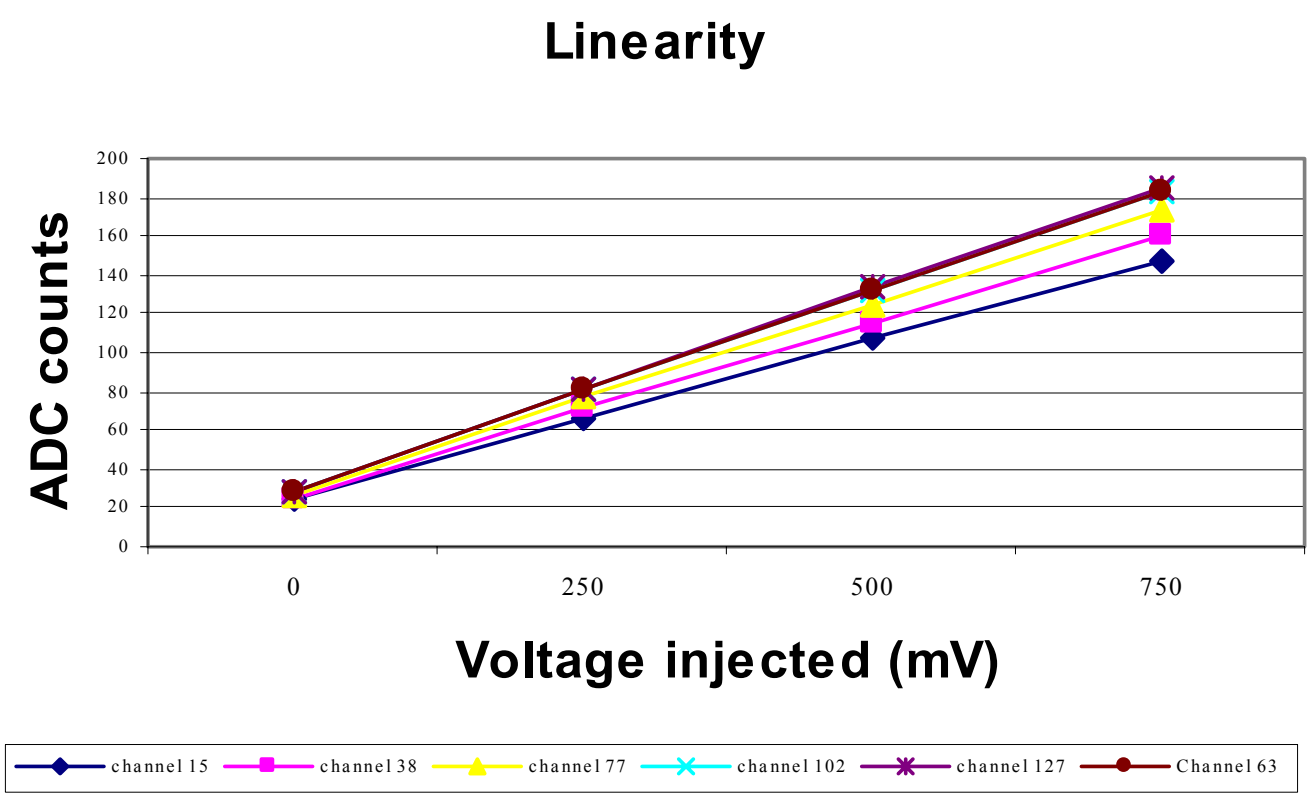
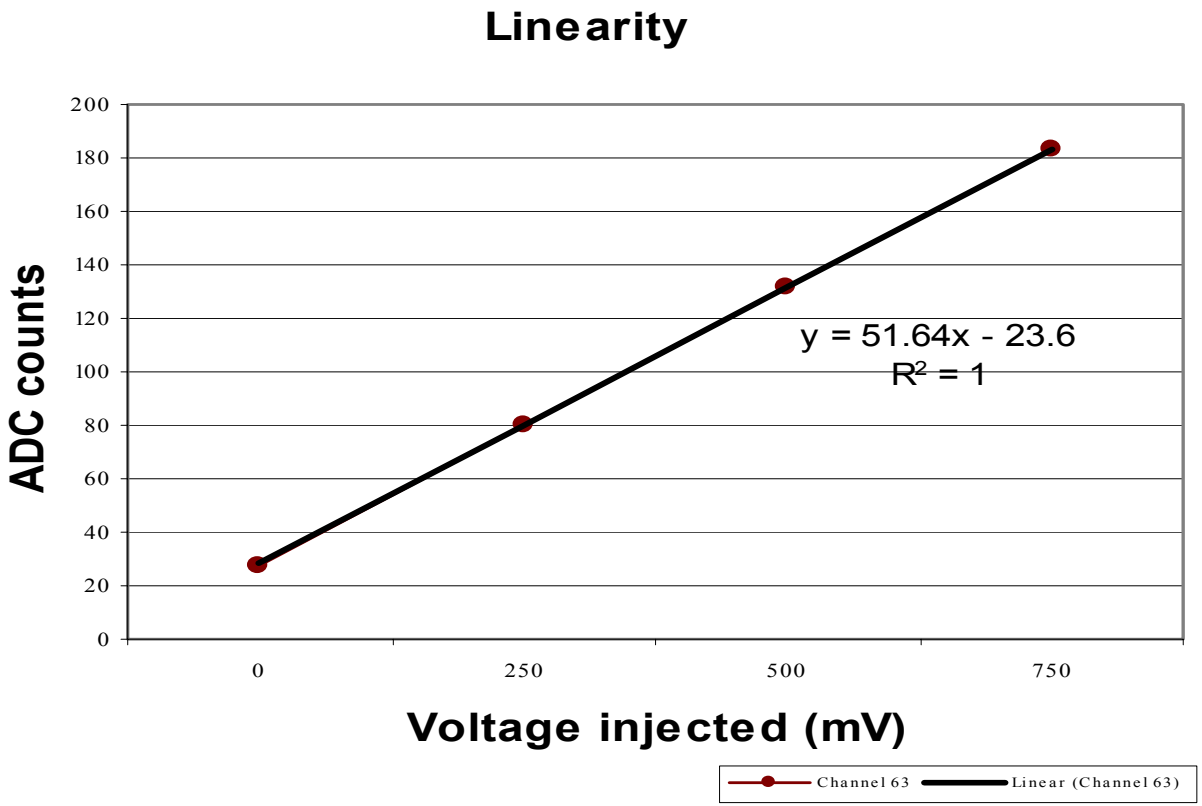
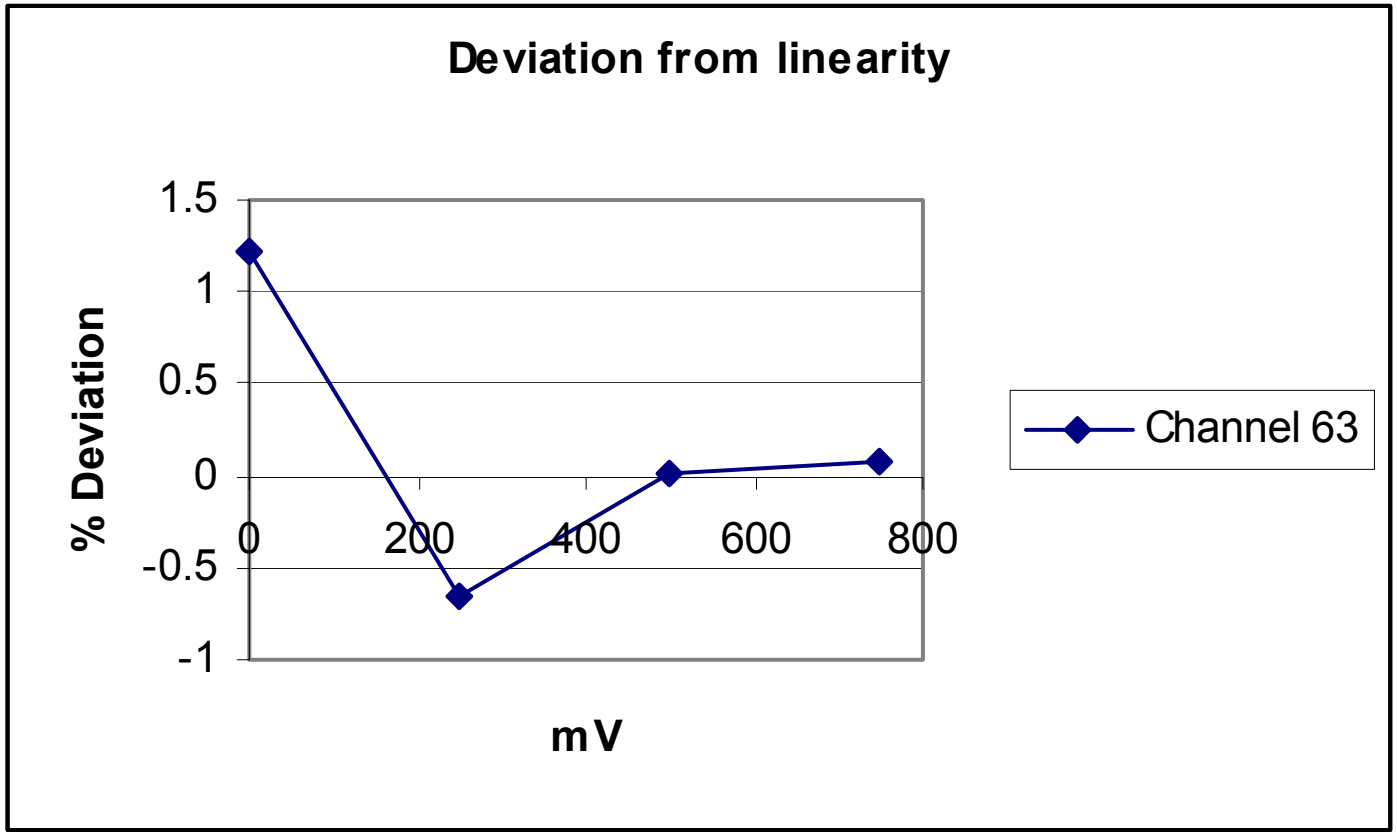


Voltage Studies Using Linearity Plots

V = 2.75 V on board (chip carrier)



V = 2.75 V on board (chip carrier)



V = 2.75 V on board (chip carrier)