

# SVX4 Design Review

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## Summary:

There has been significant progress in many areas since the last review. The existence of a successful test chip including complete preamp and pipeline circuits with acceptable performance is a major success, and considerably reduces the risk of the engineering run. The major concern at this time involves the recent TimeMill simulation results for the readout circuitry in the back-end of the chip ("FIFO"). The incorrect results observed for typical conditions and a schematic level simulation are cause for concern (although these results are quite recent, and considerable further work is required). It is quite possible that larger problems will be observed when post-layout parasitics are included, and all process and power supply corners are studied. This is likely to require several weeks of work to understand, and to place this critical circuit block on a firm foundation.

Significant work remains for the overall integration of the chip, including the wiring up of the individual blocks, and the top-level verification. The final LVS for this chip is rendered more difficult by the mixture of "pure TSMC" design and "IBM/TSMC" design which was required in order to use the standard cell library created by CERN/RAL/LBL with automated place-and-route tools. The full verification path has only been tested for one small circuit block, although no major technical obstacles are expected. This integration and verification effort requires the full-time attention of Brad Krieger to complete the chip on time. The recent results on the "FIFO" simulations also require immediate attention in order to verify the back-end digital circuitry (as is discussed in more detail below). We suggest that strong efforts be made within the collaboration to find additional manpower to try to pursue these two tasks in parallel. Otherwise, we expect the engineering run could be delayed by several weeks from the present target date in late November.

Overall, the simulation and test results presented during the review are very encouraging for the SVX4 chip. In addition to the considerable integration and verification work that remains, it now appears that significant additional simulation effort will be required for much of the digital circuitry. To complete all of these tasks satisfactorily in one month will be difficult, and a delay (on the order of weeks, not months) may occur, although it could be partially offset with additional manpower.

## Specific Concerns

During the review, we discussed several technical issues. Some of these, we feel, should be resolved before submission of this chip (and are noted as such below). Certain others represent future work in understanding system aspects, or ensuring a robust final design. Finally, some of the concerns we raise simply reflect information that we were not shown, which may well exist and should become part of the project documentation.

### *Power issues:*

1) The spec states that the max supply voltage is 3.5V. For the related IBM process, this is well beyond the recommended operating range of the process (2.7V max). Beyond 2.7V, one can expect to experience hot carrier effects (looks like radiation damage, including  $V_T$  shifts,  $g_m$  losses and changes in sub-threshold slope). The limit for the oxide is 3.6V, above which only limited transients are allowed before significant device degradation can occur. Around 4V one encounters the possibility that devices can enter the snap-back region, where high currents can cause thermal failure of devices.

- The meaning of the max voltage spec should be clarified. It appears that it refers to transient conditions of short duration. There is also presently no clamping circuitry implemented on the power pads to avoid spikes on the power supply pads propagating into the chip core.
- The spec also states that the allowed operation range for both analog and digital supplies is 2.25V - 2.75V. As this spec is right at the maximum process operating voltage, there is no margin left for transient conditions. These are difficult design areas, but exceeding vendor limits could have a serious effect on chip reliability. HEP vertex detectors require that the chips operate close to commercial reliability specs, and this will only be achieved by conservative design practices. We recommend careful assessment of chip reliability with real services and power supplies to verify whether there are significant dangers in the present specifications, or whether additional circuit protection blocks might be needed in the production version of the SVX4 chips.

2) No specification for digital power consumption, either DC or AC. Present readout design involves large AC current changes during digitize/readout phases of chip operation. We suggest that the complete digital power budget, both DC and AC, be more carefully analyzed. The related system-design issues of power distribution and decoupling should be tackled soon, to see whether the present digital power consumption is acceptable in the production chips.

3) Use of significant internal decoupling based on PMOS capacitors connected directly to substrate. What are the reliability issues for TSMC? Is there a recommended configuration? IBM strongly advises use of only an NMOS in substrate-connected N-well configuration for decoupling caps, and strongly recommends use of a small M1 trace in series, which will electromigrate away under the high current produced by a shorted capacitor. The SVX4 design uses a large series R to limit the current per shorted cap to 1mA. Is the local power distribution adequate so that a chip will operate properly with at least one such defective capacitor (without excess voltage drops)? As decent yield has been seen on a test chip with this capacitor design, there appears to be no catastrophic problem for the upcoming engineering run. However, this issue should be considered in more detail before the production run for SVX4.

One should note, however, that two versions of the IC will be submitted: one with the on-chip decoupling, and one without.

***Preamp:***

- 1) (***Should be addressed before submission***) Supply spec states the operation over the range of 2.25V to 2.75V is required. No measurements or simulations were presented to demonstrate operation at the lower supply corner.
- 2) (***Should be addressed before submission***) Preamp design involved many stacked devices (5), suggesting that there is very little margin left under operating conditions. Although some measurements have been done to demonstrate that margin exists in the test chips, we suggest more careful study of the circuit design with corners (device parameters and supply voltage) to make sure there is enough voltage margin.

***Pipeline:***

- 1) Several logic changes and improvements were made in the Pipeline Controller. These changes should be documented, and consideration given to Timemill simulation of the performance over the supply range and process corners.

***ADC:***

- 1) Many matching issues arise in the comparators used for the analog delay and for the common-mode noise threshold circuit. The critical issue here is channel-channel variations within one chip. Although it appears that there are no major problems, we would like to see a more global analysis of these issues. This would include  $V_T$  matching and its effects on channel-channel variations in delay, matching requirements on the small capacitor added to the delay comparator to create a guaranteed "offset" after reset, and sensitivity to the actual value of the 10fF parasitic capacitor used to sum the signals from the individual comparators for the common-mode threshold circuit.

***Digital back-end:***

- 1) (***Should be addressed before submission***) The design of the "FIFO" structure used to read out the appropriate set of ADC values has been done using standard cells and Verilog simulations. In order to reduce the power consumption, the design is now fairly complex, using dynamic gating of clock signals (treating the clock as a signal in the design). This is a potentially risky design approach, which requires very careful verification. Only very recently has a "spice-like" simulation been performed using TimeMill. Unfortunately, it does not show correct operation of the "FIFO". This problem requires immediate concentrated effort. Until it is deeply understood, one should assume that the real verification of this circuit block must be performed with TimeMill, and all of the key test vectors used for the Verilog verification should be re-simulated using TimeMill, including process and power supply corners. The present design may require improvement in order to operate properly, and this will almost certainly delay the engineering run.