

Observations by module/hybrid tests

1. Systematic pedestal shift event by event, showing bipolar distribution.
2. This happens when you reset the pipeline pointer in each event.
3. If the disable mask is on (=preamp kept resetting), no such bipolar distribution.
→ No problems on the digital or backend part.
4. The amplitude of the bipolar swing depends on the risetime, i.e. load capacitance and BW setting.
5. AVDD fluctuation.
6. Extra PRD2 right after readout period fixes this problem.
← need to understand the reason. Otherwise, the same (or another) problem would happen if we change the SVX4 control pattern.

What are these?

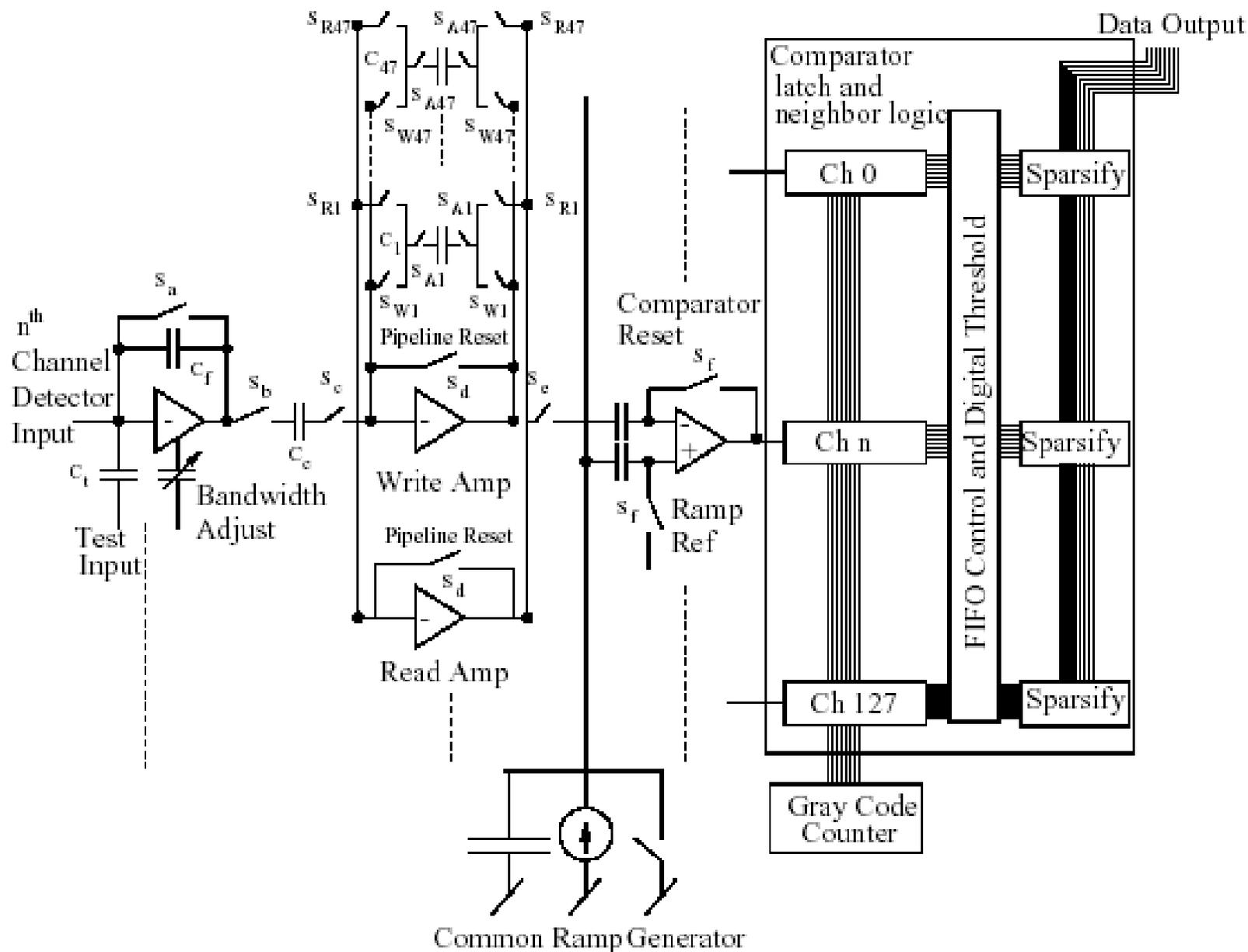
- Pipeline reset:
A capacitor cell is reset if FE clock is high. Once the FE clock low, the write amp sends charge, which is being integrated by the preamp, to the cell for store.
- Reset pipeline pointer:
Cal_sr in init mode resets the pointer of the pipeline, I.e. physically the first cell (0-th cell) is forced to store the charge from the preamp. NOTE! no cell is reset.
- PRD2:
 1. Putting the cell, which is taken by PRD1 for readout, back to the pipeline.
 2. Refresh, or actually taking pedestal, for reference cell. NOTE – the nominal cell is skipped, but the pipeline pointer is still advanced.

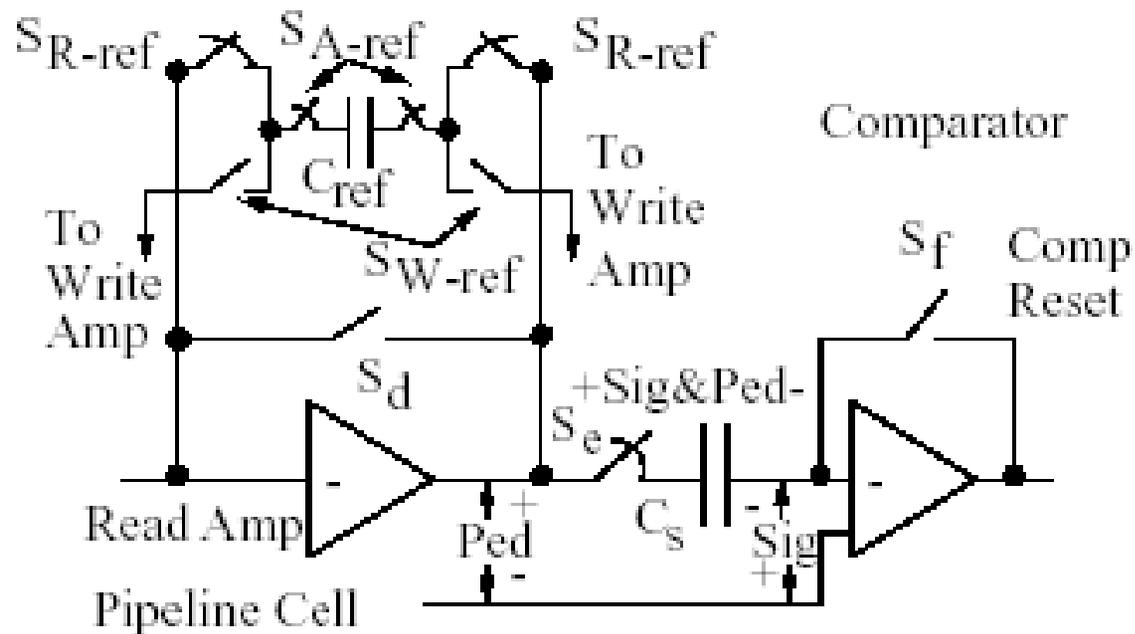
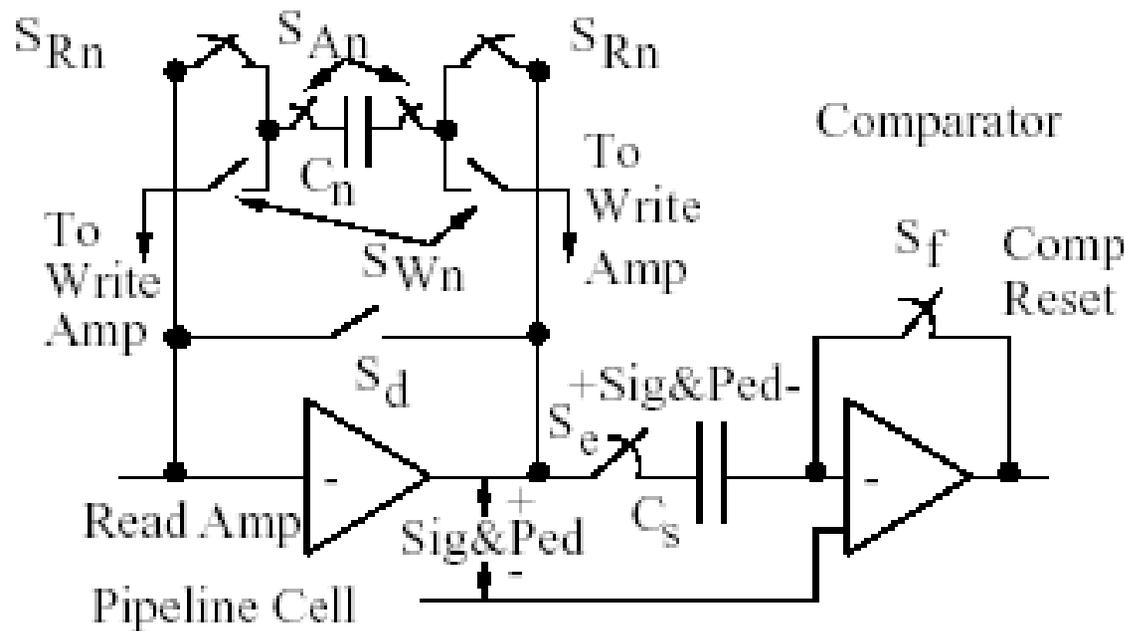
Preamplifier

Analog Pipeline

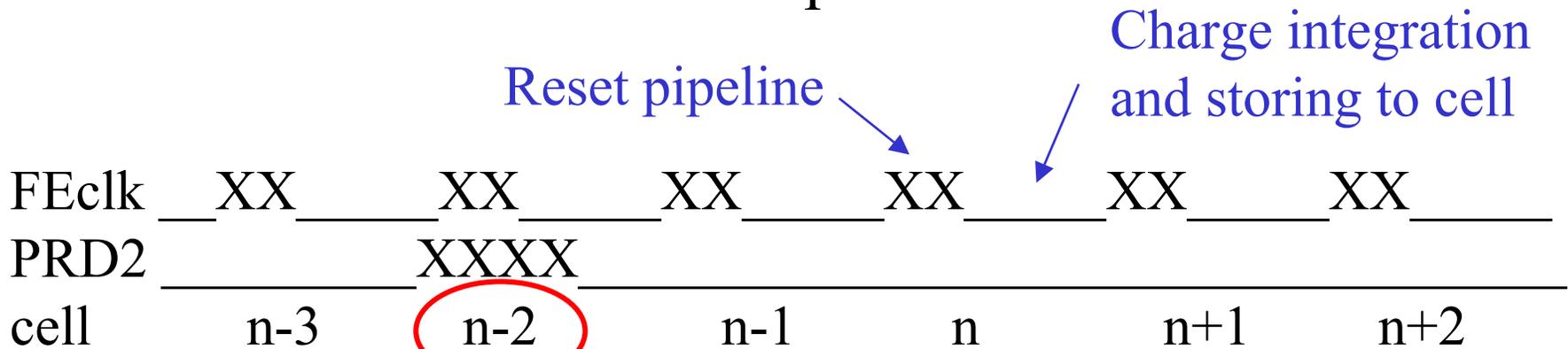
Comparator

Digital Functions





Example



Write amp not connected to this (n-2) cell, but to ref. cell.

- Be careful!
In the experiment, don't read out the cell n-2 in the example. ← needs veto in DAQ (perhaps relevant for CDF), or N clocks after PRD2, where the N is the same as pipeline depth, to make sure we don't read out (n-2)th cell or before. (I had thought the pipeline pointer was not advanced during PRD2 high.)

Firmware Definitions

A. Acquire \rightarrow digitize \rightarrow readout \rightarrow acquire \rightarrow interval \rightarrow
PRD2 (PRD2)

We put cal_sr in init mode to reset the pipeline pointer each event

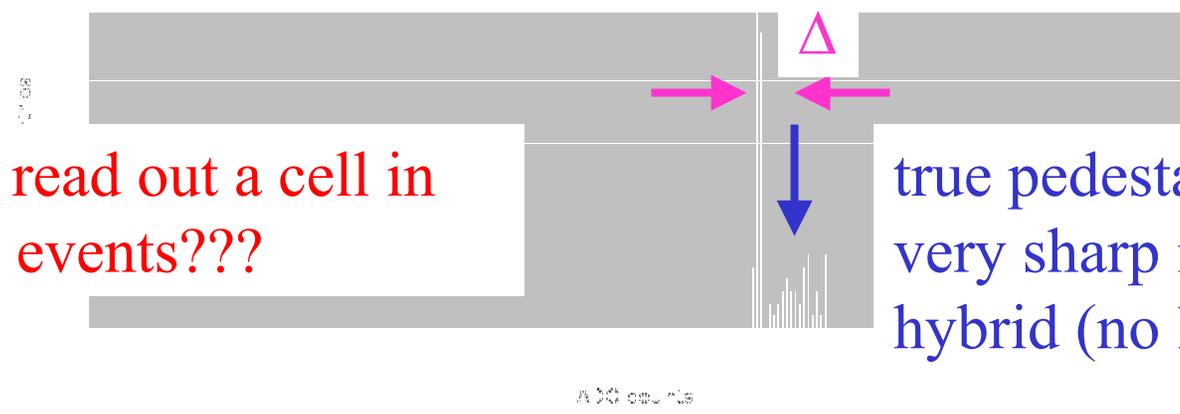
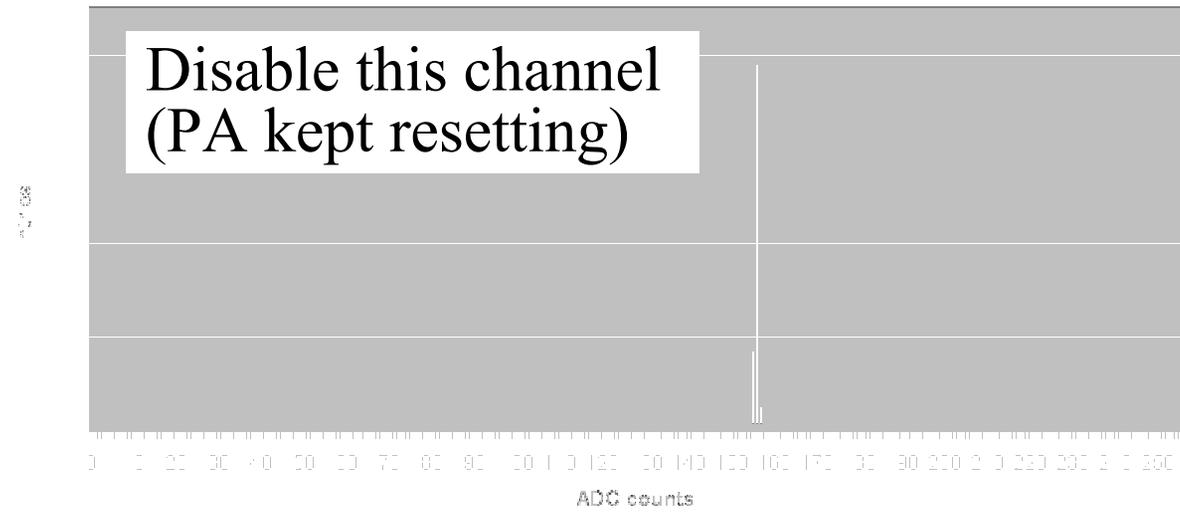
B. Init \rightarrow acq \rightarrow dig \rightarrow r/o \rightarrow acq \rightarrow interval \rightarrow
PRD2

C. Init \rightarrow acq \rightarrow dig \rightarrow r/o \rightarrow acq \rightarrow interval \rightarrow
PRD2 PRD2

D. = C' extra clock before PRD2 in the first acq period.

Observation

RecoSim -> Simulation



→ Fail to read out a cell in every two events???

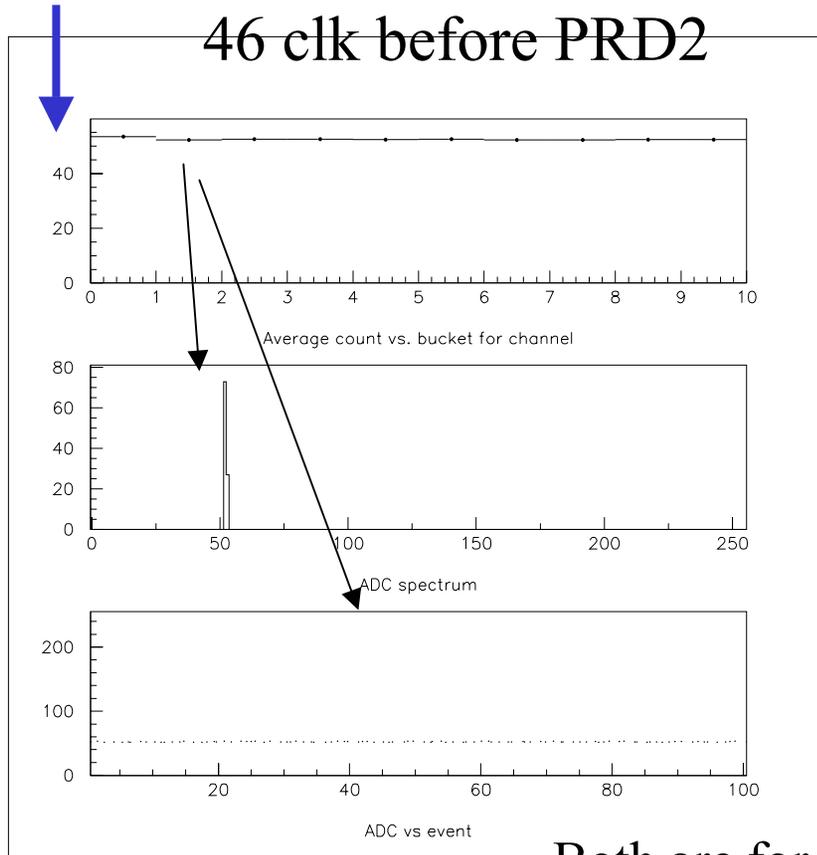
true pedestal. this is very sharp in bare hybrid (no load).

Another Observation & Proposal

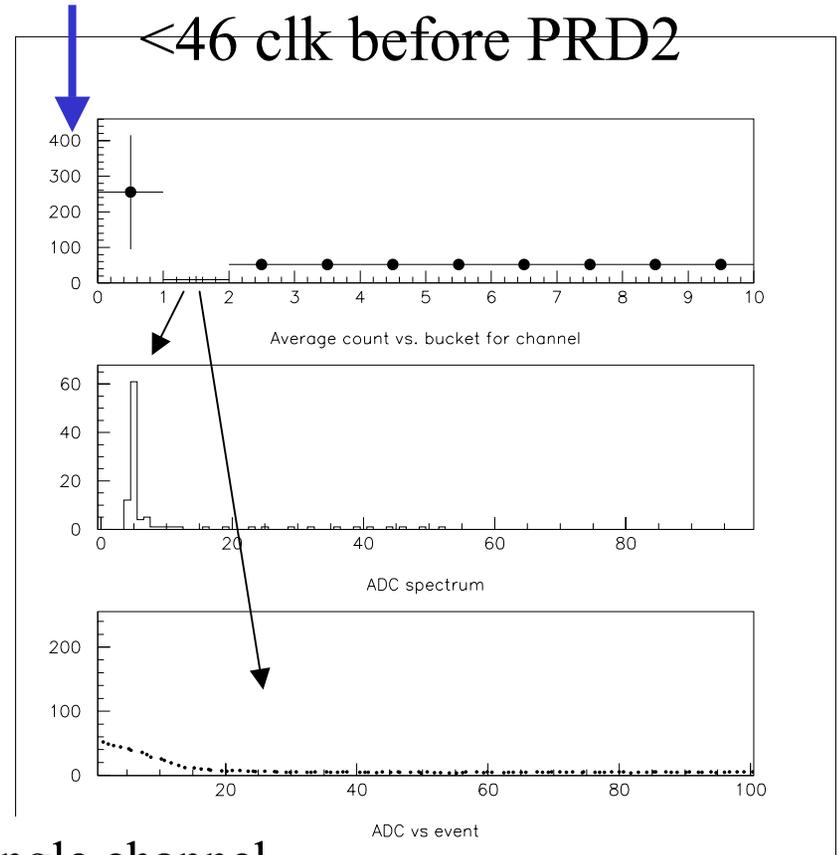
- In version B, L1A (and other bus line activities) in the second acq period, instead of PRD2. ← very suspicious.
- Remove the weird L1A and others in version B.
- Remove the extra PRD2 after readout in version C to see if we really need two PRD2.
- We always have to ask Mike to change the modification, even one change. This is a heavy load.
- Isn't it possible to run the hybrid by the stimulus setup?
AVX connector – board – stimulus connector ?????
← necessary debugging in a second.

Single chip test result

PRD2



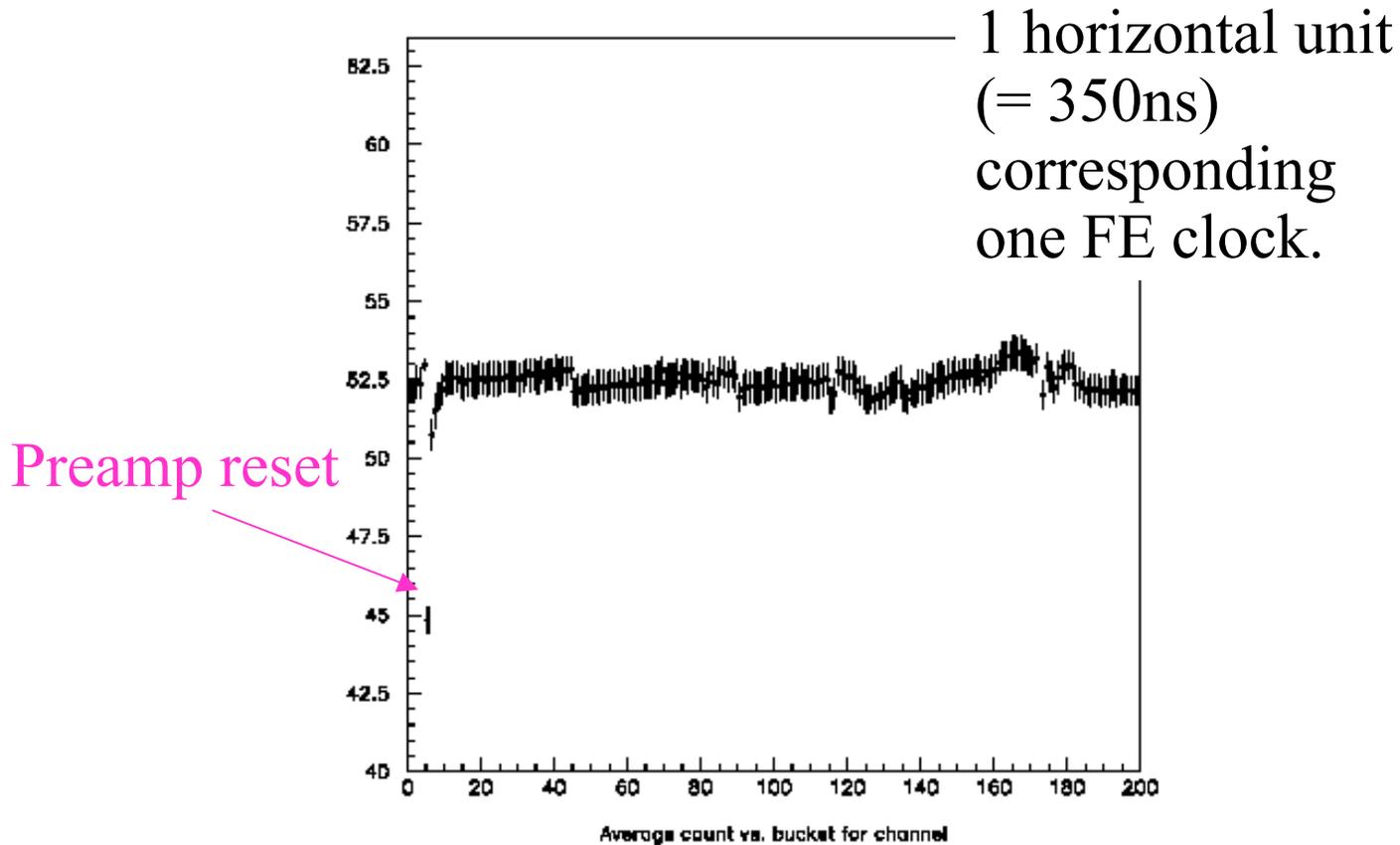
PRD2



Both are for single channel.

Resetting pipeline before real acquire seems mandatory if there is a period without clock.

Another test result



preamp reset time $\sim 1\mu\text{s}$ or more to be stable ?