

Possible Use of Multiple buffers in the SVX 4

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Introduction

Present readout times for the D0 silicon detector are about 15 μ s for the best rates and substantially longer for some crates. The 15 μ s time comes from 11 μ s of digitization and readout and 4 μ s from restarting the pipeline. Because of errors in the design of the SVX 2 pipeline counter, this counter must be reset after every readout so there is no possibility of restarting the pipeline.

The long readout times for some crates are limiting the detector L1 accept rate to about 1 KHz. Fixing the problem crates or imposing a maximum readout length per silicon ladder will increase the L1 trigger rate. But unless the readout time is artificially limited by imposing a length cut off, the event rate that we can expect is not likely to be over 3 KHz for 5% detector dead time.

Estimating L1 Accept Rates

We can estimate the maximum L1 bandwidth from a simple queuing theory model. Event arrival times follow a Poisson distribution. Digitization and readout times are not likely to follow a Poisson distribution (digitization time is fixed, for example) but Monte Carlo simulations indicate that simple queuing theory gives reasonable estimates. If there is sufficient interest, it is straight forward to perform more detailed simulations with a commercial modeling program.

The probability of all buffers being full in an n buffer system is given by

$$p = \frac{(1-R)R^n}{1-R^{n+1}}$$

where n is the number of buffers and R is the ratio of arrival time to readout time. When all buffers are full, the experiment is dead so p is set to the desired dead time. This is currently about 5%. Table I shows the maximum arrival rate for 5% and 10% dead time for 1 to 8 buffers.

Buffers	R for 10%	L1 rate at 10%	R for 5%	L1 rate at 5%
1	.11111	7,406	.0526	3,508
2	.3935	26,232	.2572	17,149
3	.6021	40,141	.4416	29,442
4	.7394	49,295	.5766	38,443
5	.8314	55,426	.6738	44,924
6	.8952	59,677	.7451	49,675

7	.94089	63,723	.7986	53,241
8	.9745	64,969	.8397	55,980

Table 1. L1 rate as a function of number of SVX 4 buffers for 5 and 10% dead time. The mean readout rate is 15 μ s. for this analysis.

As one can see, adding derandomizing buffers has a dramatic affect on the L1 rate. Since this analysis treats only a single queue, the real experiment rate is likely to be substantially less . I would suggest reducing these rates by 30%. This reduction implies that the maximum L1 accept rate for single buffer mode and 5% dead time is around 2500 Hz. Adding one buffer would increase this to 12 KHz and using all 4 buffers would raise it to 26 KHz. Table 2 shows the L1 accept rates from table 1 scaled by 70%.

Number of Buffers	Achievable rate L1 for 10% dead time	Achievable rate L2 for 5% dead time
1	5185	2456
2	18362	12004
3	28098	20610
4	34506	26910
5	38789	31447
6	41774	34772
7	43906	37269
8	45478	39186

L1 rates for 5 and 10% dead time scaled by 70% to reflect other limitations in the DAQ system. The 70% figure is my estimate and is not yet supported by detailed calculations.

Possible Ways to Use More SVX 4 Buffers

The SVX 4 chip has 4 on board buffers for each channel. All 4 are available in CDF mode and only 1 is available in D0 mode. My suggestion is to implement a combination of CDF and D0 modes to get 2 buffers which increases the L1 accept rate by about a factor of 5 for 5% dead time. Note that this idea is not yet confirmed by tests.

There are two basic differences in chip control between D0 mode and CDF mode. CDF mode has an independent front end and back end clock and four control lines (L1 Accept, PRD1, PRD2, Preamp Reset) are independent pads in CDF mode and part of the bidirectional buss for D0 mode. The main reason that we cannot use CDF mode is the lack of control lines from the sequencer. A hybrid operation, however, does not need all these lines and the front end clock line which is needed does not have to be controlled by the sequencer.

The basic idea is as follows. The D0 mode bit would be controlled by the current sequencer. This could be done by using the VCAL line which may not be used on the hybrid. Use of this line requires a wire patch either on the sequencer or the interface board. An additional clock line would be wired from the adapter card to hybrid. This would be the front end clock and would run at 396 ns. It would be a common line for all ladders, driven from the adapter card and run continuously . There would be a 1553

controlled gate on the adapter card that would connect this clock line to the sequencer controlled SVX clock so that the straight D0 mode of operation is preserved.

For this combined operation, the chip would be put into CDF mode at the start of data taking. Data would be acquired by the front end clock. When a trigger occurred, the sequencer would switch to D0 mode, issue L1 accept and two PRD1 signals to set up the chip to readout the first capacitor and then switch back to CDF mode. This operation currently takes about 21 clock cycles so it just fits into one 396 ns crossing. Digitize and readout would work as it does now. If another L1 trigger occurred during digitize and read out, the front end clock would halt to preserve the L1 data and raise L1 busy to stop additional triggers. After completing readout, the sequencer would switch back to D0 mode and issue a PRD2. If there was a pending trigger, it would follow with 2 PRD1's to set up to digitize the signal. The time length here is not important if there is a pending trigger since the front end clock is stopped (and L1 busy is high). When all this is done, the sequencer switches back to CDF mode and lowers L1 busy to accept another trigger .

It may also be possible to run completely in CDF mode. There are 8 additional lines that are on the 50 conductor cable. The first method involves using 1 of these lines. If a second one could be added, then instead of using one for D0 mode, the two would be used for PRD1 and PRD2. The clock, preamp reset and L! accept could all be common lines driven from the adapter card by a global controller. Lines from the adapter card to the chip would need to be added

Drawbacks

There are 3 main problems that need to be addressed before deciding to pursue this.

The first and probably most important is noise in the calorimeter. This was measured during the last shutdown and it shows that the single ended signals create a lot of noise. The SVX 4 uses mostly differential signals but there are still single ended control signals which could produce unacceptable noise. This will require careful design.

The second drawback is project delay. The combined mode may require only adding a clock line if we can use the Vcal line. However, the adapter card would need to be redone and some type of global L1 clock would need to be designed. Total CDF mode would require some patching to the interface card as well as modifications to the hybrid.

The third drawback is the need to replace the CFT system. The L1 accept rate is determined by the slowest element and the SVX 2 in the CFT system would still have the same rates as shown in table 1 for a 1 buffer system. The TriP chip could be implemented to have multiple buffers by changing the FPGA coding. There should be no additional costs for the added buffers over the replacement that has been discussed before.

Conclusion

This is a quick description of a possible scheme. I have discussed this with Brad Krieger and I think that it conforms to his view of how the SVX 4 chip operates. However, the chip has been designed by several people and it is a very complex part so oversights are easily possible. The only real way to be certain that this method will work is to mount a test. The effort required for this test is probably similar to that required for testing the SVX3 with the D0 readout system. That test took about 3 weeks.

I also did not discuss the option of limiting the readout time by stopping the readout after a certain amount of data is read. This feature is available for each sequencer crate. It seems to me that this would have to be set quite long so that it does not introduce subtle biases in the data