5/3/05 DS, AN

1) Cal inject splitting problem stayed after we used new firmware for SEQC from Mike and for SCL emulator from Ted. We see CALSR has two time locations w.r.t. clock.

About the new firmware from Mike: The file NRZGenB_042905 is now ready for testing. In the old cal_inject mode, it synchronizes the computer-generated cal inject command with the crossing clock currently in use.

About the new SCL firmware from Dave (mail to Ted Zhmuda):
Ted,
Can you change the firmware we use in the SCL daughter card at SiDet so that external triggers get synchronized with the 396ns clock. At the moment they are synchronized to the 132 ns clock. Since we will only be using a 396ns from the accelerator we would like to change to that. We see this as a problem when we set the svx chips up in cal inject mode. We see 3 separate responses depending on which on the 132ns clocks we trigger on in the gap in the pipeline. Can you also make the trigger occur near the start of the transition after a 396ns clock?
We are currently using firmware

DEVICE_1=EPM9320A

p:\electronics\vrbc\altera_design_files\scl_firmware\zmuda\sclr_v10_test_vectors\sclr_test_vectors.pof

2) 5% of channel order error became 1% when we downloaded new firmware to sequencer Control_050205. Further investigations showed that the 1% was occurring at the hybrid connected to the purple card. Three modules and one hybrid connected through full chain didn't have errors.

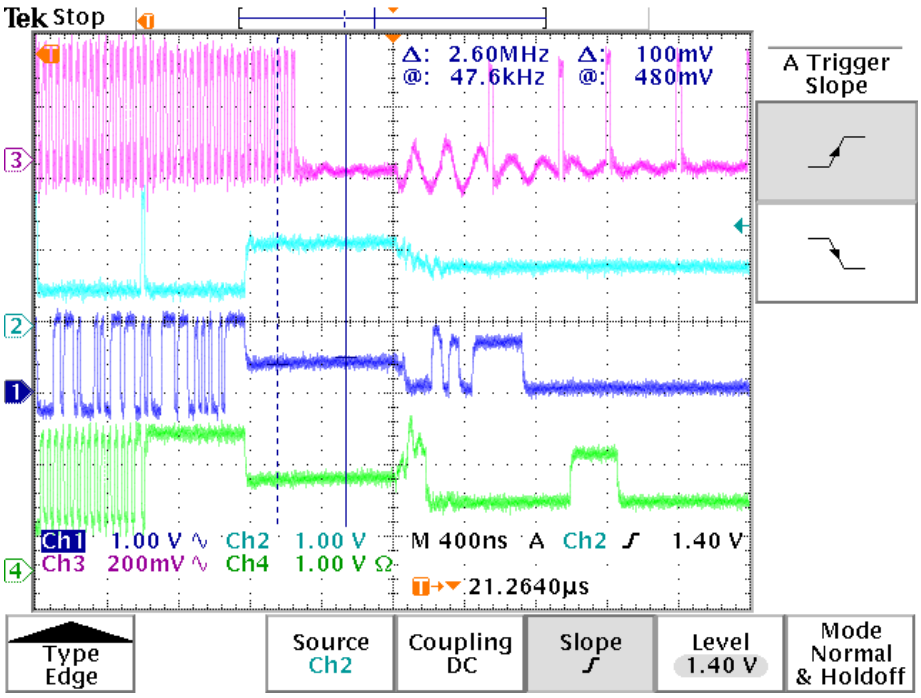
From Mike : Control_050205 delays the start of the 26MHz clock by 18ns but lowers Pri_In 18ns sooner than before.

3) Also looked at data is zero error which was happening at ~1% at the beginning. Then did not observe it when we ran off the 'data' page and then it disappeared also for the 'statistics' page. We don't know why!

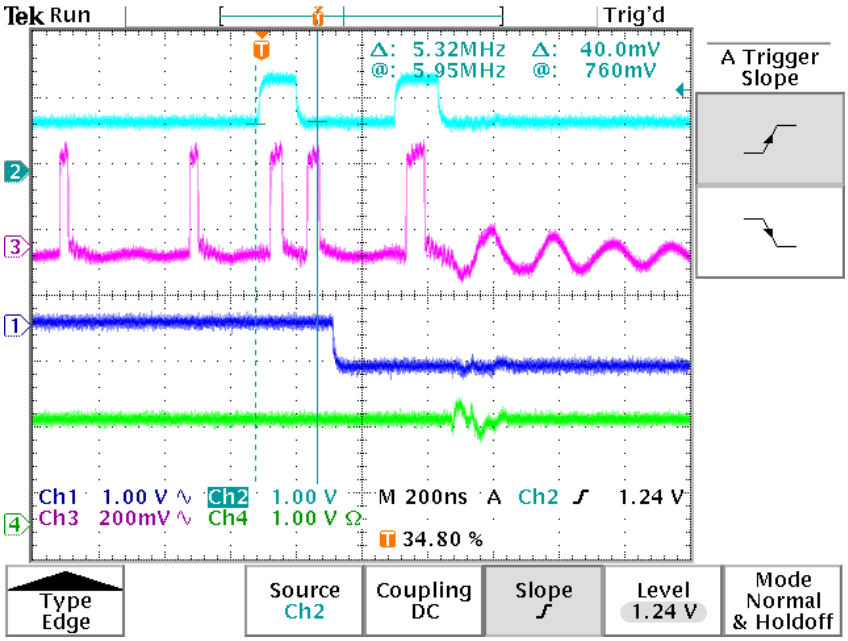
4) Reprogrammed sequencer with Control_050305.

Didn't see any changes in the data. PRD2 (blue) has two extra pulses before going to Acquire, but there are no clocks (purple) under those pulses. Note that there is another PRD2 accompanied by the clock and synchronized with PARST (green trace). This PARST happens all over the place during Acquire.

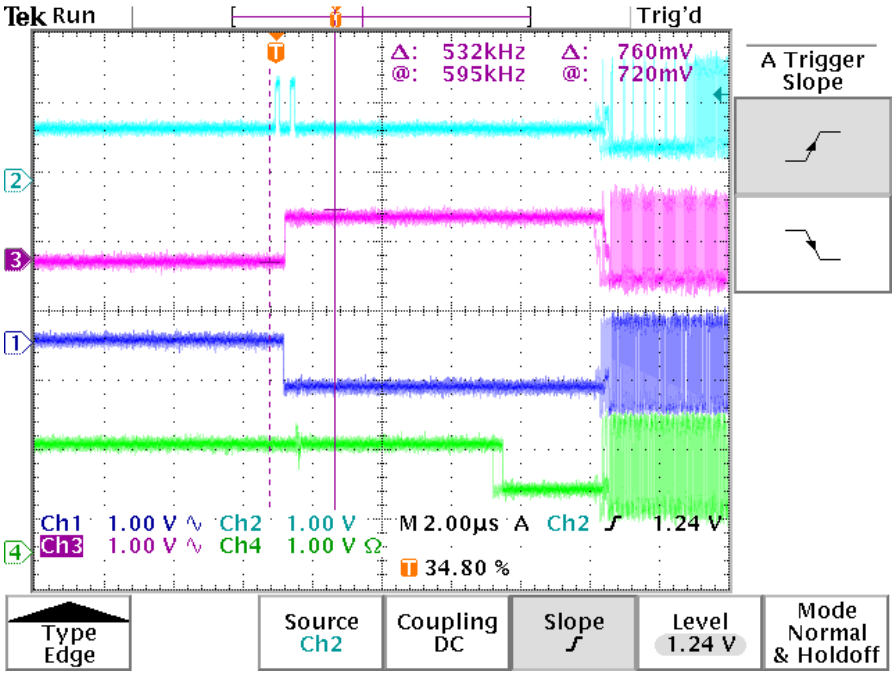
From Mike: The PRD2 had no associated clock at the beginning of acquire, so I made the double PRD2 the same. I understood this to be correct but we should double check as I could introduce a clock under the PRD2 pulse if necessary.



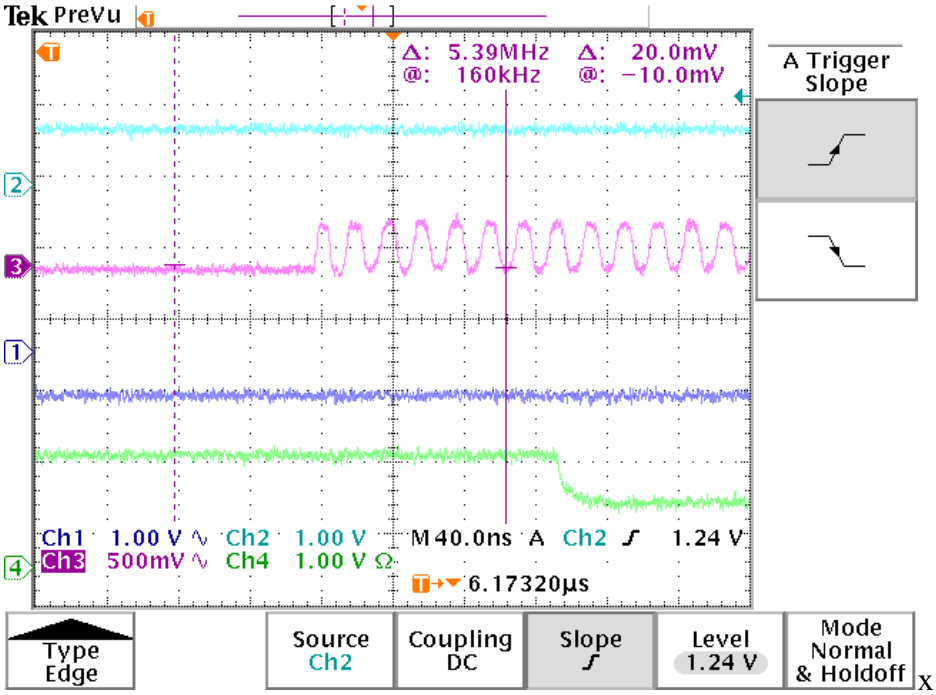
5) Looked at ADC control signals trying to understand the difference in pedestal values between SASEQ (~ 65 ADC counts) and Seq (~ 30 counts).



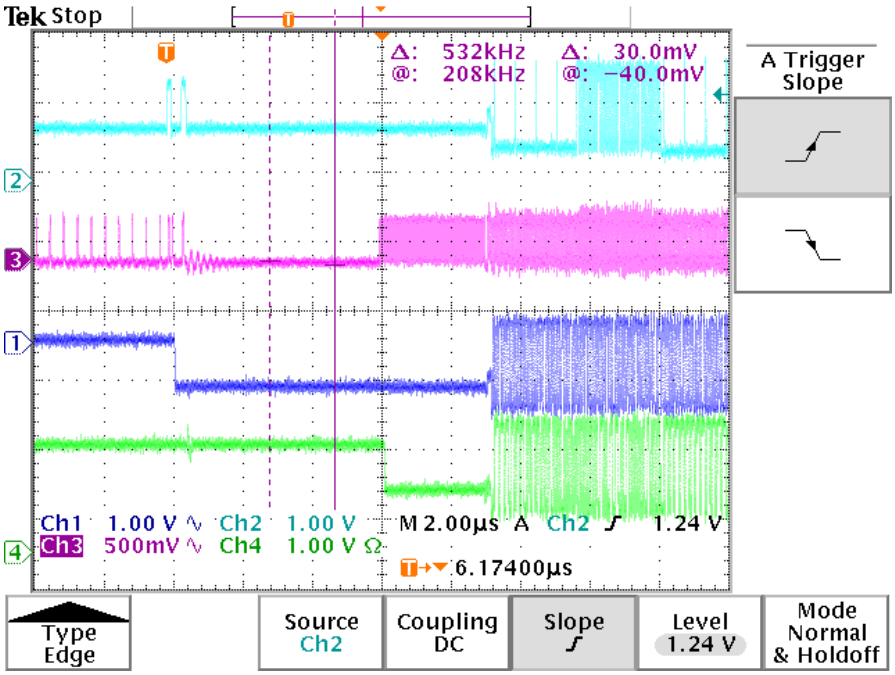
Seq : PRD1, CLK, D0/1/3



Seq : PRD1, D0/1/3

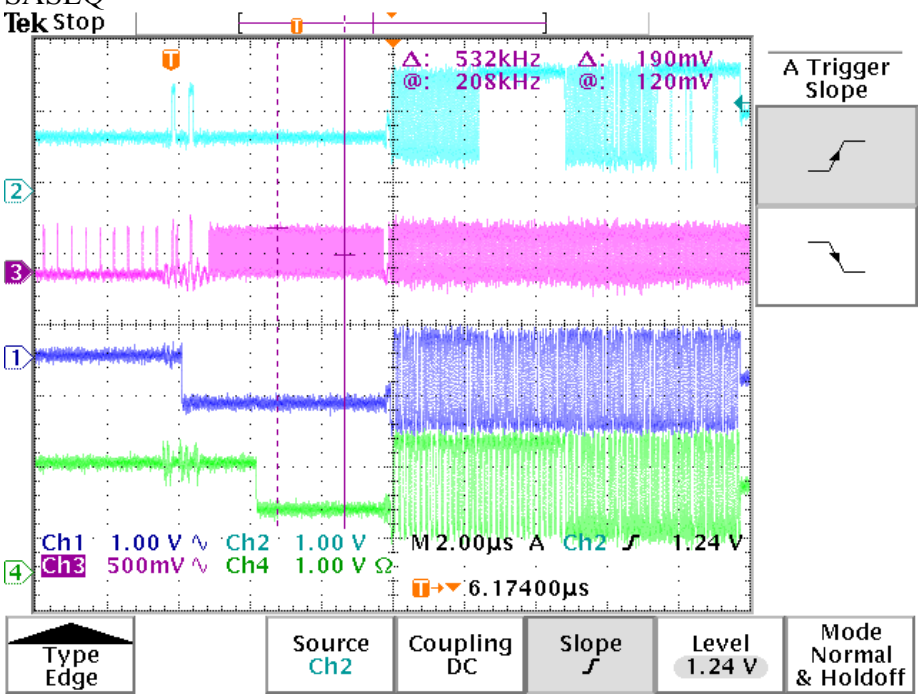


Seq : PRD1, CLK, Cnt_Reset

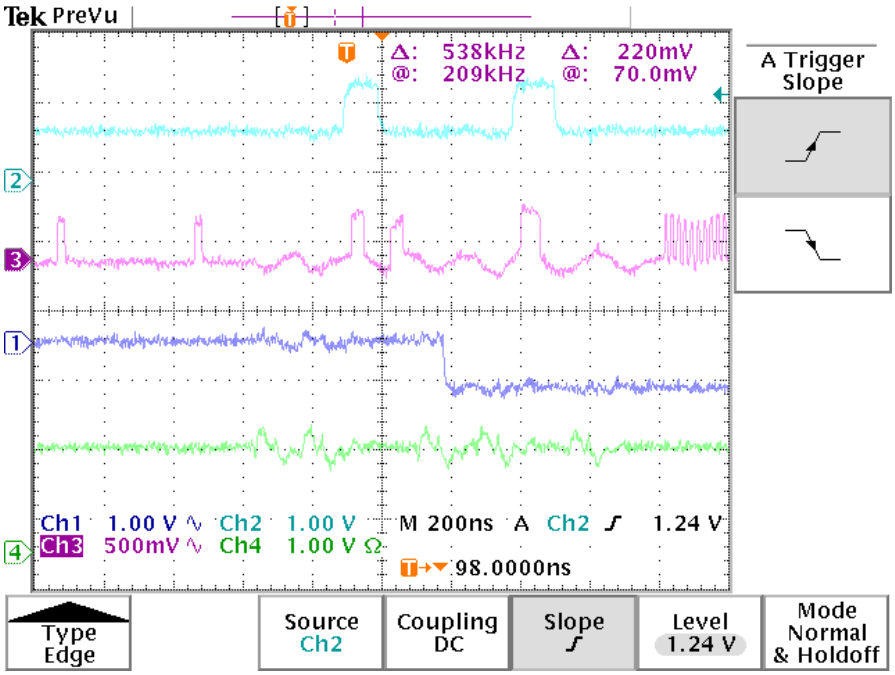


Seq : PRD1, CLK, Cnt_Reset

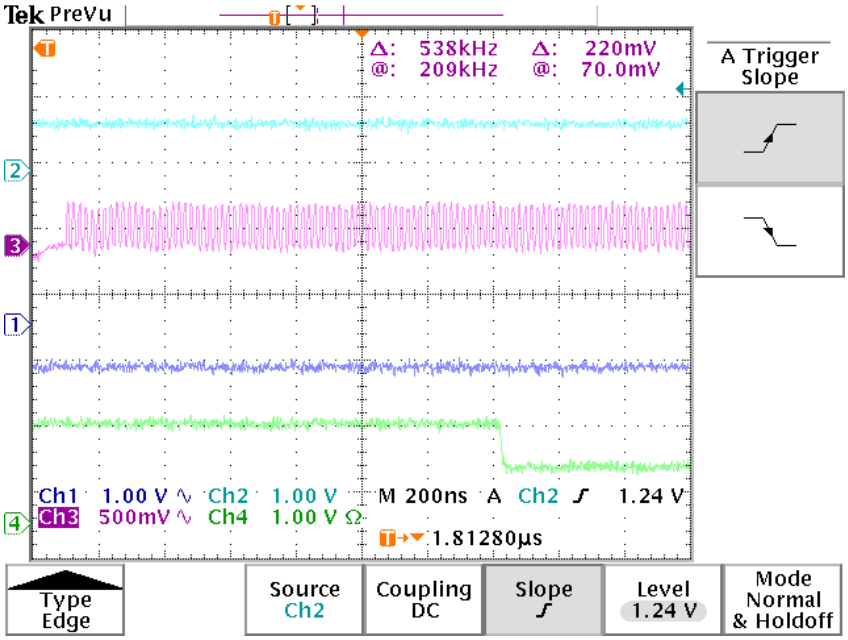
SASEQ



SASEQ : PRD1, CLK, Cnt_Reset



SASEQ : PRD1, CLK, D0/1/3



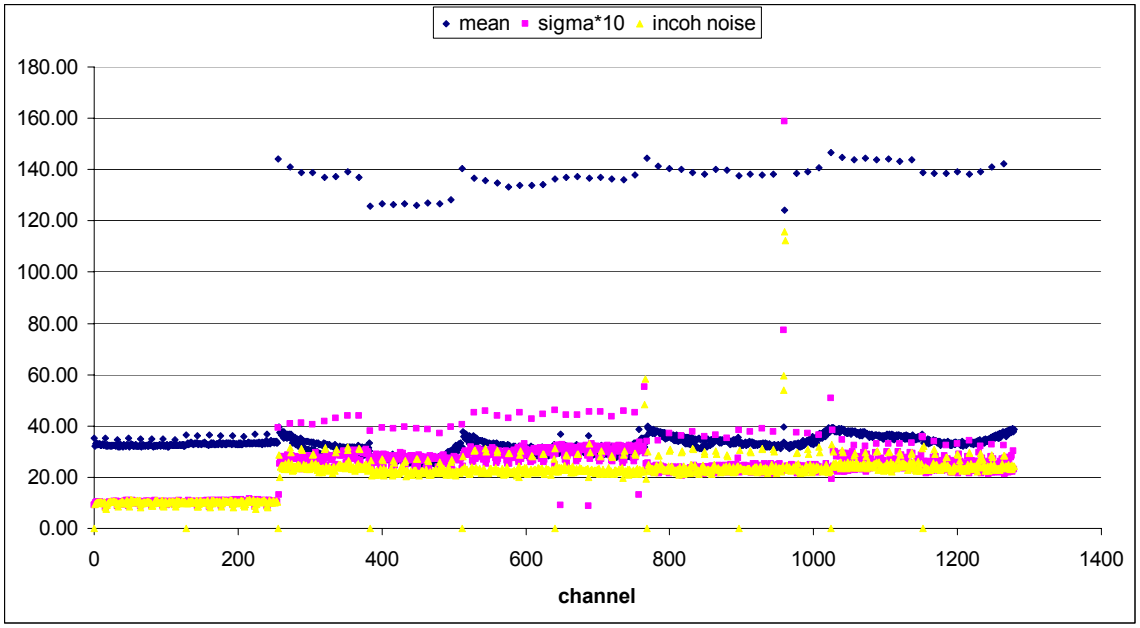
SASEQ : PRD1, CLK, Cnt_Reset

Noticed two apparent differences :

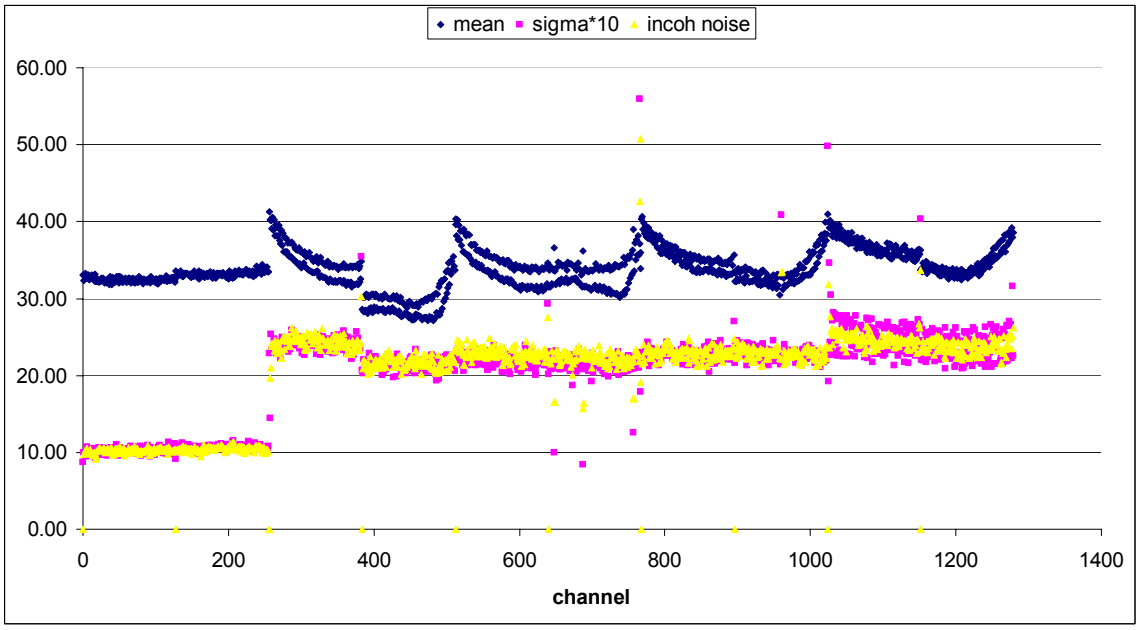
a) digitize clock starts much in advance for SASEQ (~50 cycles vs ~8)
b) for Seq Cnt_Reset happens after ~ 6 usec after going to Digitize while for SASEQ it happens after 2 usec. May be because of SVX2 ?

4/28/05 DS, AN

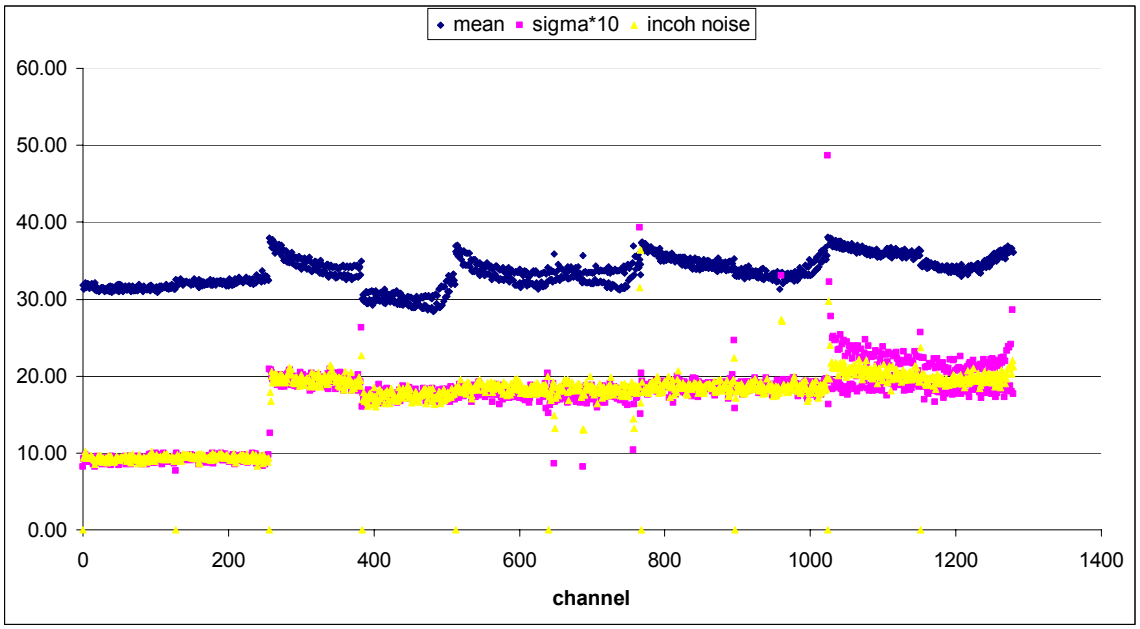
T = -6.4 C Bias Voltage = 50V Current = 70nA (typically 300nA at room Temp)
Default Values: Pipeline = 3 PABW = 4 Preamp Current = 4



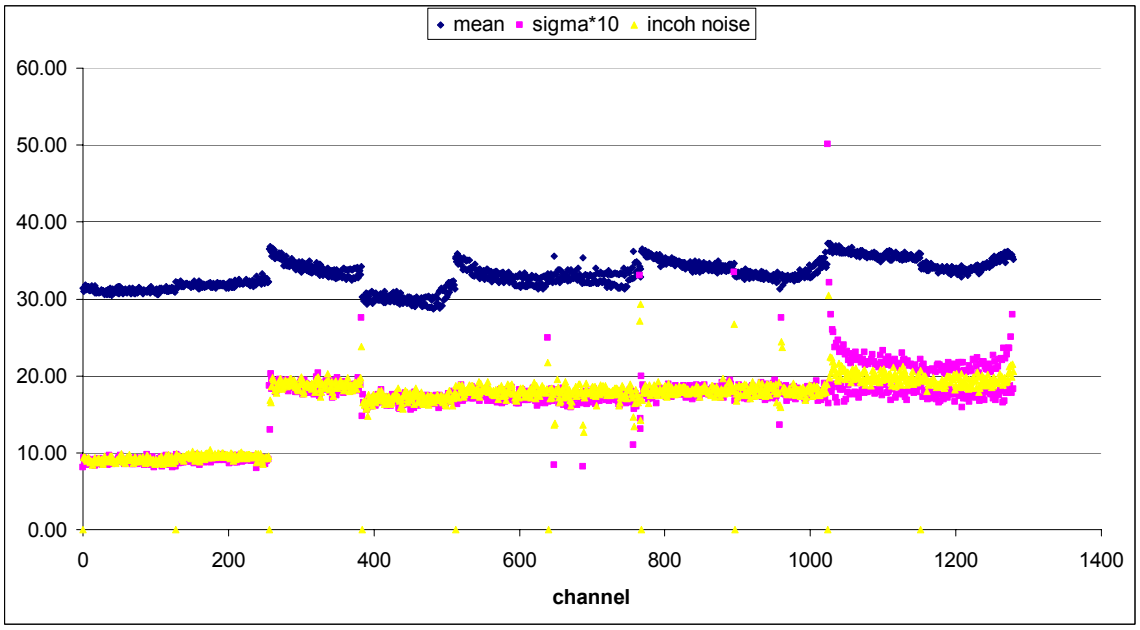
T= -6.4 C Bias Voltage = 50V Current = 70nA
Pipeline = 5 PABW = 4 Preamp Current = 4



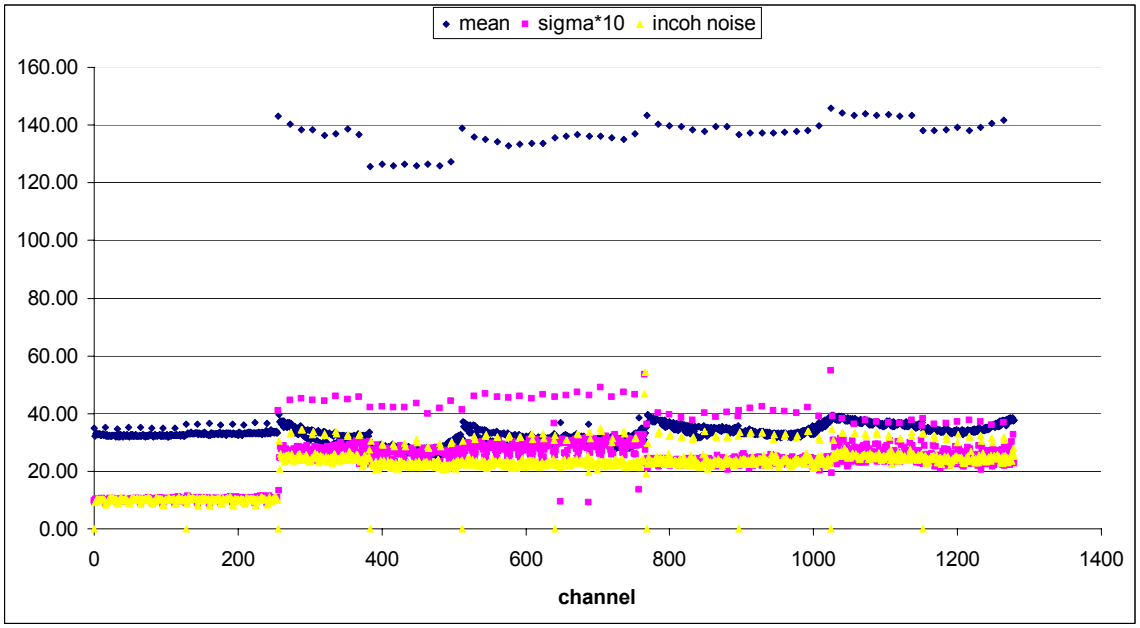
T= -6.4 C Bias Voltage = 50V Current = 70nA
Pipeline = 5 PABW = 15 Preamp Current = 4



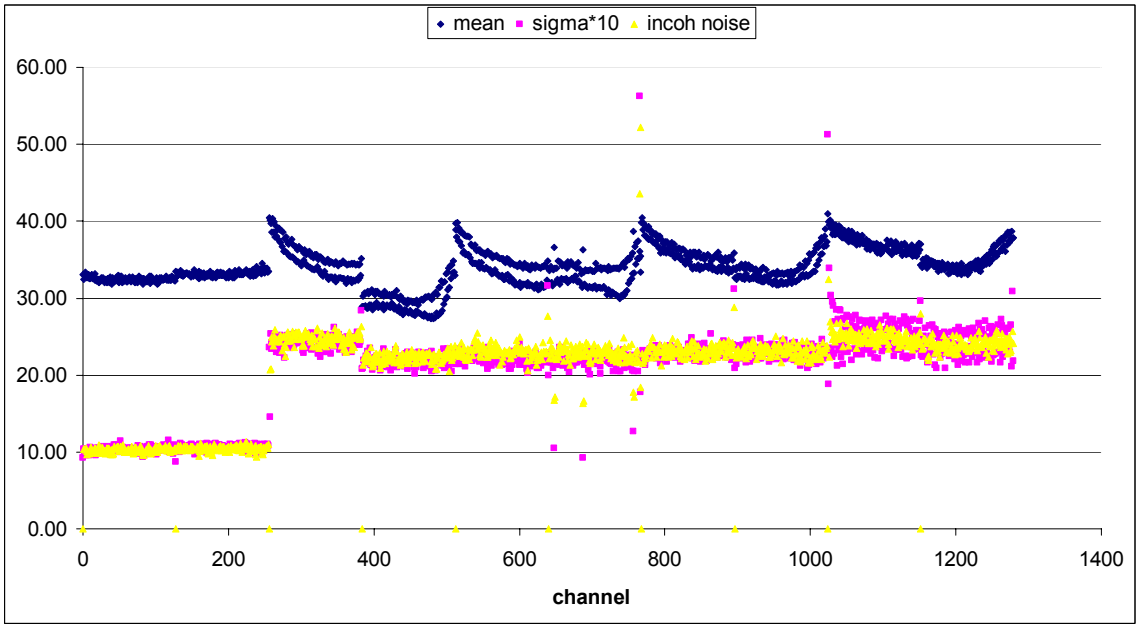
T= -6.4 C Bias Voltage = 50V Current = 70nA
Pipeline = 5 PABW = 15 Preamp Current = 0



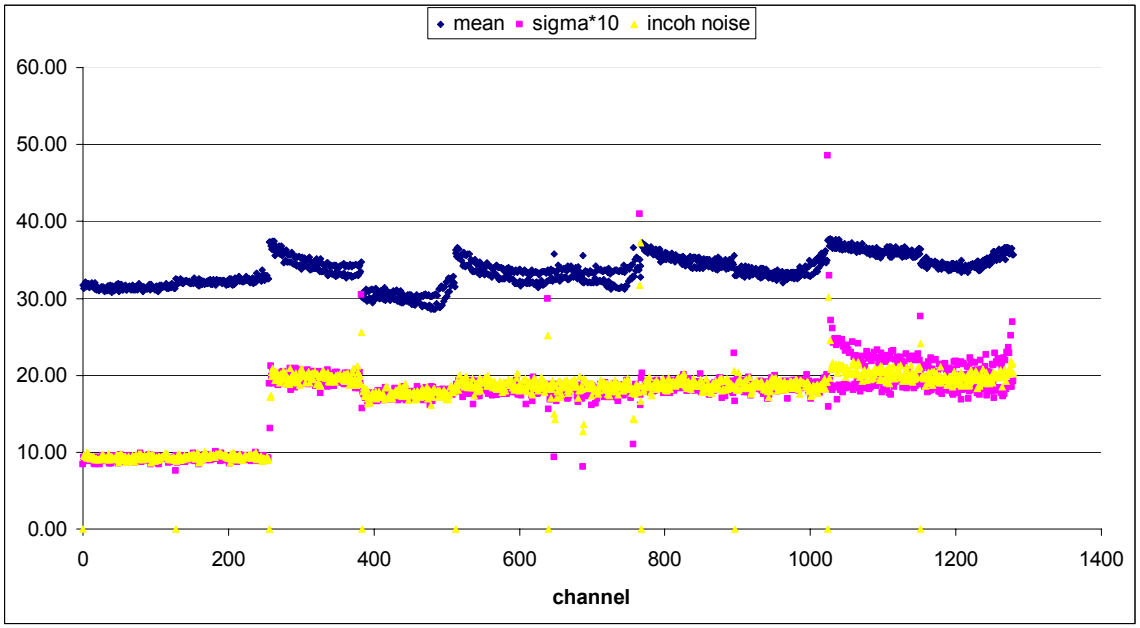
T = +6.2 C Bias Voltage = 50V Current = 80nA (typically 300nA at room Temp)
Default Values: Pipeline = 3 PABW = 4 Preamp Current = 4



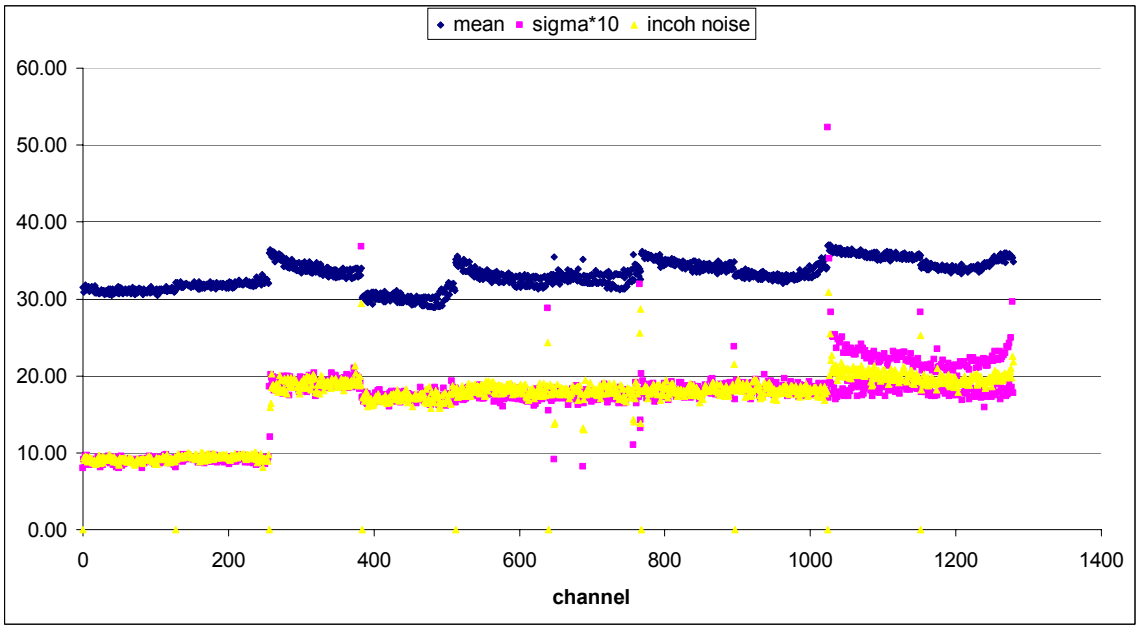
T = +6.2 C Bias Voltage = 50V Current = 80nA (typically 300nA at room Temp)
Pipeline = 5 PABW = 4 Preamp Current = 4



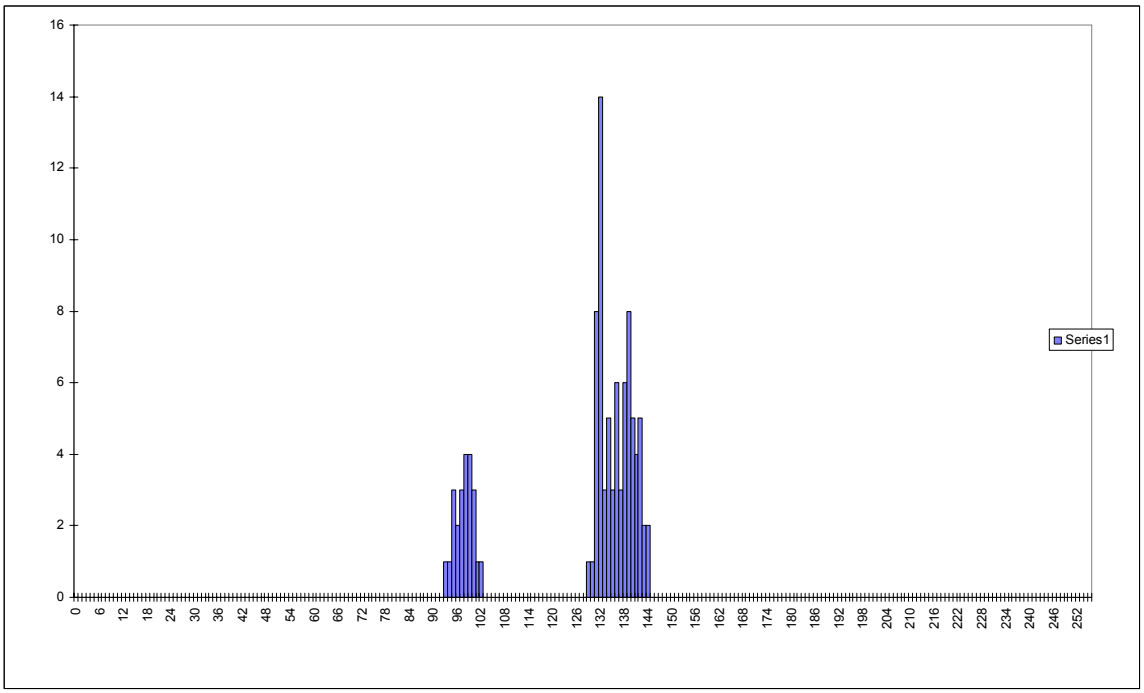
T = +6.2 C Bias Voltage = 50V Current = 80nA (typically 300nA at room Temp)
Pipeline = 5 PABW = 15 Preamp Current = 4



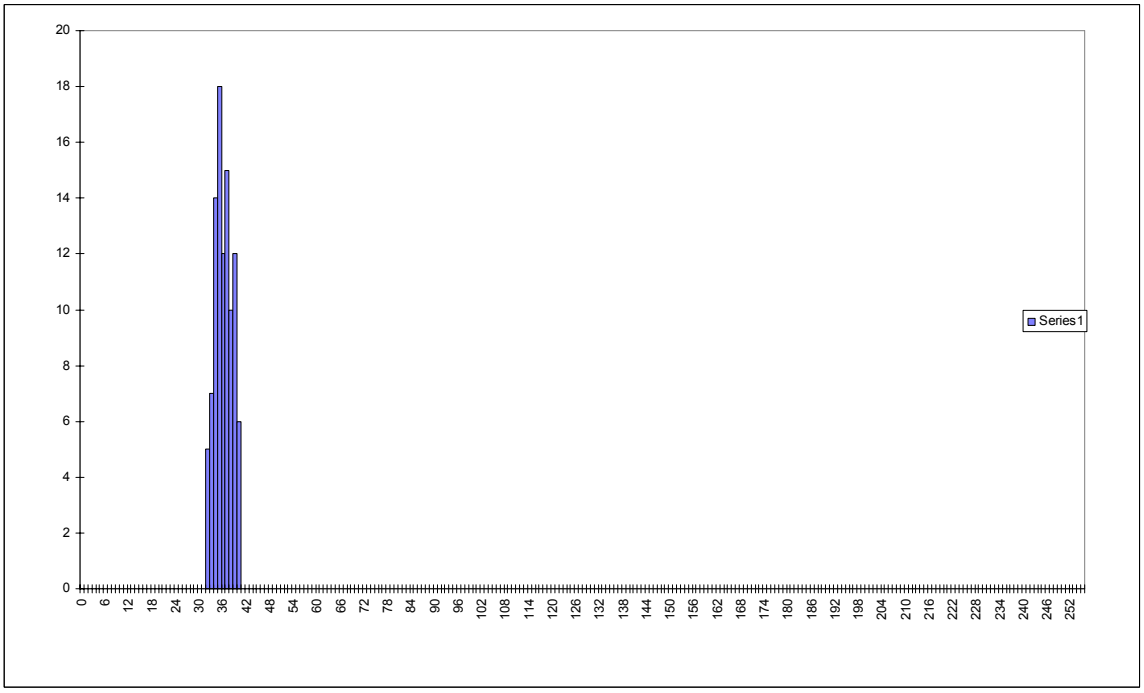
T = +6.2 C Bias Voltage = 50V Current = 80nA (typically 300nA at room Temp)
Pipeline = 5 PABW = 15 Preamp Current = 0



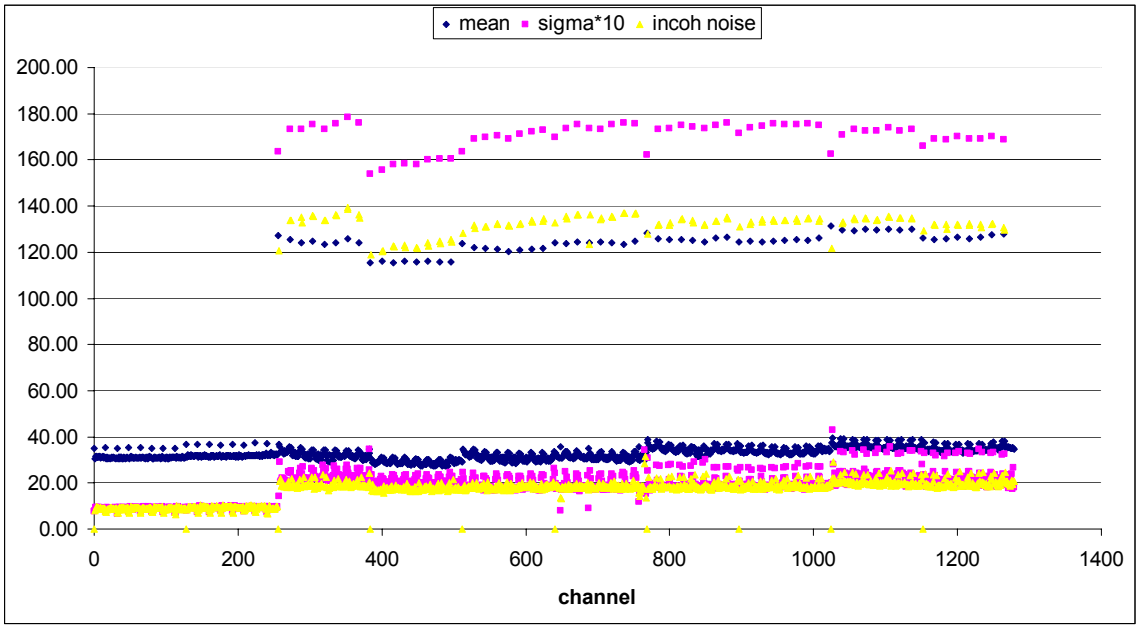
Channel 16



channel 17

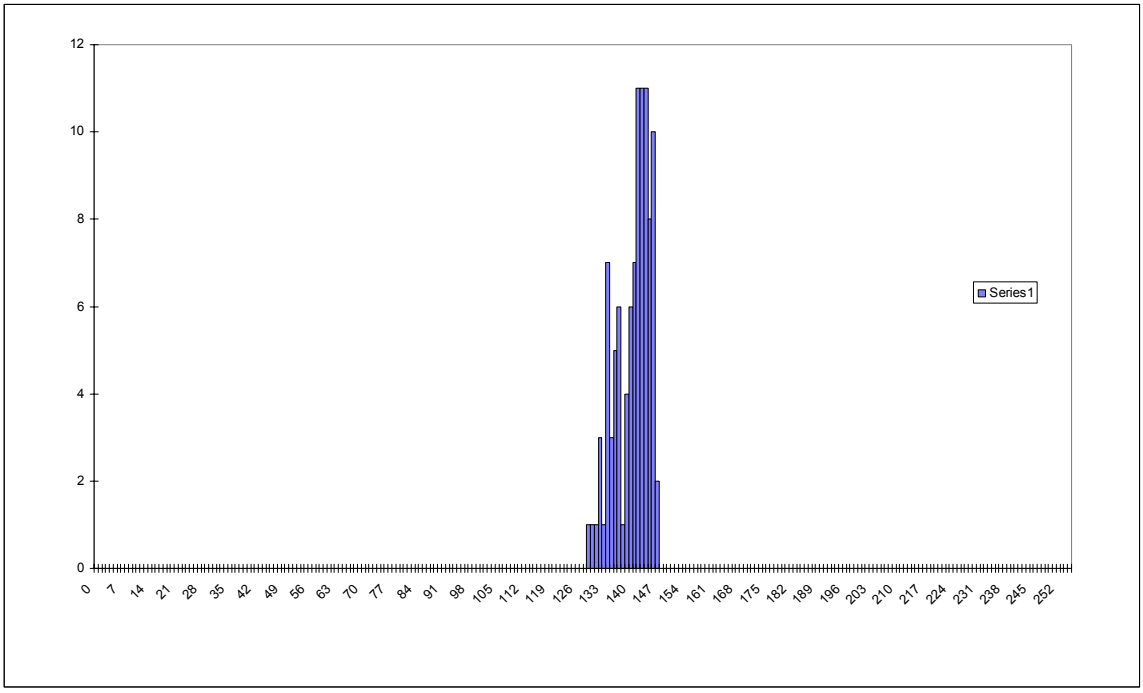


T = +6.2C Current = 80nA
Pipeline = 3 PABW = 15 Preamp Current = 0

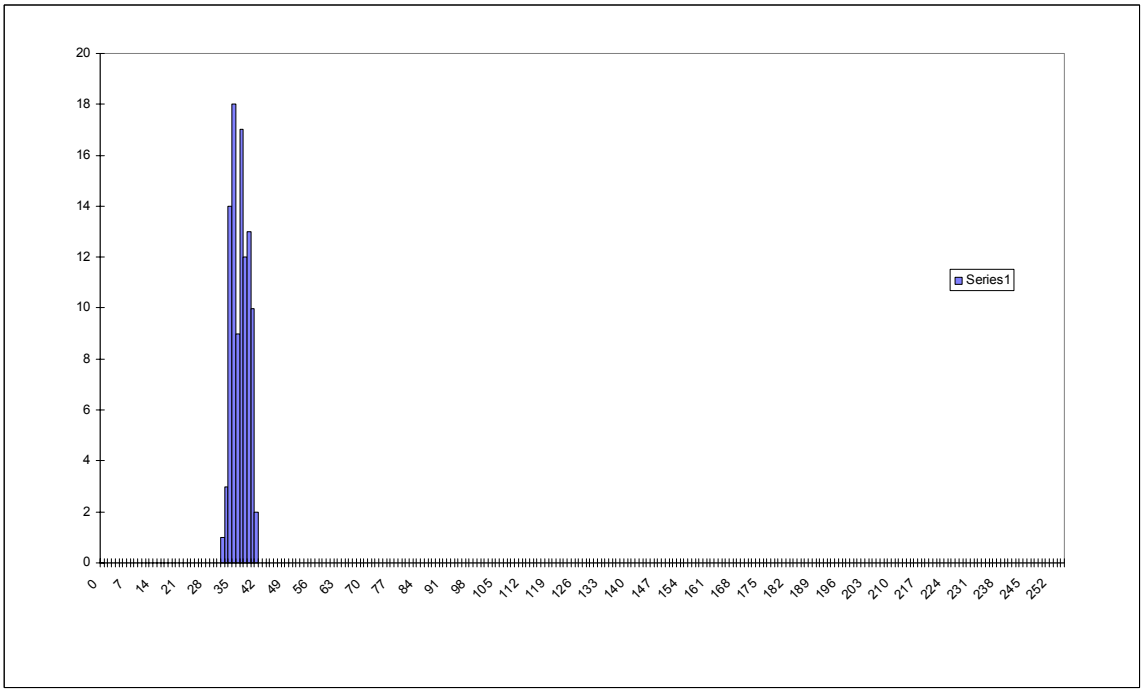


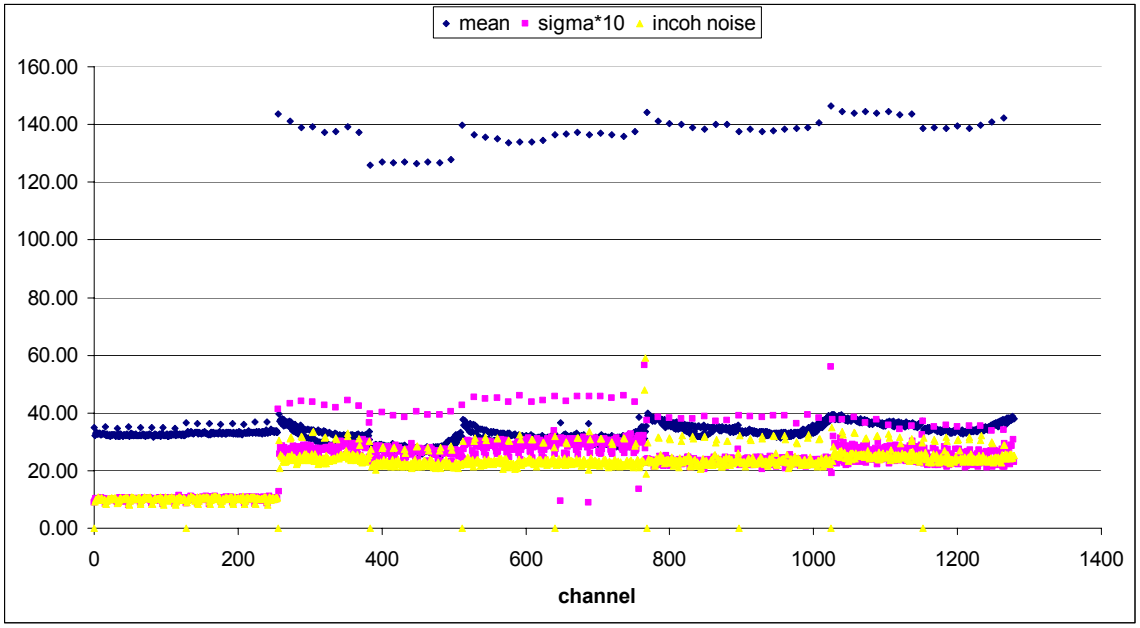
T = 1C Current = 50nA Bias Voltage = 50V
Default Settings

Channel 16



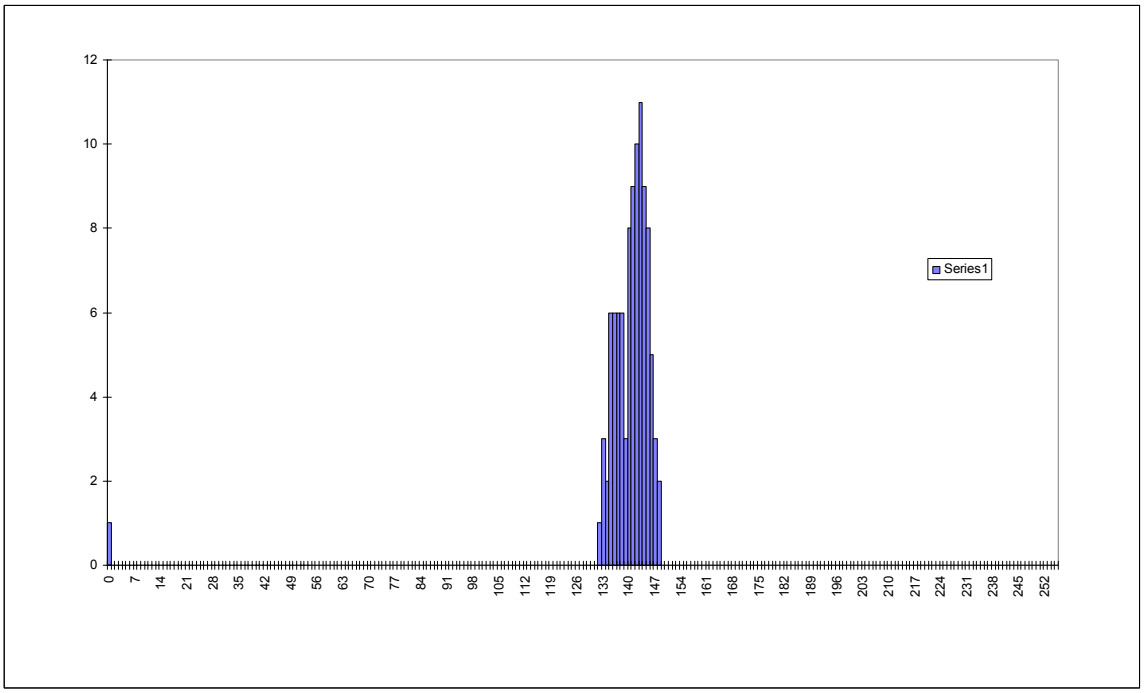
channel 17



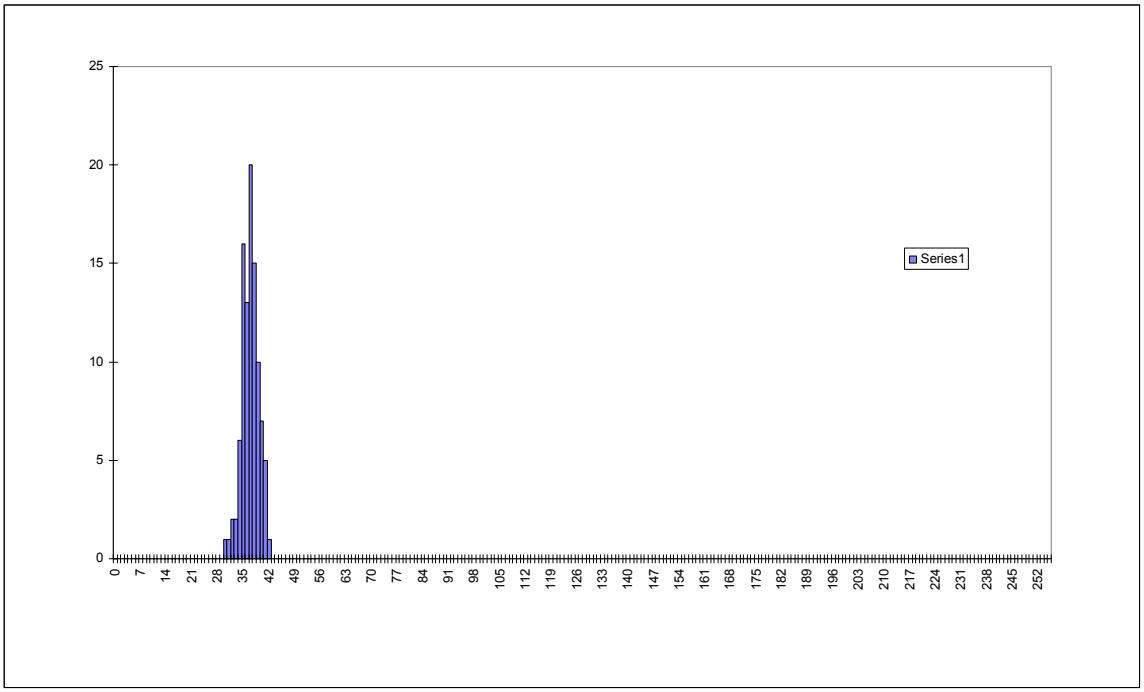


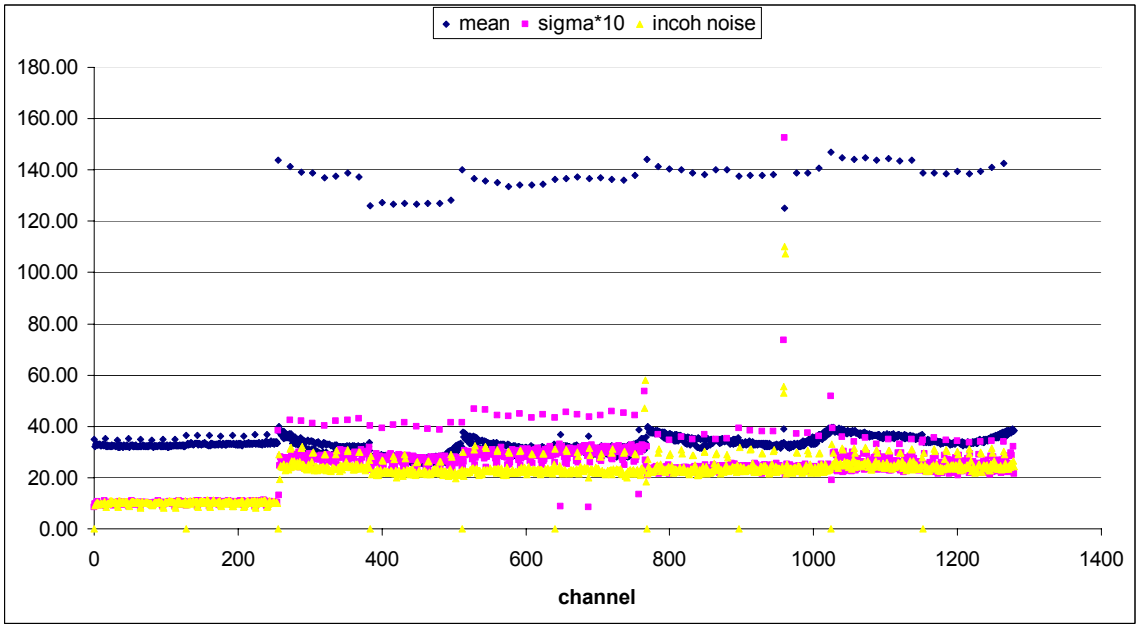
T = -2C Current = 50nA Bias Voltage = 50V
Default Settings

Channel 16



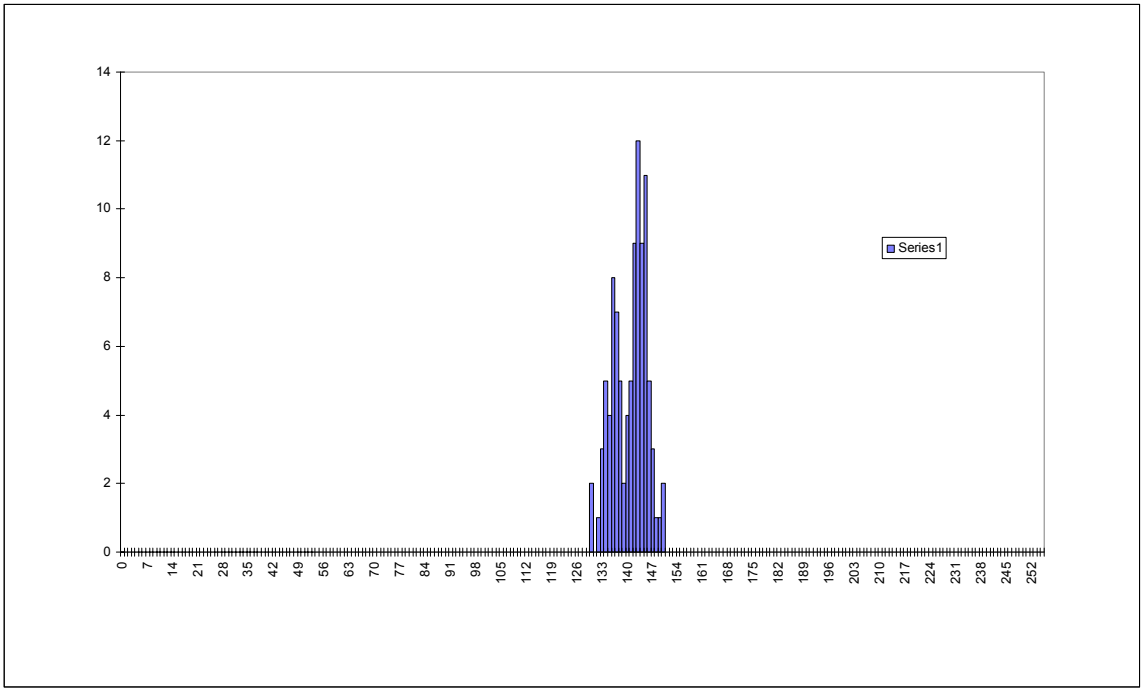
channel 17



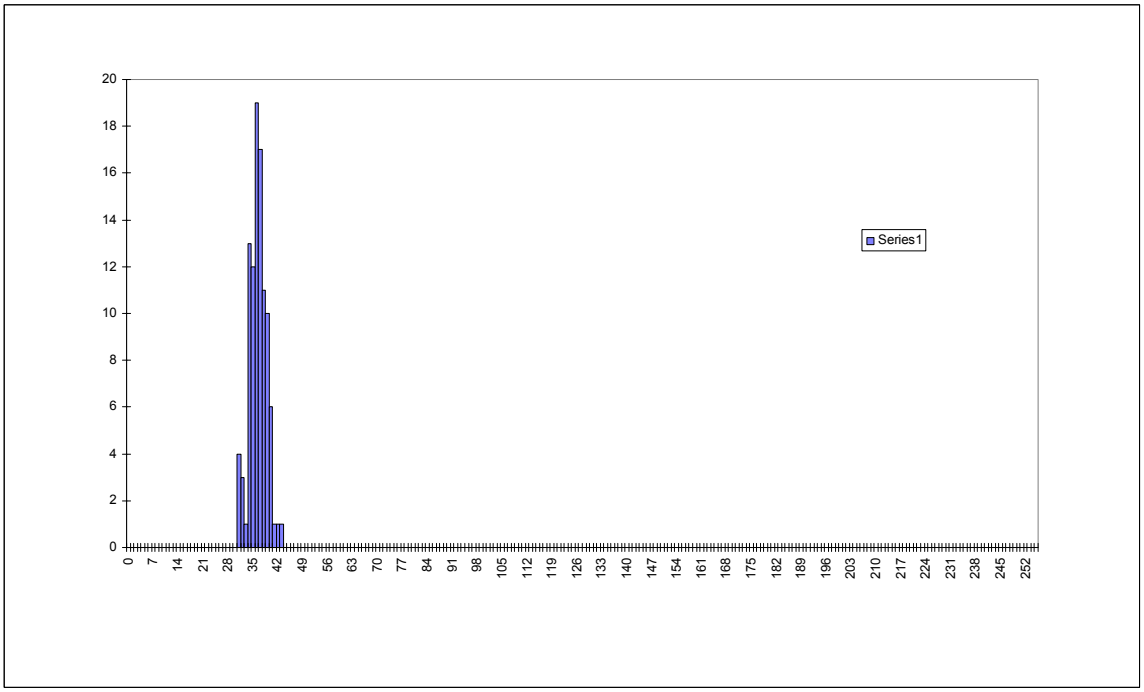


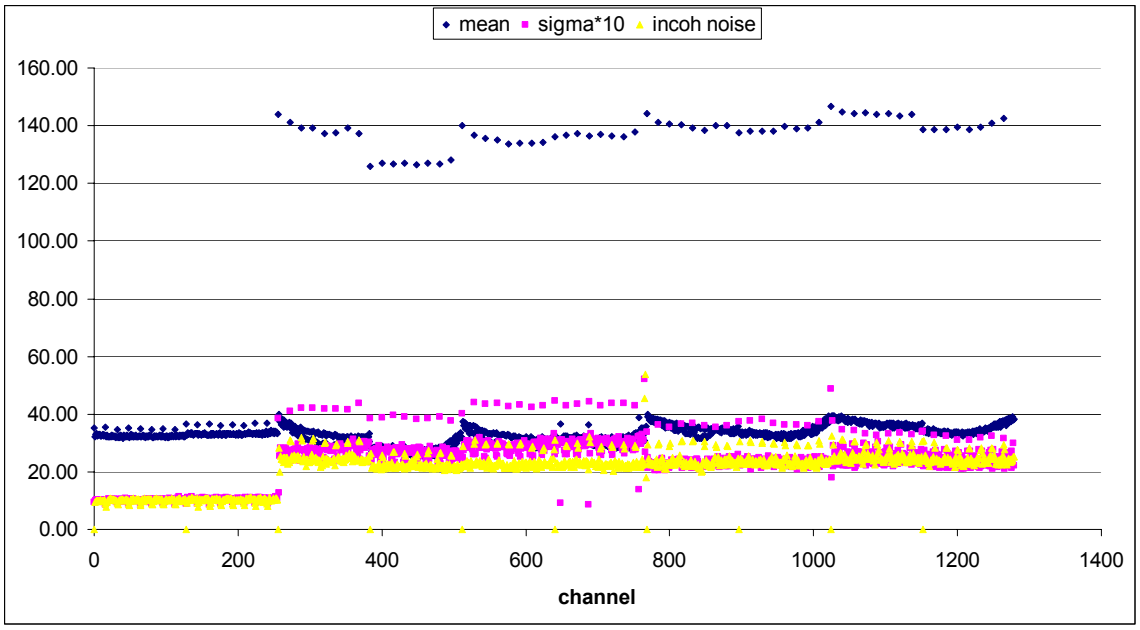
T = -3C Current = 50nA Bias Voltage = 50V
Default Settings

Channel 16



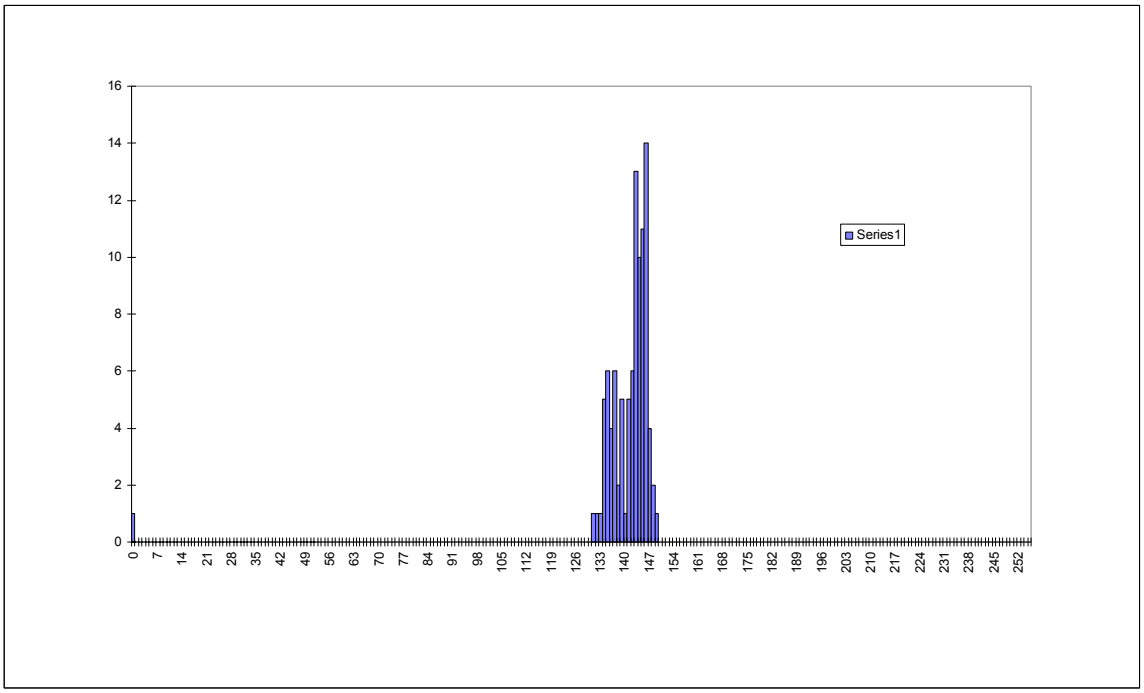
channel 17



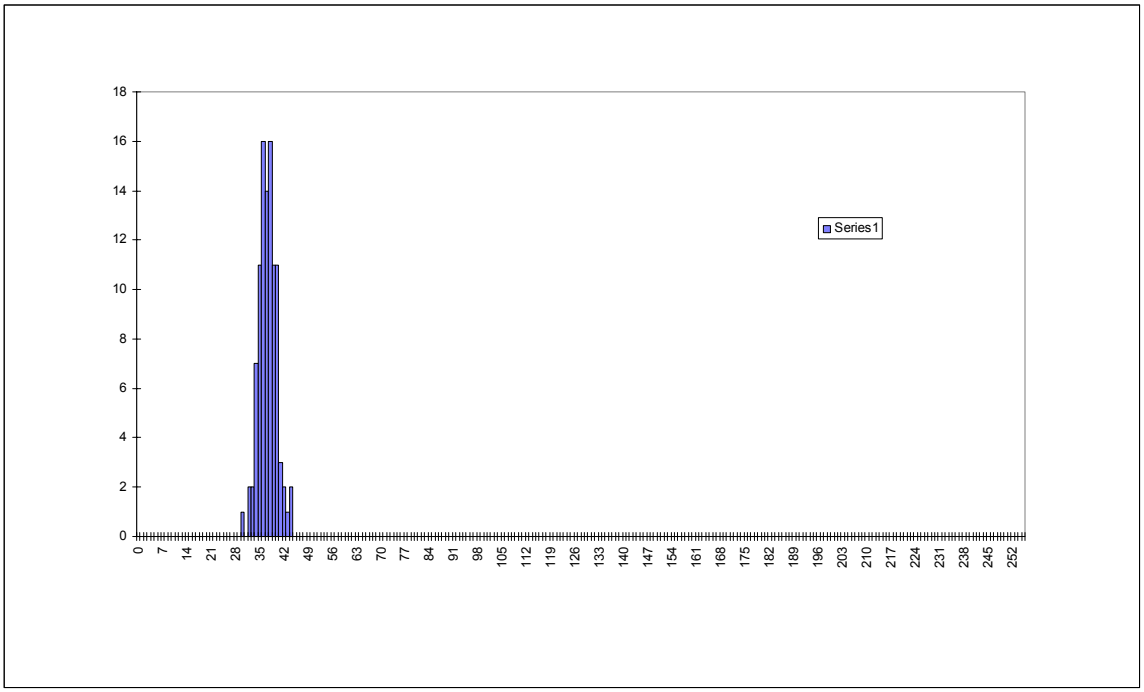


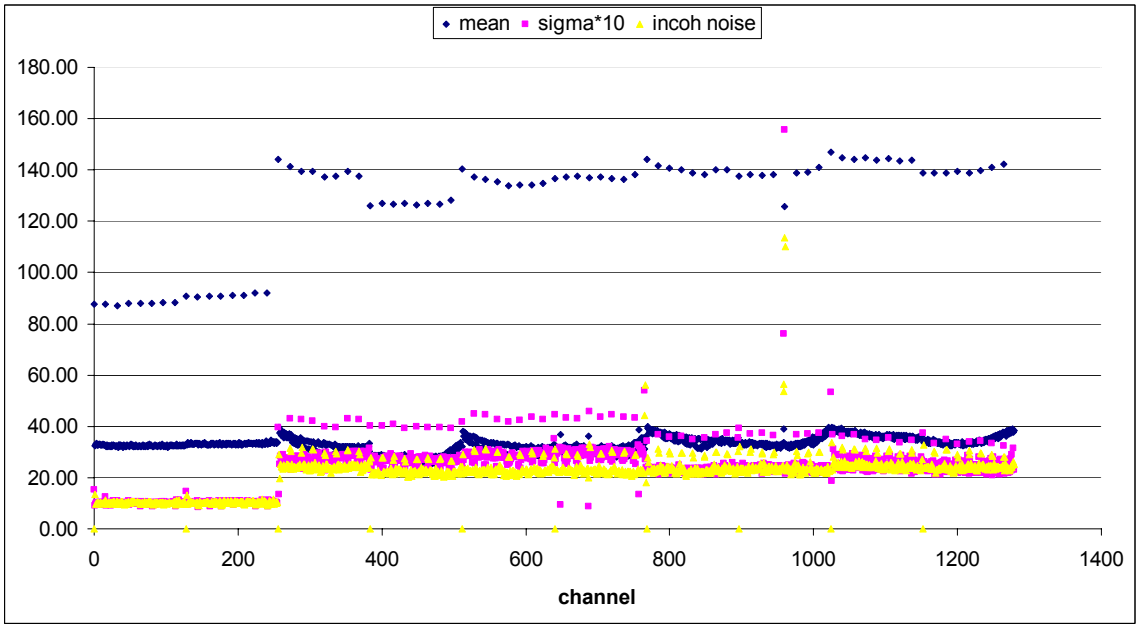
T = -4C Current = 50nA Bias Voltage = 50V
Default Settings

Channel 16



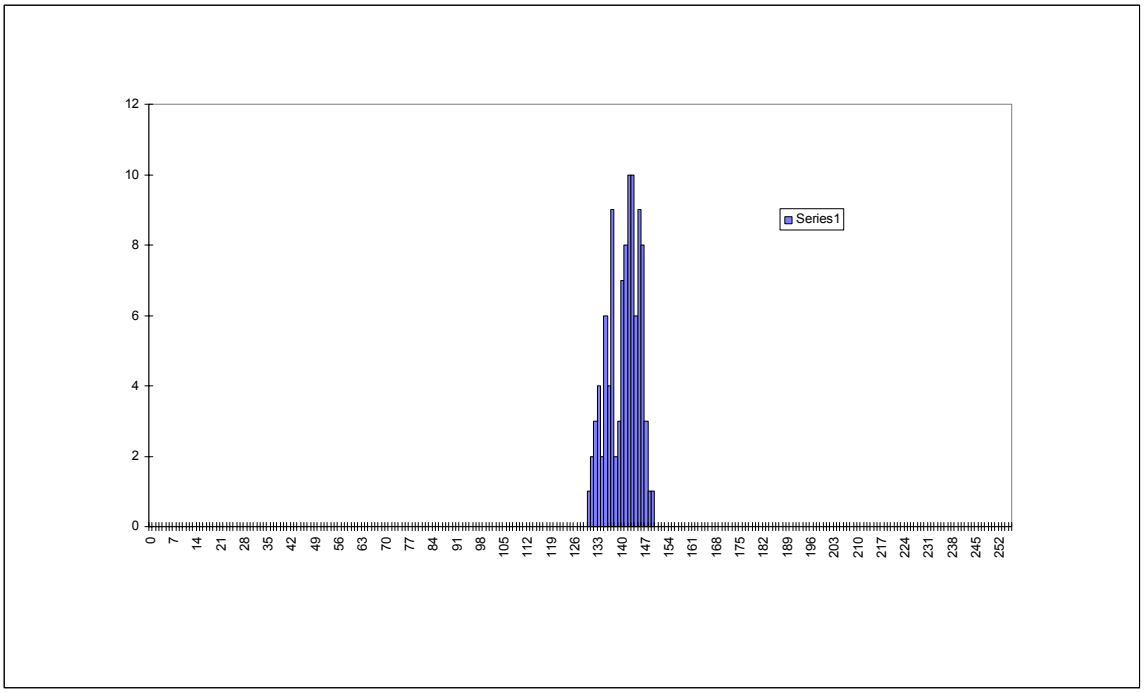
channel 17



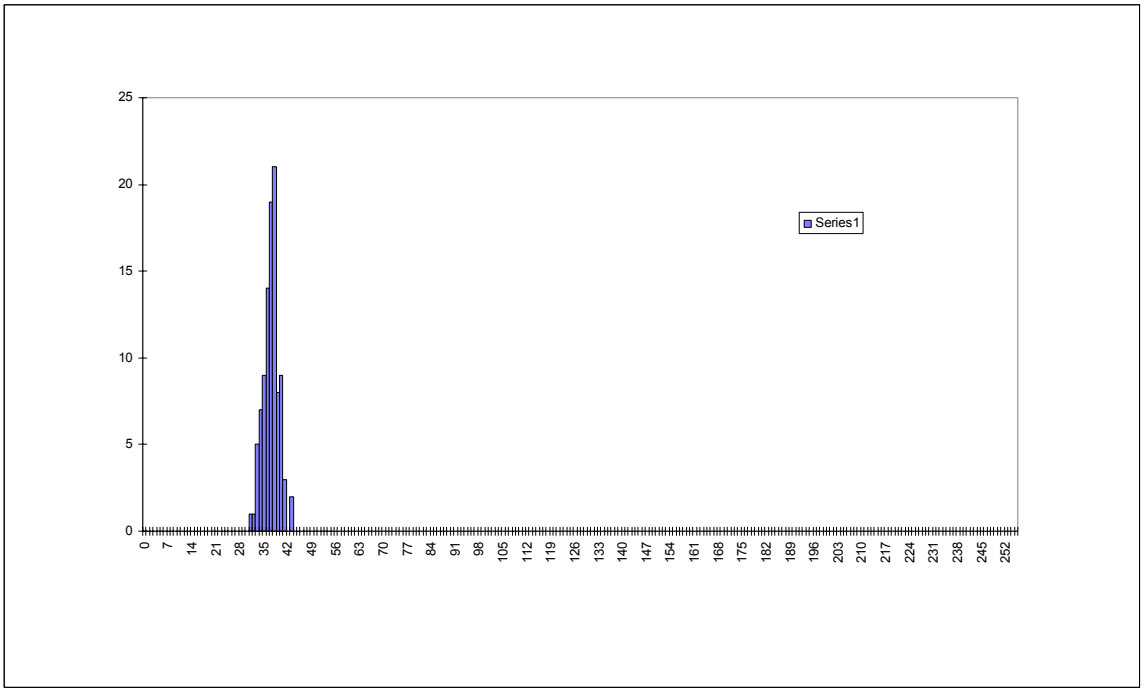


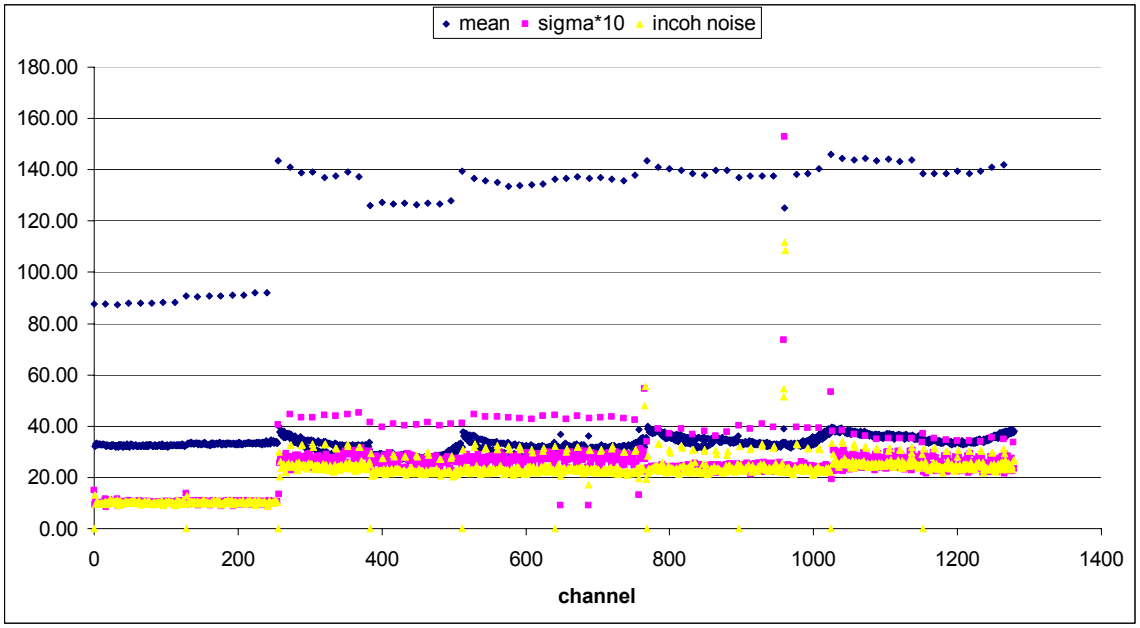
T = +4C Current = 50nA Bias Voltage = 50V
Default Settings

channel 16



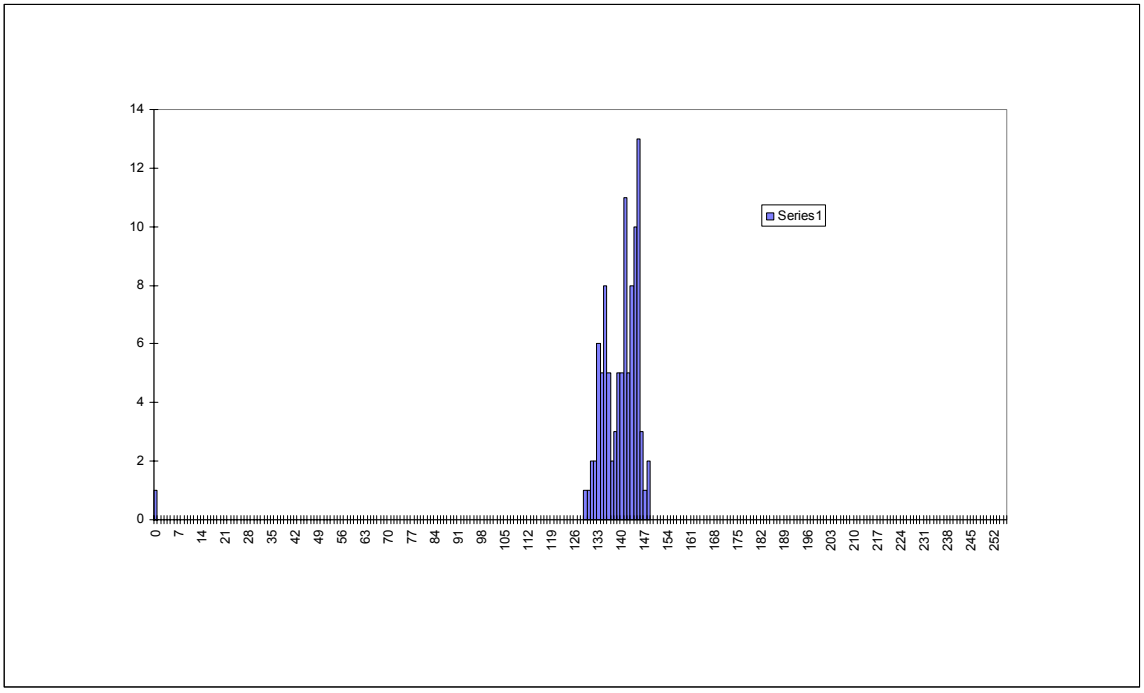
channel 17



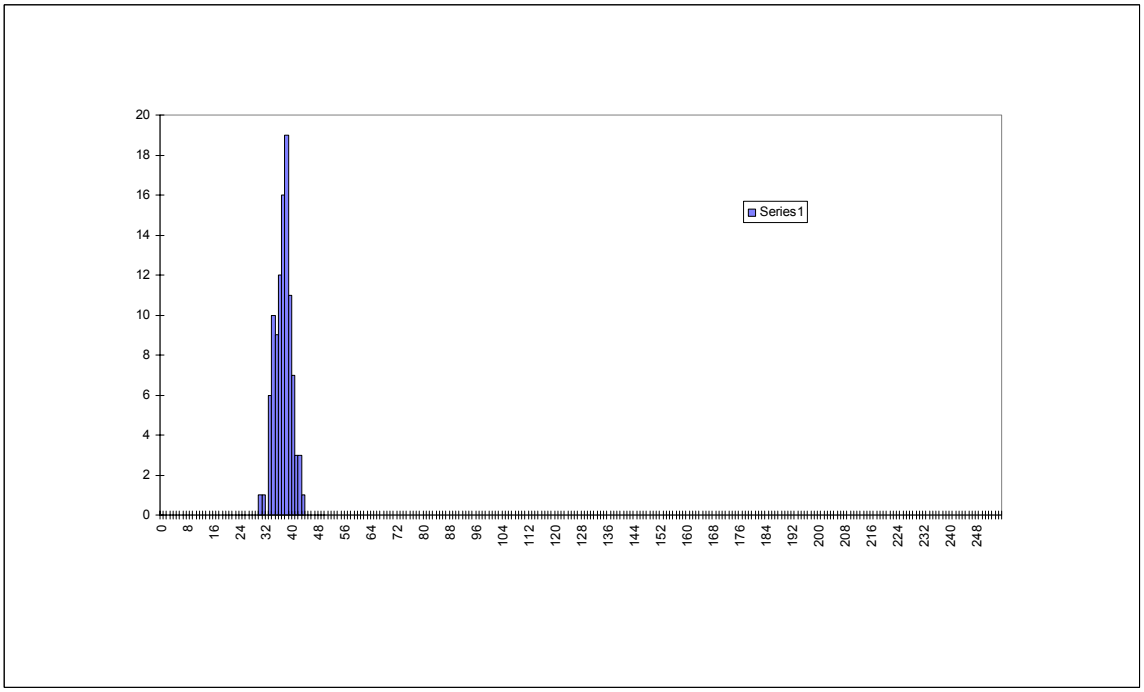

mean
sigma*10
incoh noise
180.00
160.00
140.00
120.00
100.00
80.00
60.00
40.00
20.00
0.00
0
200
400
600
800
1000
1200
1400
channel

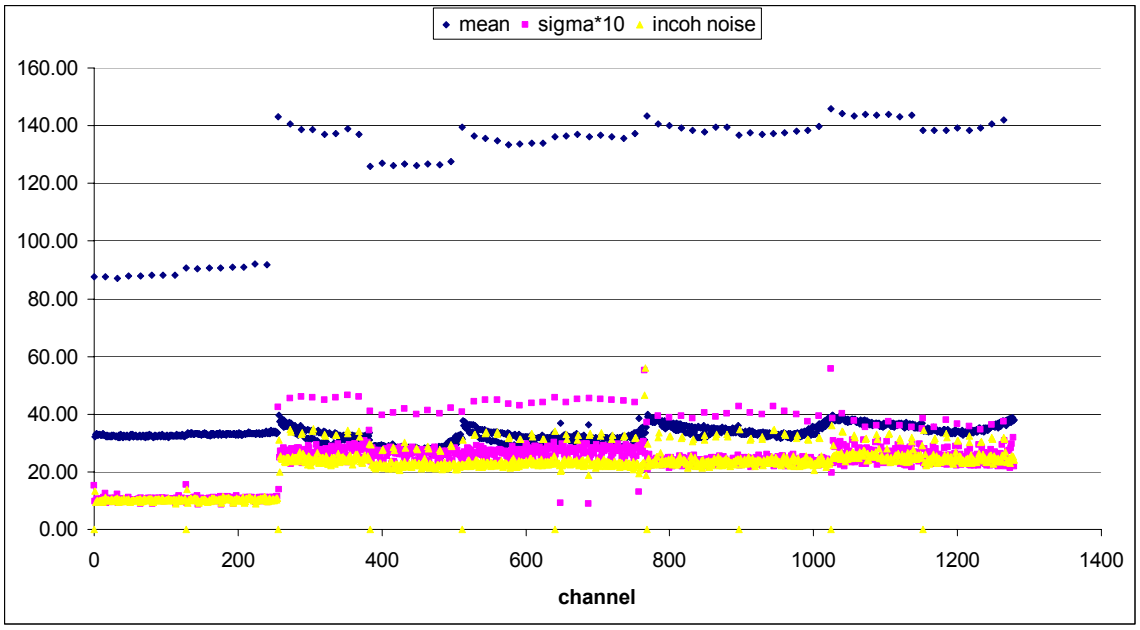
T = +6C Current = 50nA Bias Voltage = 50V
Default Settings

Channel 16

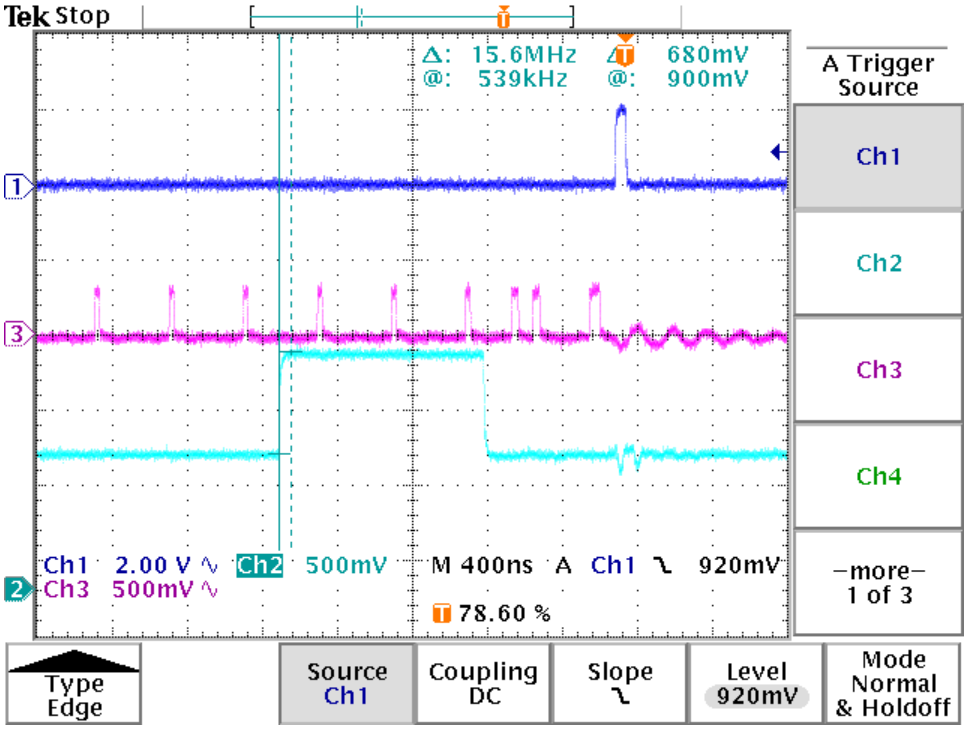


channel 17

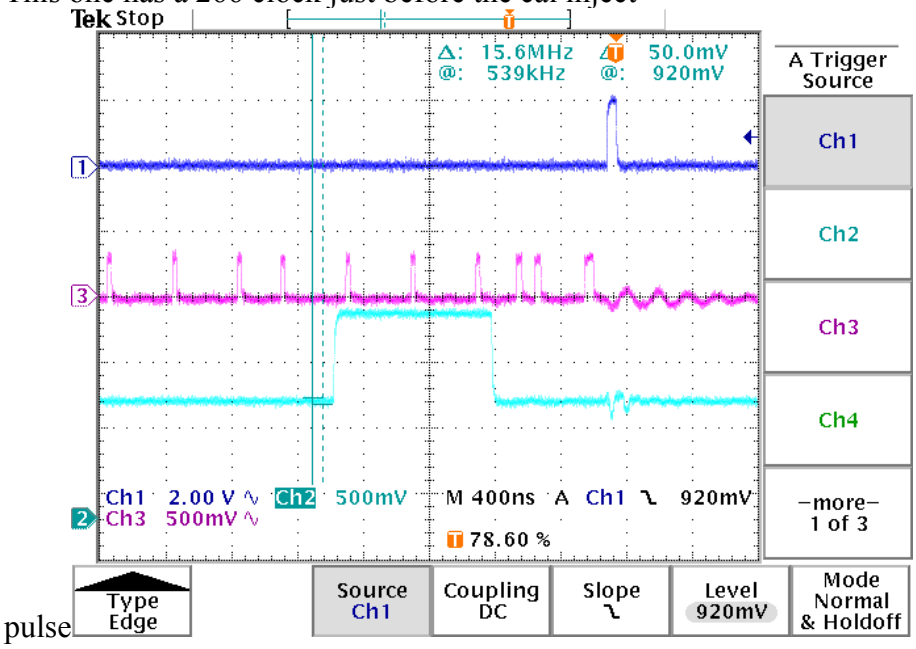



mean
sigma*10
incoh noise
160.00
140.00
120.00
100.00
80.00
60.00
40.00
20.00
0.00
0
200
400
600
800
1000
1200
1400
channel

Trigger on change mode, look at CAL SR line and clock pulse, this comes in middle of clock width

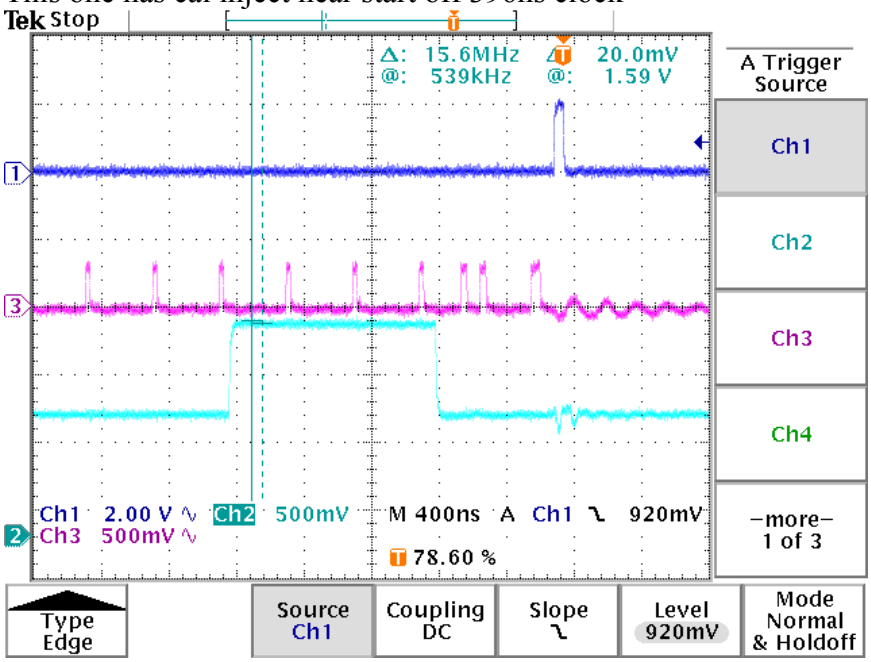


This one has a 266 clock just before the cal inject

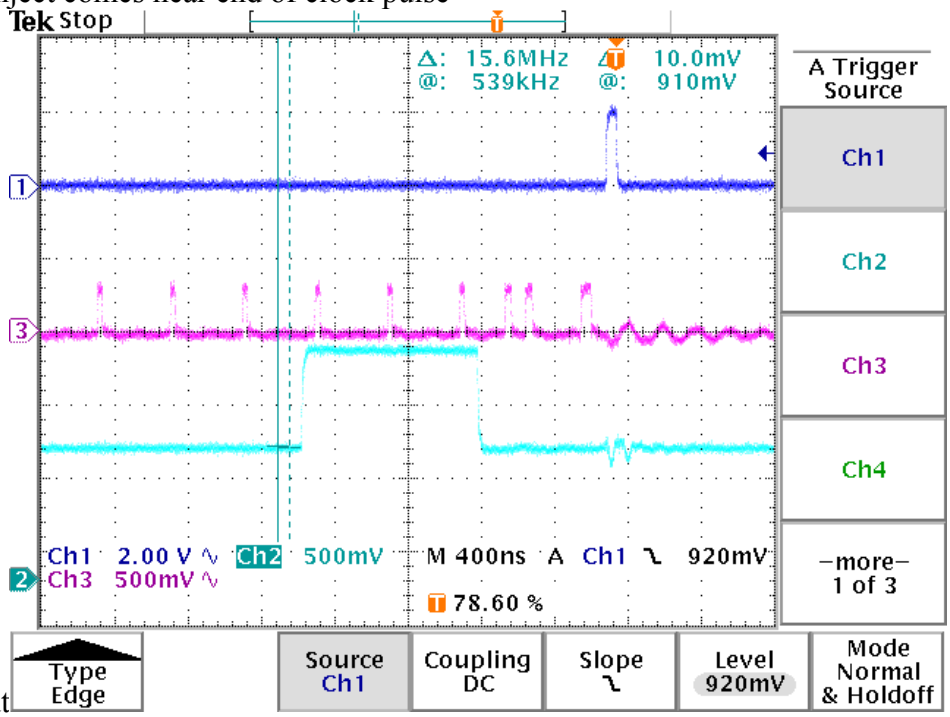


pulse

This one has cal inject near start off 396ns clock

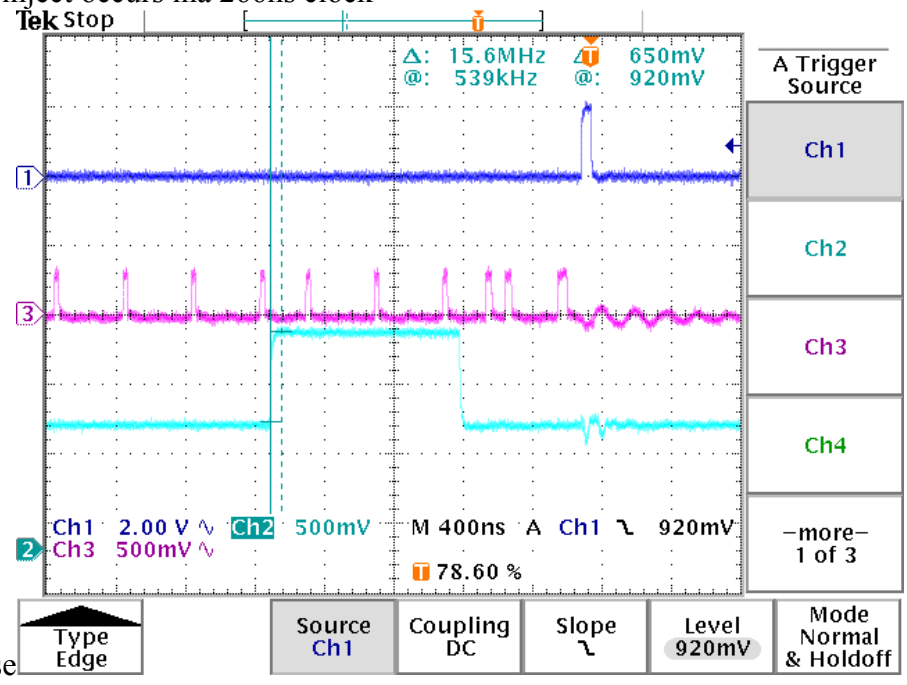


al inject comes near end of clock pulse

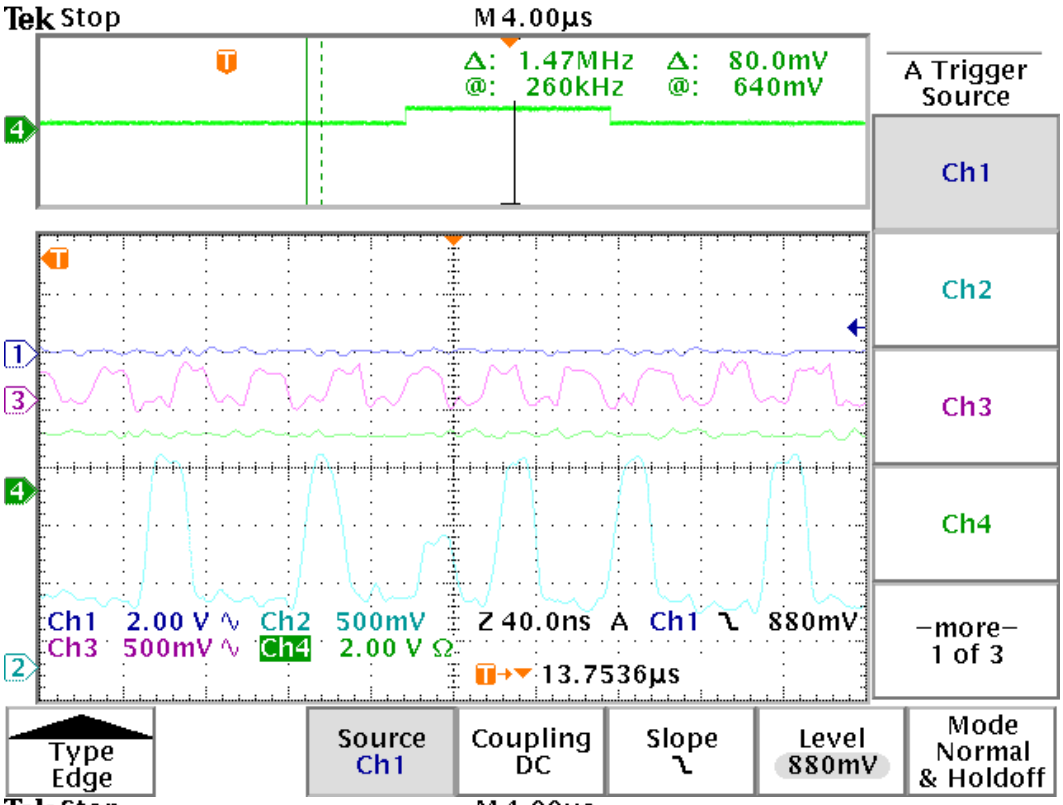


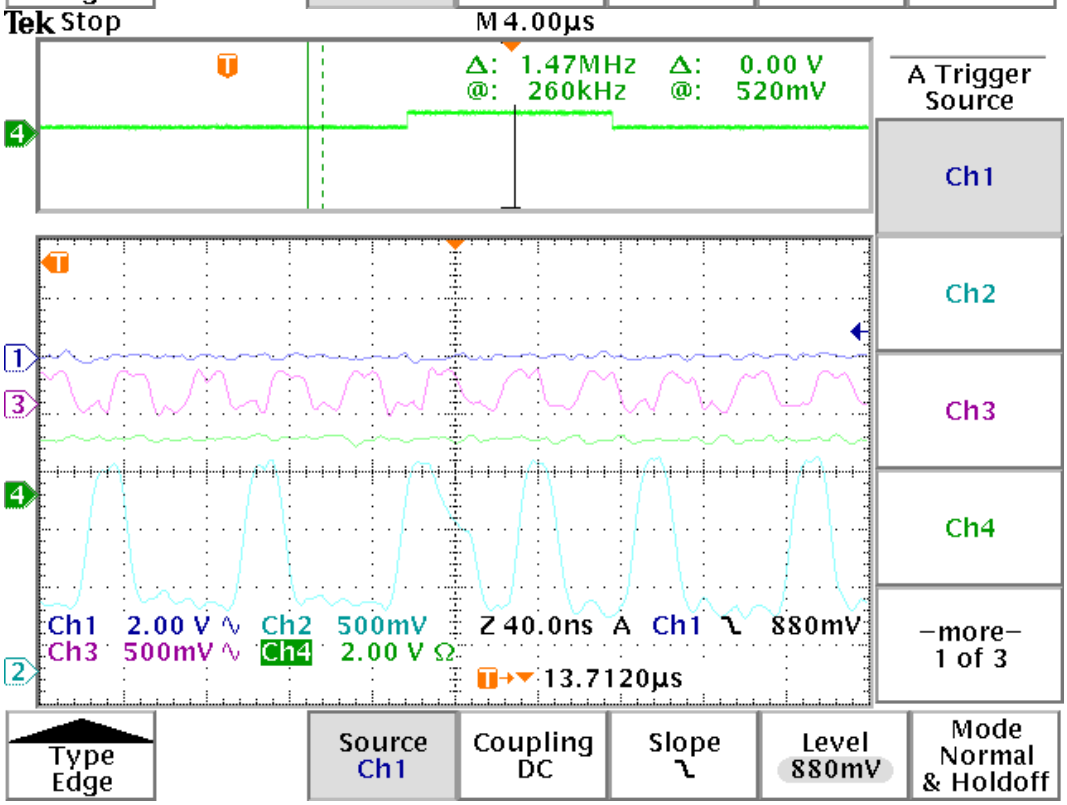
widt

Cal inject occurs ina 266ns clock



pulse


Tek Stop
M 4.00µs
Δ: 1.47MHz Δ: 80.0mV
@: 260kHz @: 640mV
A Trigger Source
Ch1
Ch2
Ch3
Ch4
Ch1 2.00 V Ch2 500mV Z 40.0ns A Ch1 880mV
Ch3 500mV Ch4 2.00 V Ω
13.7536µs
–more–
1 of 3
Type Edge
Source Ch1
Coupling DC
Slope
Level 880mV
Mode Normal & Holdoff

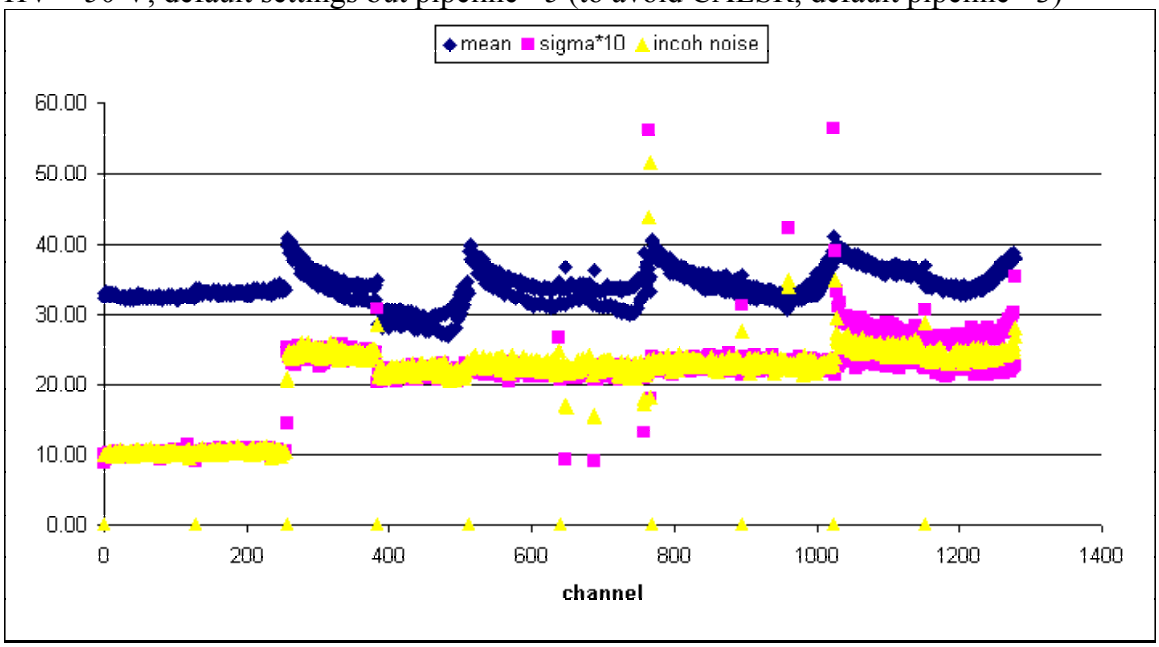

Tek Stop
M 4.00µs
Δ: 1.47MHz Δ: 0.00 V
@: 260kHz @: 520mV
A Trigger Source
Ch1
Ch2
Ch3
Ch4
Ch1 2.00 V Ch2 500mV Z 40.0ns A Ch1 880mV
Ch3 500mV Ch4 2.00 V Ω
13.7120µs
–more–
1 of 3
Type Edge
Source Ch1
Coupling DC
Slope
Level 880mV
Mode Normal & Holdoff

4/22/2005 DK, FG, AN
same configuration as yesterday. HV 50 V, Ibias ~ 160 nA. Scanned BW, ISEL parameter space taking ped and calinject runs for each point (BW =0,4,10,15; ISEL = 0,4,10,15).

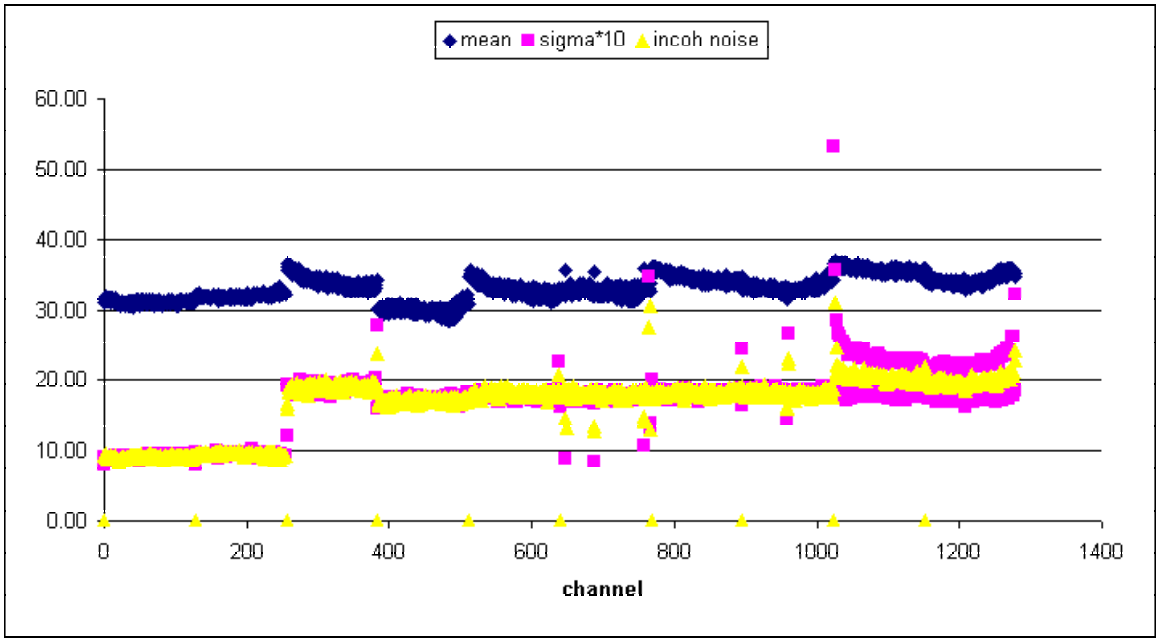
4/21/2005 AN

Connected all four modules to the new AC. The modules are connected in the following order : the module closest to Z=0 is read out first and so on sorted by Z location. Replaced the hybrid 246 -> hybrid 334.

HV = 50 V, default settings but pipeline =5 (to avoid CALSR, default pipeline =3)

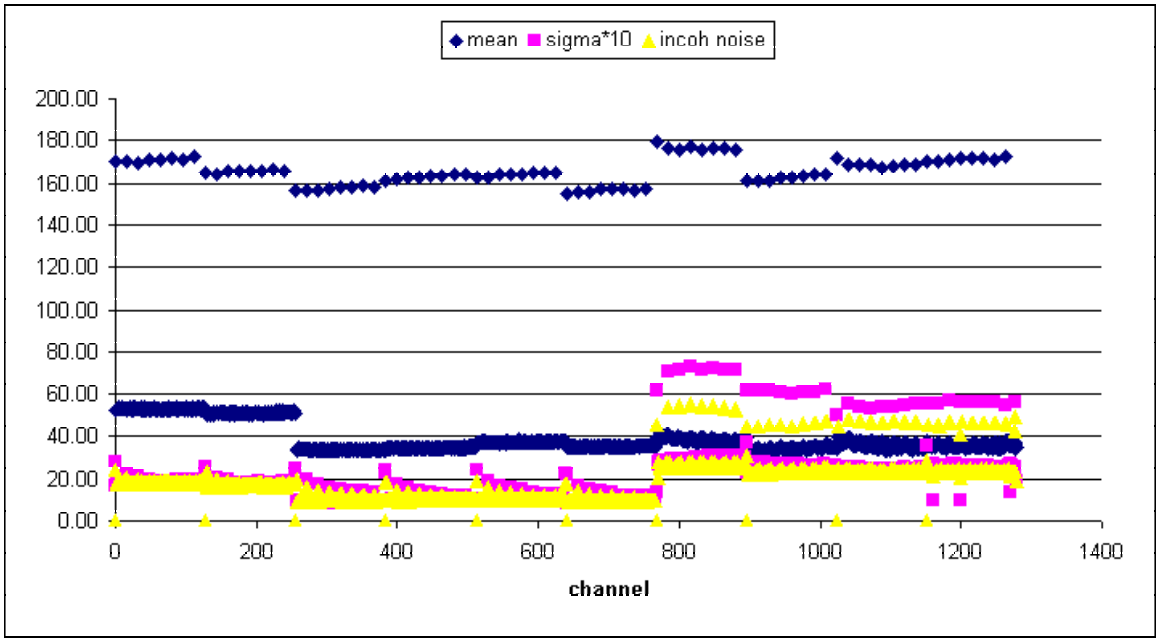


same as above but BW=15, Preamp Current=0



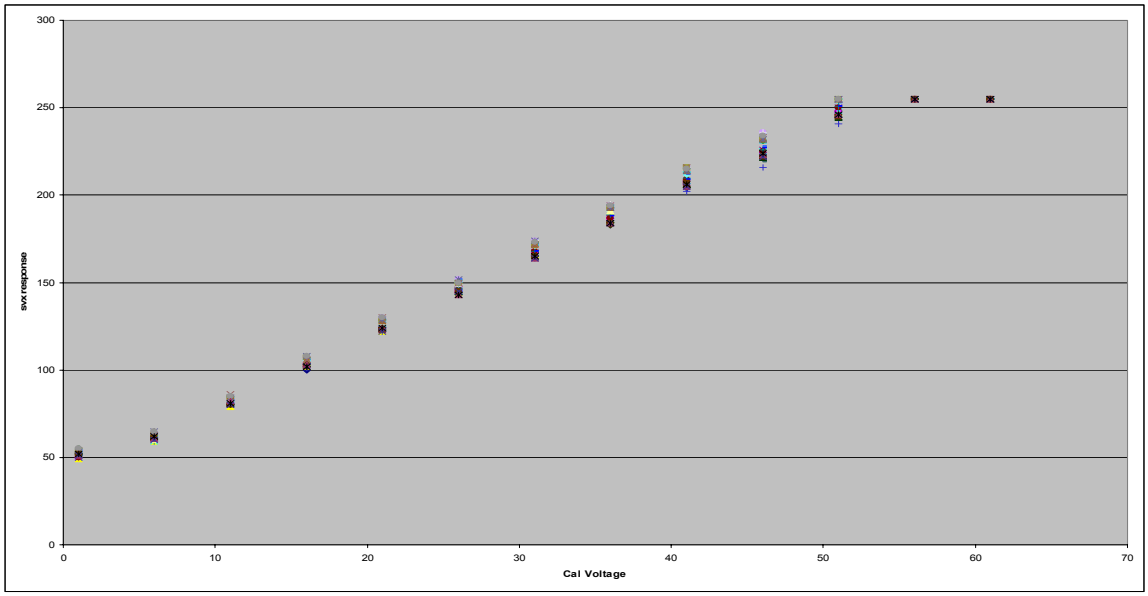
so
1) the mystery of the purple card is solved – it was the bad hybrid.
2) it is still not clear why the pedestals are lower
3) word count errors are still at 5%
4) we are ready for measurements with modules

4/20/05 AN : coherent noise for biased modules looks decent after I shorted the isolated and common grounds at the Adapter Card. Now the mystery we need to solve is the difference in the pedestal value 1) between readout through SEQ and SASEQ 2) between Purple Card and full chain if both readout through SEQ (hybrid 1 and hybrids 2/3 at the plot below). I still see the errors at ~5% level.

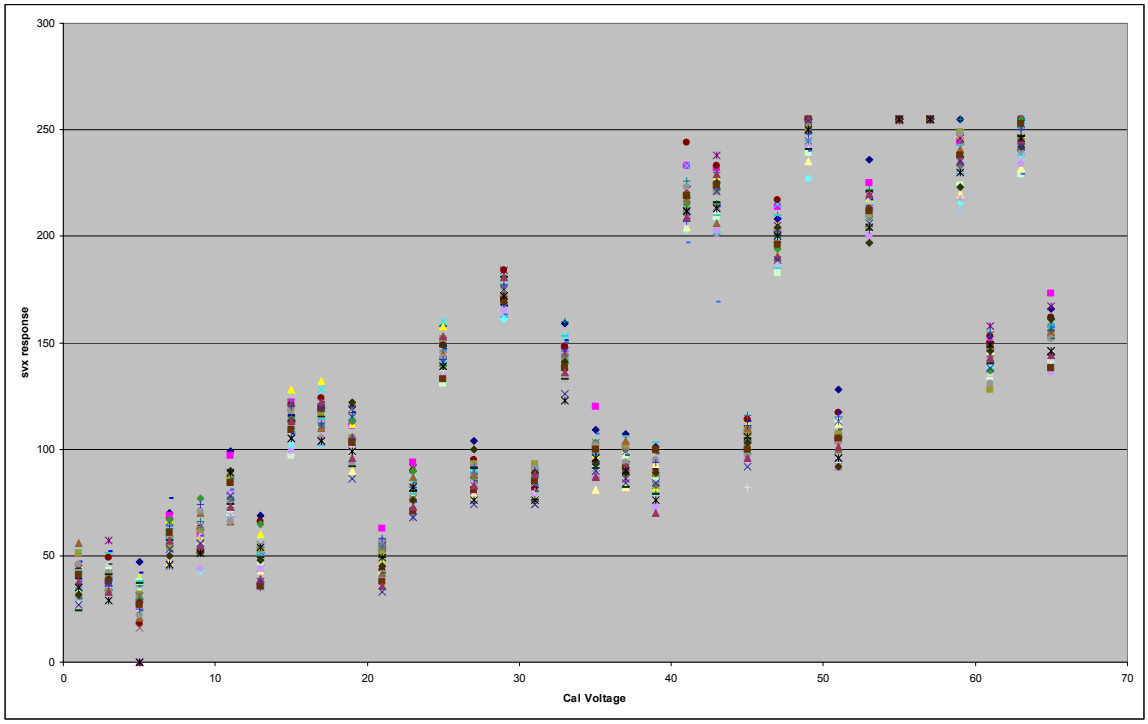


Linearity Tests D. Buccholz, D. Strom 4/20/05
Test Stand 6C

Hybrids



Modules

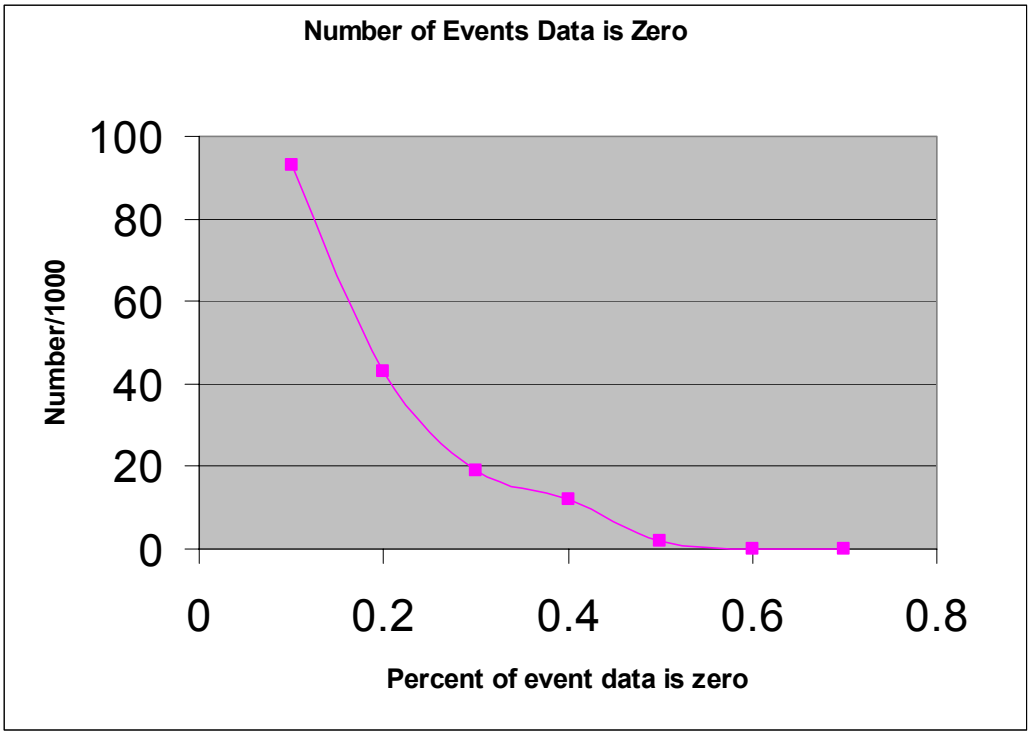


Data is zero study

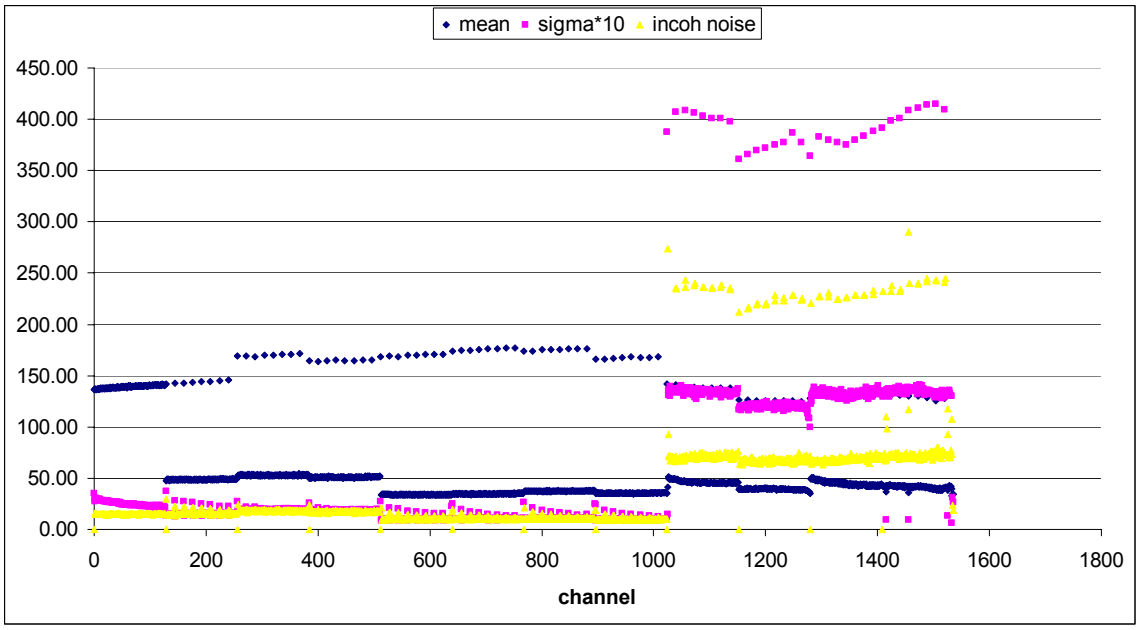
10 chips total
4 hybrid

4 modules
2 purple card

1000 events taken.



Statistics



firmware
sequencer- p:\electronics\run2b_firmware\control_040605\prtcrd.pof
sequencer controller- p:\electronics\run2b_firmware\nrzgenb_113004\nrzgen.pof

Errors

event #	HDI 0	HDI 1	HDI 2	HDI 3	HDI 4	HDI 5	HDI 6	HDI 7
94	208	208	208	208	208	20A	0	0
570	208	208	208	208	208	20A	0	0
742	208	208	20A	208	208	208	0	0

channel order	57
repeated events	0
data is zero	2
data is large value	0
incomplete readout	0
flying geese	0
wrong word length	3
event number	0
word count too large or 0	0
Lengths wrong	0

sparse channel ord. 0

event	raw index	channel check	lchan	chain	error count
19	1208	137	127	4	1
104	1468	209	127	5	1
106	688	161	127	2	1
137	1468	209	127	5	1
169	1468	209	127	5	1
172	1208	137	127	4	1
190	1468	209	127	5	1
219	688	161	127	2	1
225	688	161	127	2	1
253	948	177	127	3	1
254	1208	137	127	4	1
264	948	177	127	3	1
280	1208	137	127	4	1
283	1208	137	127	4	1
291	1468	209	127	5	1
310	688	161	127	2	1
325	1208	137	127	4	1
326	688	161	127	2	1
341	688	161	127	2	1
357	948	177	127	3	1
361	1468	209	127	5	1
366	1208	137	127	4	1
376	688	161	127	2	1
457	688	161	127	2	1
482	948	177	127	3	1
483	1468	209	127	5	1
512	1468	209	127	5	1
542	948	177	127	3	1
586	948	177	127	3	1
596	948	177	127	3	1
613	948	177	127	3	1
622	1468	209	127	5	1
624	688	161	127	2	1
633	688	161	127	2	1
635	1468	209	127	5	1
678	688	161	127	2	1
684	948	177	127	3	1

691	948	177	127	3	1
755	688	161	127	2	1
758	1468	209	127	5	1
765	948	177	127	3	1
789	1208	137	127	4	1
790	688	161	127	2	1
796	1468	209	127	5	1
801	688	161	127	2	1
810	1208	137	127	4	1
831	1208	137	127	4	1
892	948	177	127	3	1
897	688	161	127	2	1
923	1468	209	127	5	1
930	948	177	127	3	1
931	1208	137	127	4	1
939	1208	137	127	4	1
940	688	161	127	2	1
949	1208	137	127	4	1
965	1468	209	127	5	1
976	688	161	127	2	1