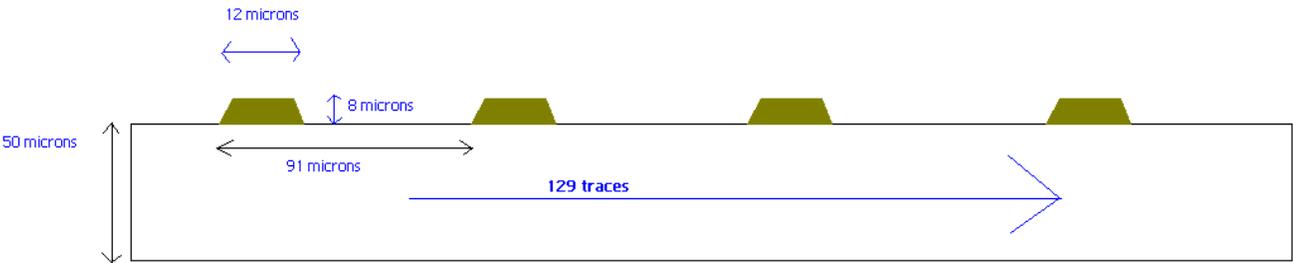
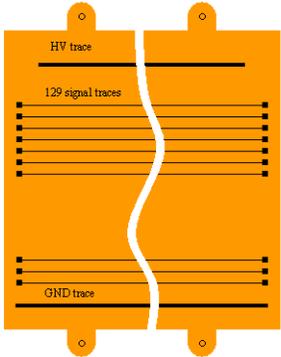
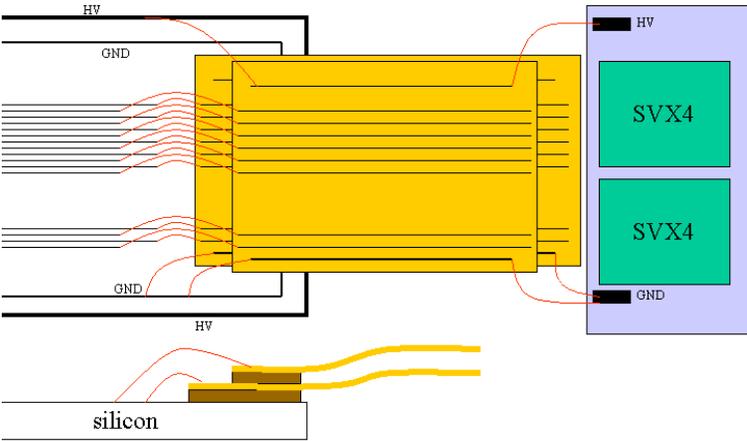


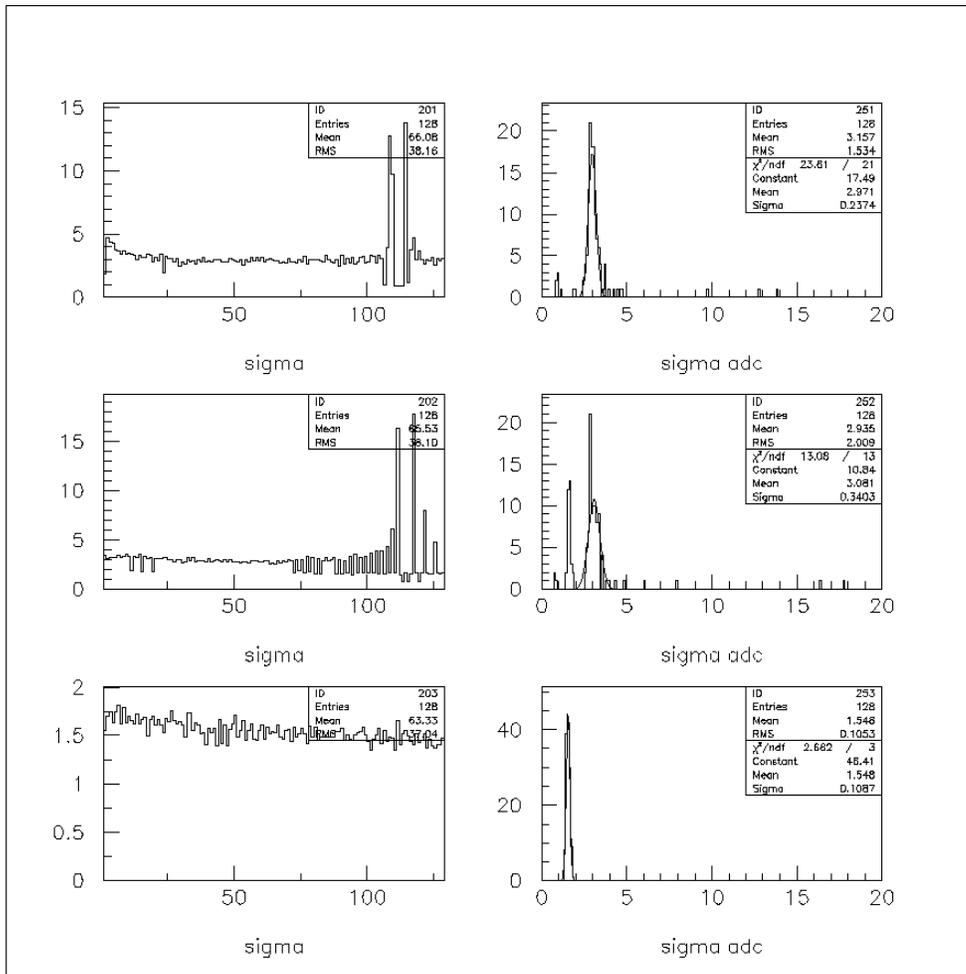
# Cursory Study of Various Properties of L0 Hybrid Prototype

## And Various Noise Dependencies Thereof



To ensure the validity of these measurements, I started by taking 10 noise readouts in a row without changing any conditions to determine how constant the noise was.

When taking measurements, the burn-in test generated plots like these:

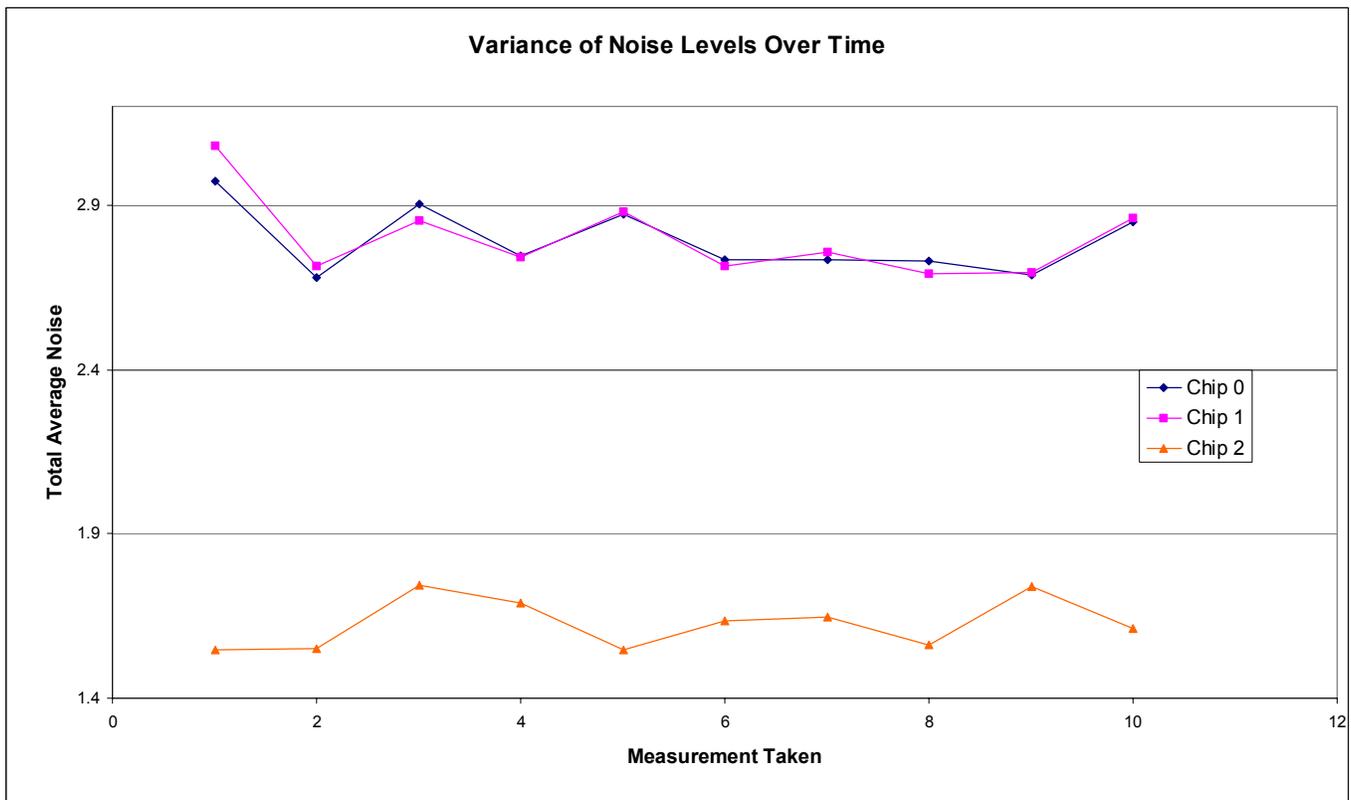


The 3 plots on the left show the noise readout per channel for each of the 3 chips. Topmost is chip 0, middle is chip 1, and the bottom plot represents chip 2 readout. Chip 2 is not bonded to the sensor, and thus provides a baseline for our measurements. Incidentally, during the course of this study, I failed to find any factor that noticeably affected Chip 2's readout.

The right 3 plots are histograms of the corresponding plots on the left.

As you can see by the plots on the left (for chips 0 and 1), while most of the channels are at a comparable level, quite a few channels appear to be bad. These appear as the secondary spikes and isolated blips in the histograms. To ensure that these bad strips do not skew the noise average that I record, I fit a gaussian to that small region of the histogram which obviously contains the valid data, and record the mean of that gaussian as the "noise average."

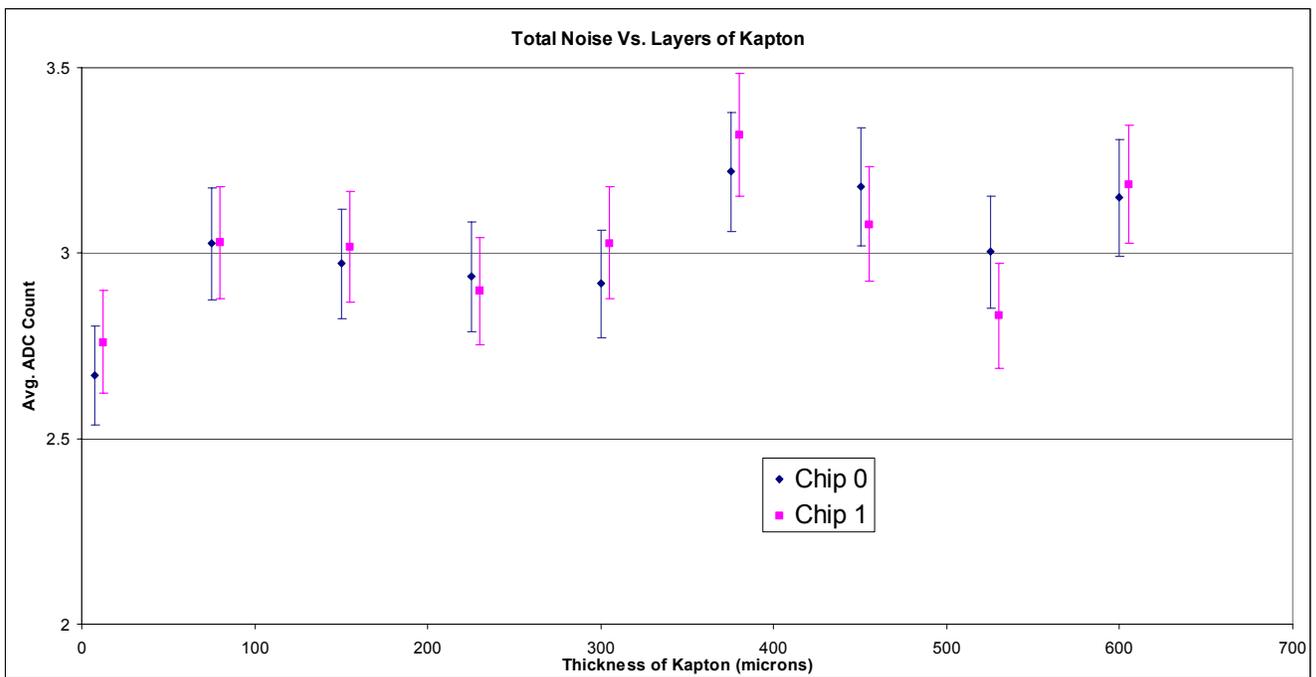
So I did this 10 times in a row without changing anything. Here's what I got:



From this one can see several interesting things. First, Chip 2, which is bonded out, clearly shows much lower noise than Chips 0 & 1.

Secondly, all 3 chips deviate from their average value by no more than 10%. So on all future measurements (in which I do change various factors), I can trust my data to accuracy within about 5-10%. And the final inference that one can take from this graph is the clear interdependence of Chips 0 and 1. In other words, they fluctuate together. So obviously, the noise variation is not purely random – there is a systematic component to this behavior that needs further analysis.

Next, Andrei wanted me to study the noise dependence on the distance between the two cables. I did this first by placing 75 micron thick kapton strips between the cables, and then placing a few hundred grams of weight on top of the cables to ensure they were pressed together as firmly as the layers of kapton would allow. Unfortunately, 75 microns was much too thick, and the capacitance between the cables quickly became negligible.

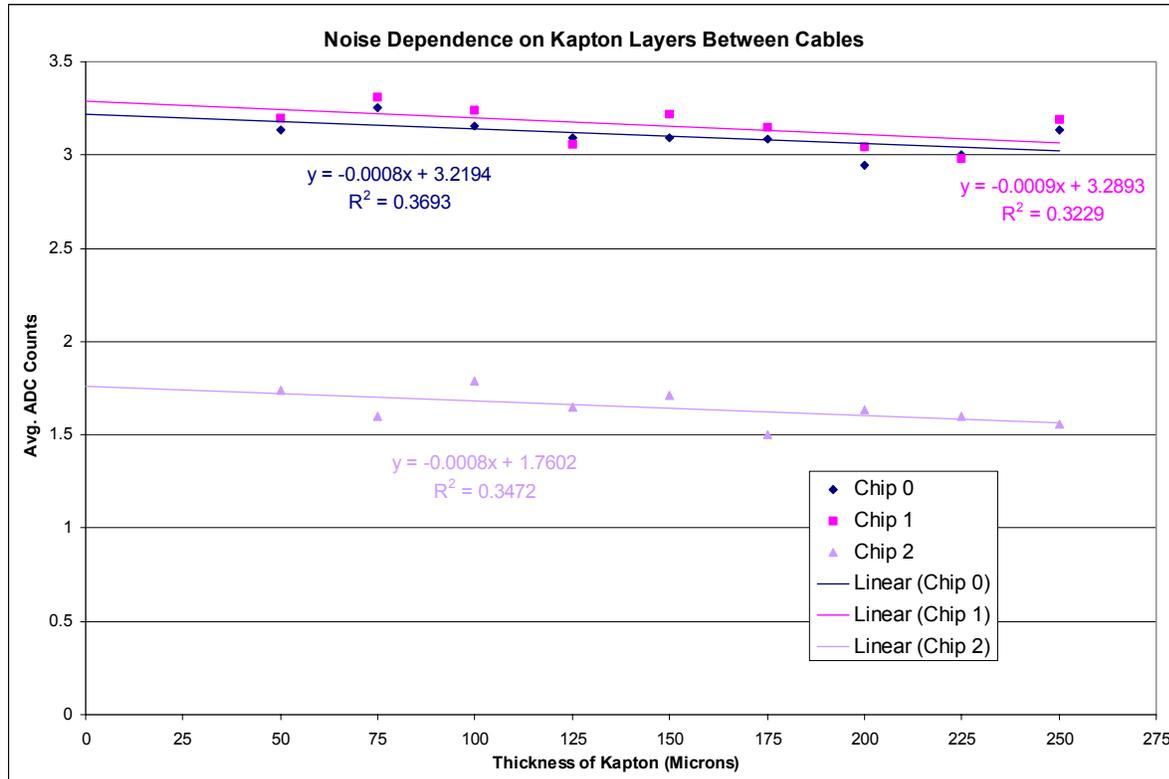


\*Error Bars of 5% are shown

Theoretically, we would expect the average noise level to decrease as the distance between the cables increased, as the capacitance and therefore the “cross-talk” between the cables decreased in proportion. Clearly, a decrease is not immediately evident from this graph, leading one to the conclusion that the kapton layers were too thick to show the effects of decreasing capacitance, and the fluctuations which we see are merely statistical.

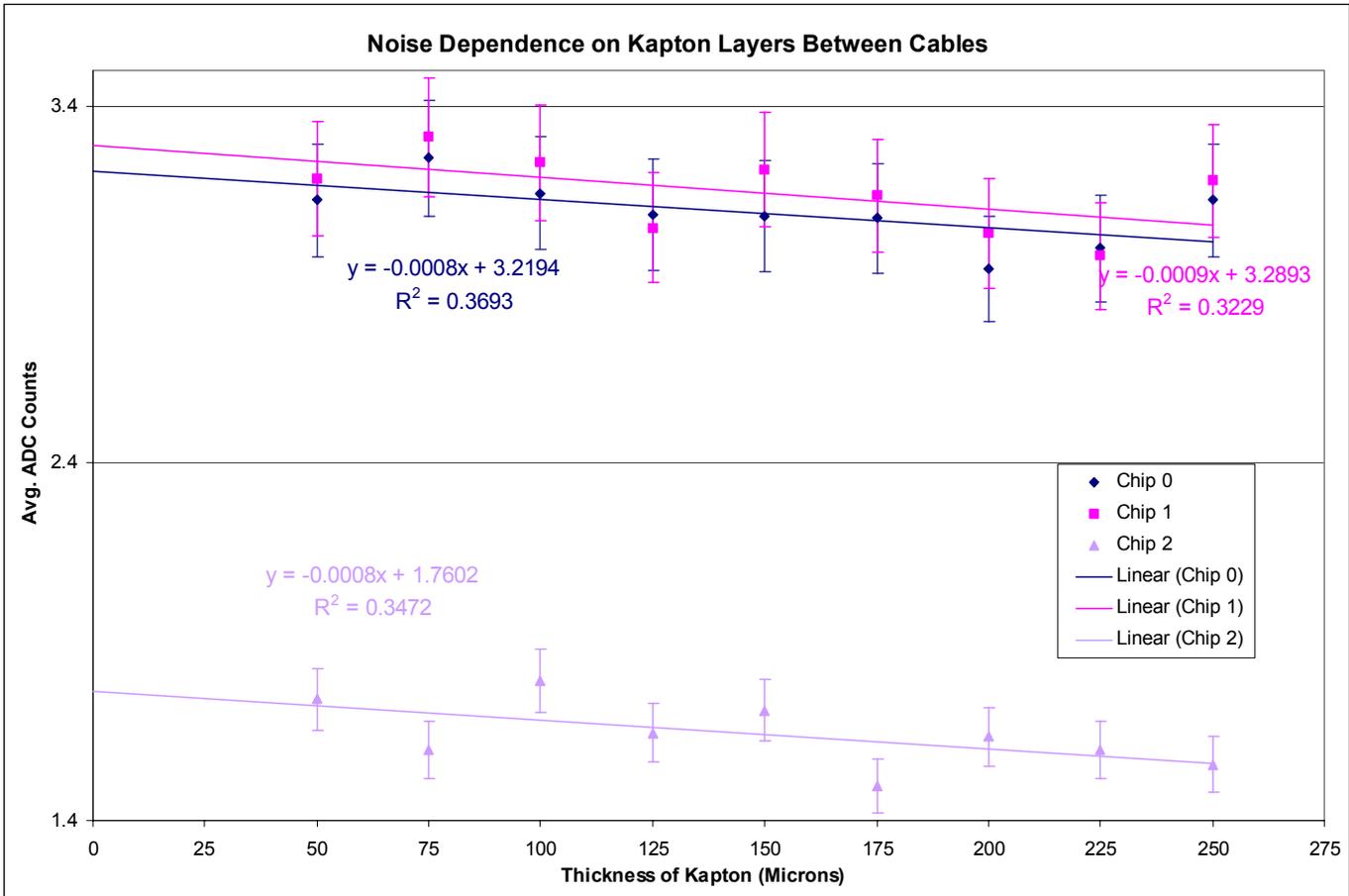
Ok... so we find thinner kapton...

I redid the same study with one mil kapton to “zoom in” on the region of interest:

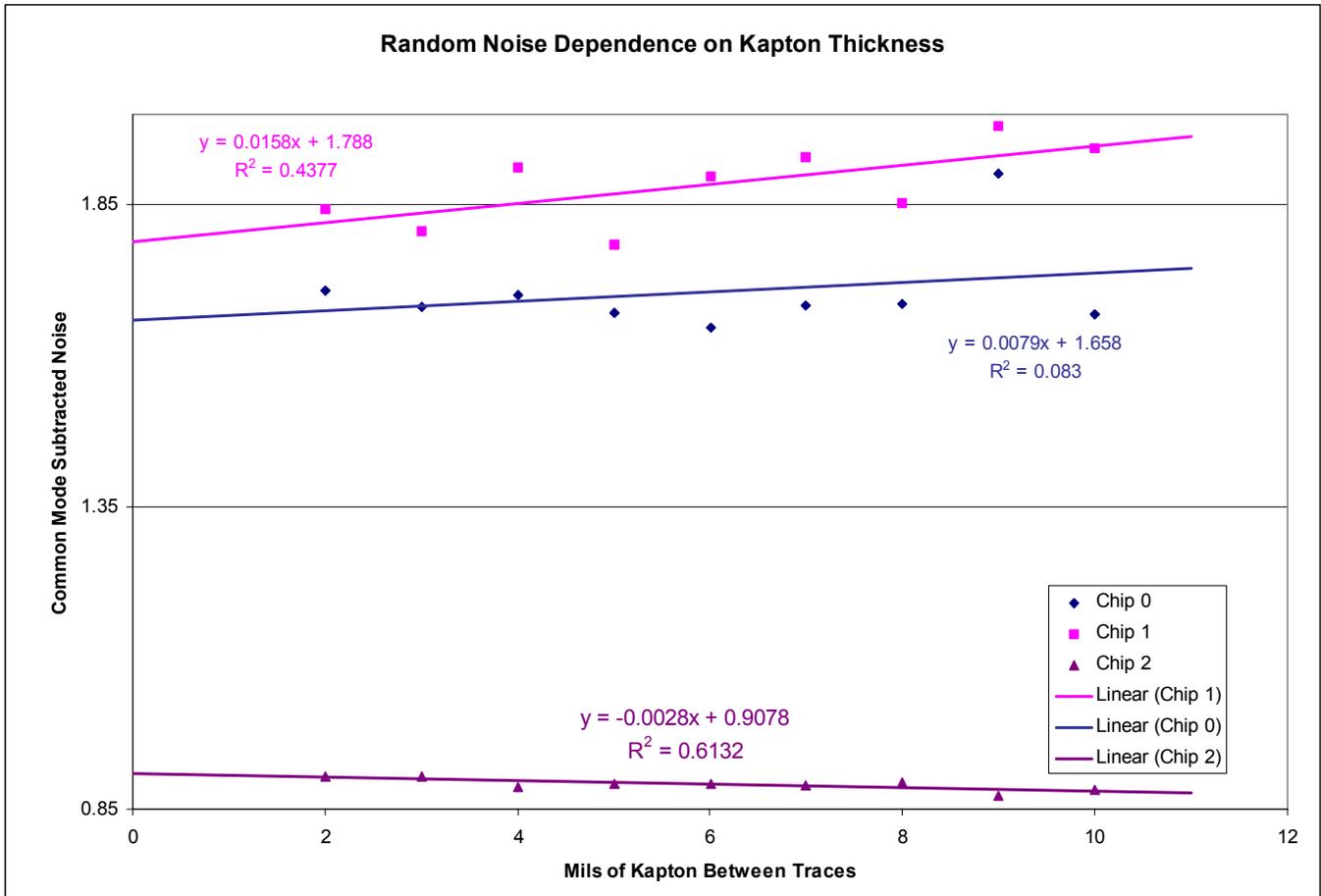


This time chip 2 is also shown for comparison. From the best-fit lines, it is apparent that Chips 0 and 1 show no more dependence on the thickness than Chip 2, which should show no dependence at all. The slopes and  $R^2$  values for all 3 chips are very similar (slopes =  $-.0008$ ,  $-.0009$ ,  $-.0008$  &  $R^2$ s =  $.369$ ,  $.323$ ,  $.347$ ) – the fact that all three display a negative slope of similar magnitude (when one should theoretically have a slope of 0) suggests that the slight dependence seen is more a factor of the chip and/or the measuring the process, rather than any capacitance effect between cables.

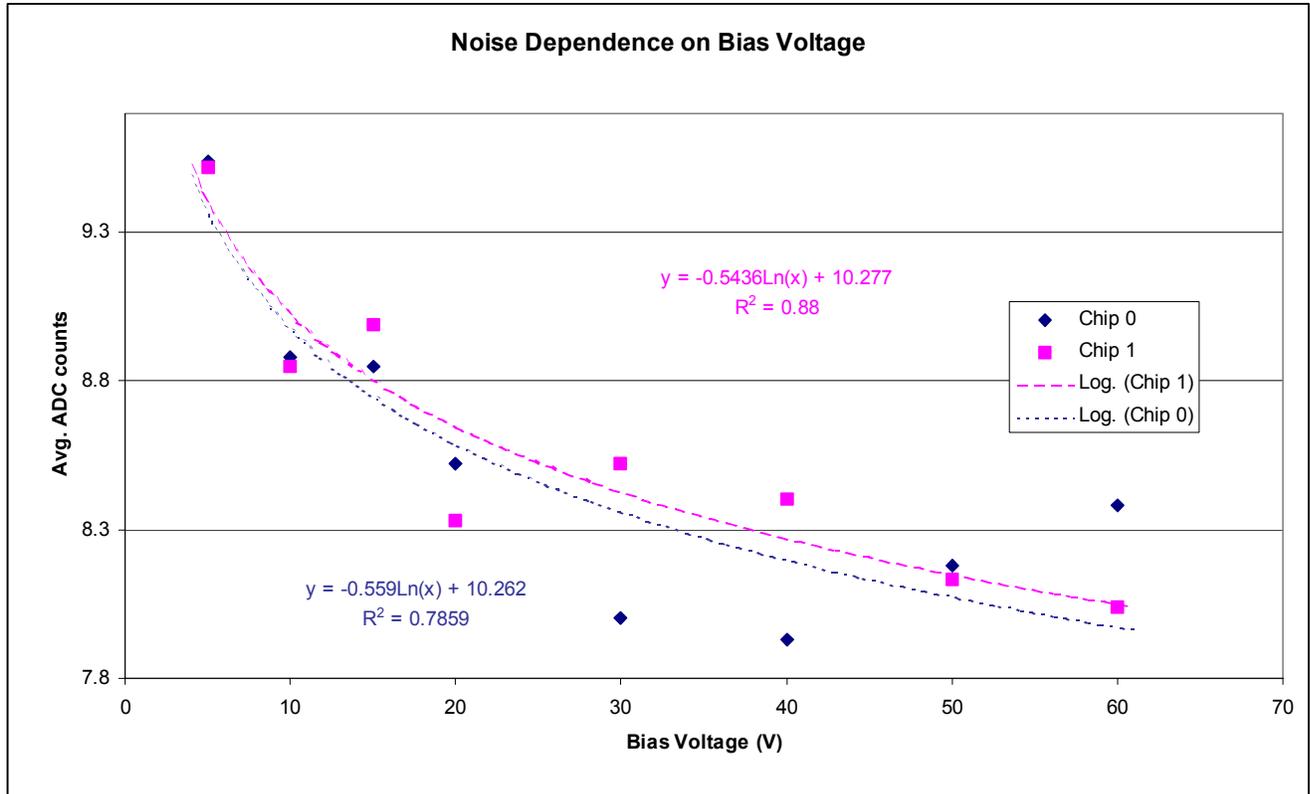
**When 5% error bars are added, the linear relationship is shown to be even more tenuous.**



**When one considers not total noise but random noise (common-mode subtracted), the situation becomes even less understandable: Here the linear fits are terrible, but tend to show a general upward trend in the bonded chips, and slight downward trend in Chip 2. I don't know if this represents anything significant, but I would suspect not.**

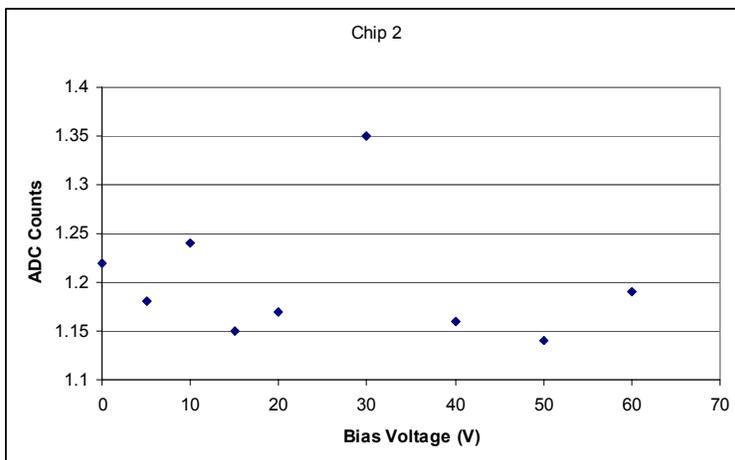


**Kazu has already done a bias voltage dependence study, but here's mine anyway:**

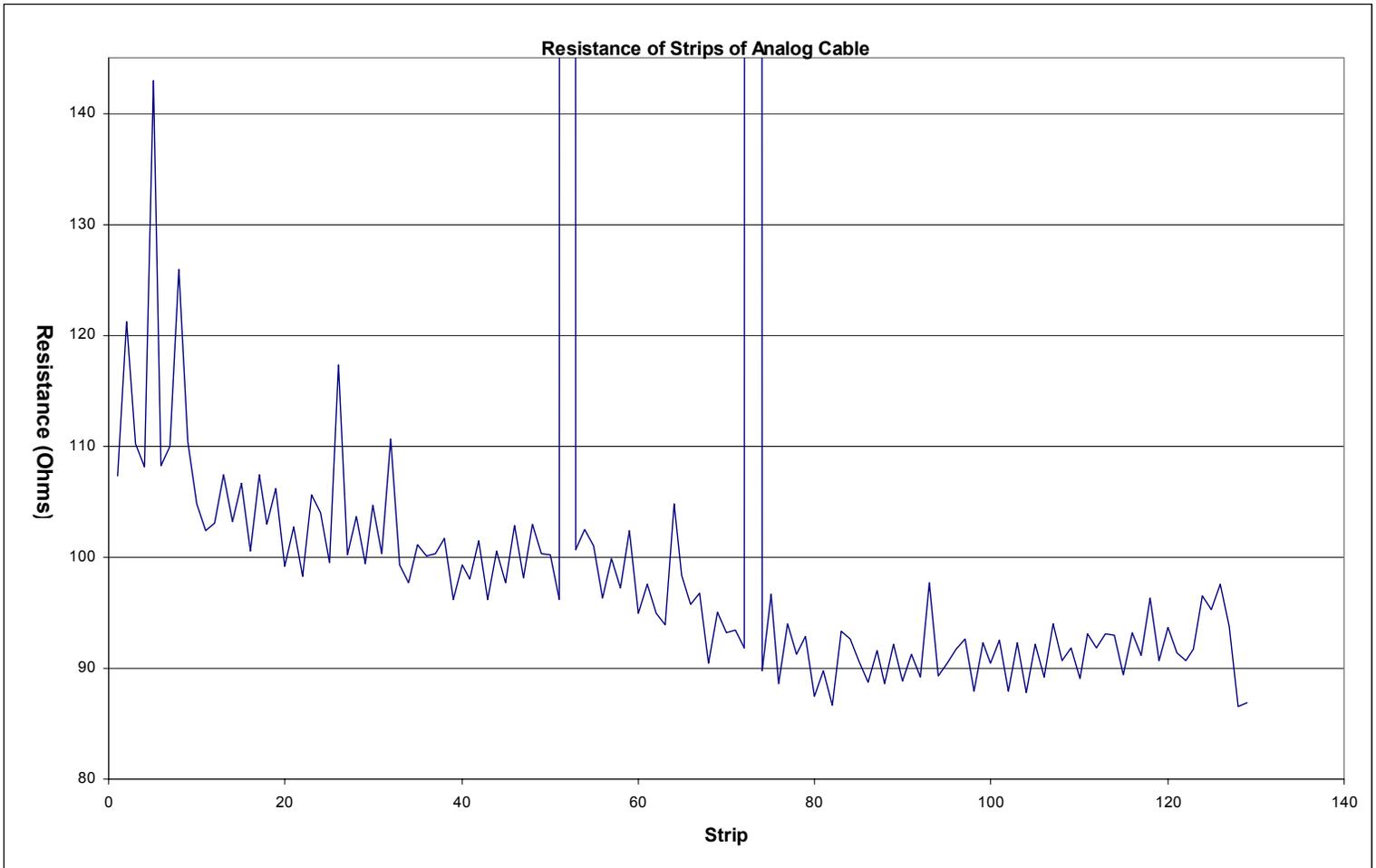


**These noise levels are much higher than for the previous graphs because these measurements were taken before I wrapped the setup box in an aluminum foil shield and grounded it. Doing this decreased the total noise in the bonded chips by a factor of about three. Despite this, the fundamental relationship between bias voltage and noise should be unchanged.**

**Similar Data for Chip 2 shows no obvious dependence on bias voltage.**

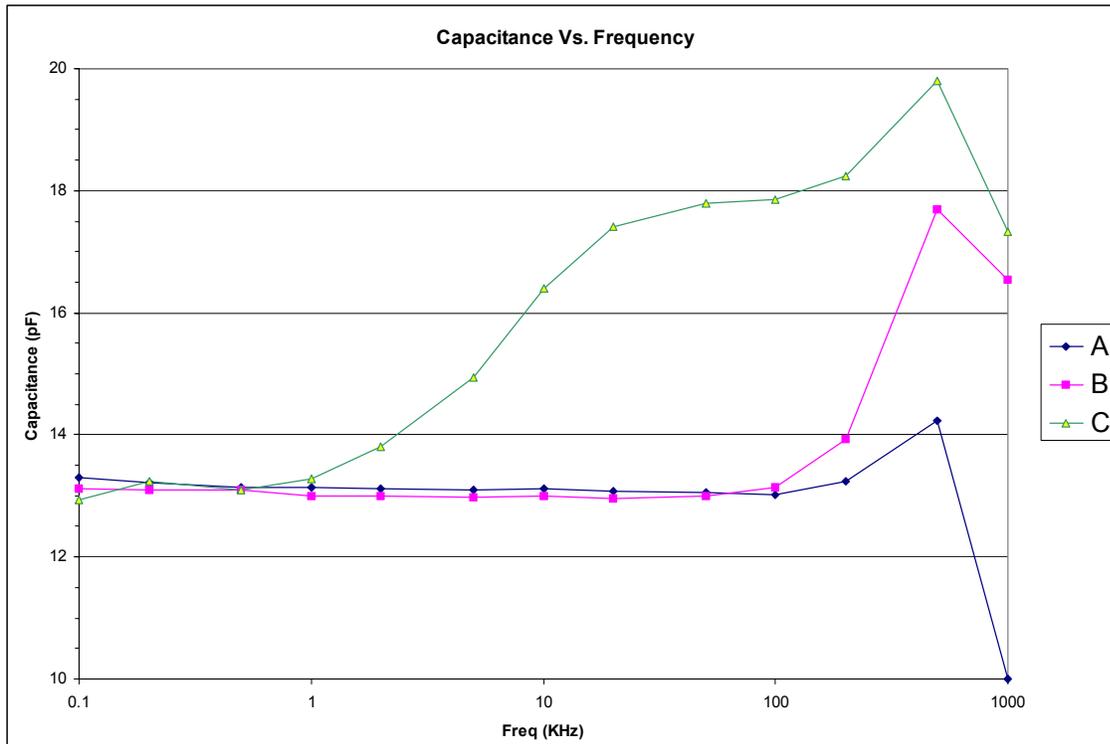


**Finally, I'd like to present some data on the Dyconex Analog Cables which Frank Lehner and I have analyzed in the last few days. He and I measured the resistance along each strip to find open traces.**



**From this, we found strips 52 & 73 to be bad. Every other strip looks good, although there does seem to be some sort of positional relationship to the resistance.**

Next we measured the capacitance of 3 strips to both of its direct neighbors.



A, B, C merely represent our designations for each strip that we tested. All three strips were near the middle of the cable. Strip C's behavior could be an anomaly of our measurements, or there could be something odd about that strip; we really haven't had enough time with the equipment to be sure.

Frank redid some measurements Friday morning more carefully, and found things to be a little better behaved. A fair assumption is that the capacitance is fairly constant up to ~200 KHz. From this data, we can see that at low frequencies, the one trace experiences a capacitive coupling to its two neighbors of about .3 pF/cm. I believe the calculations suggested a value of about .35 pF/cm.

