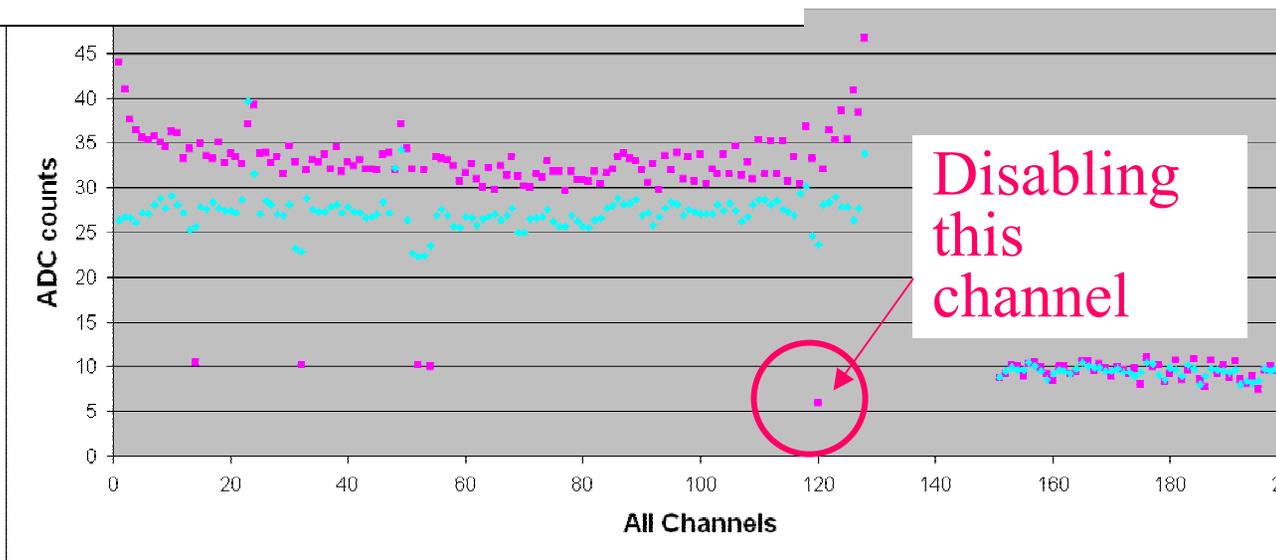
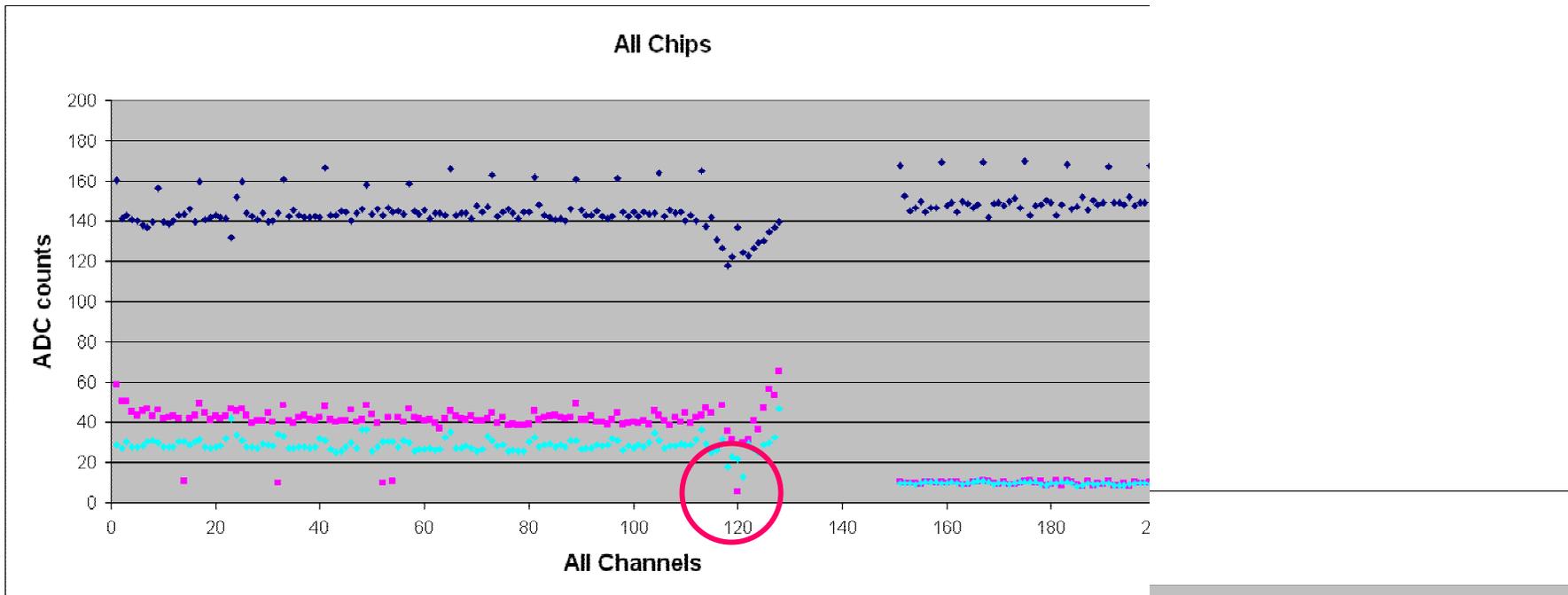


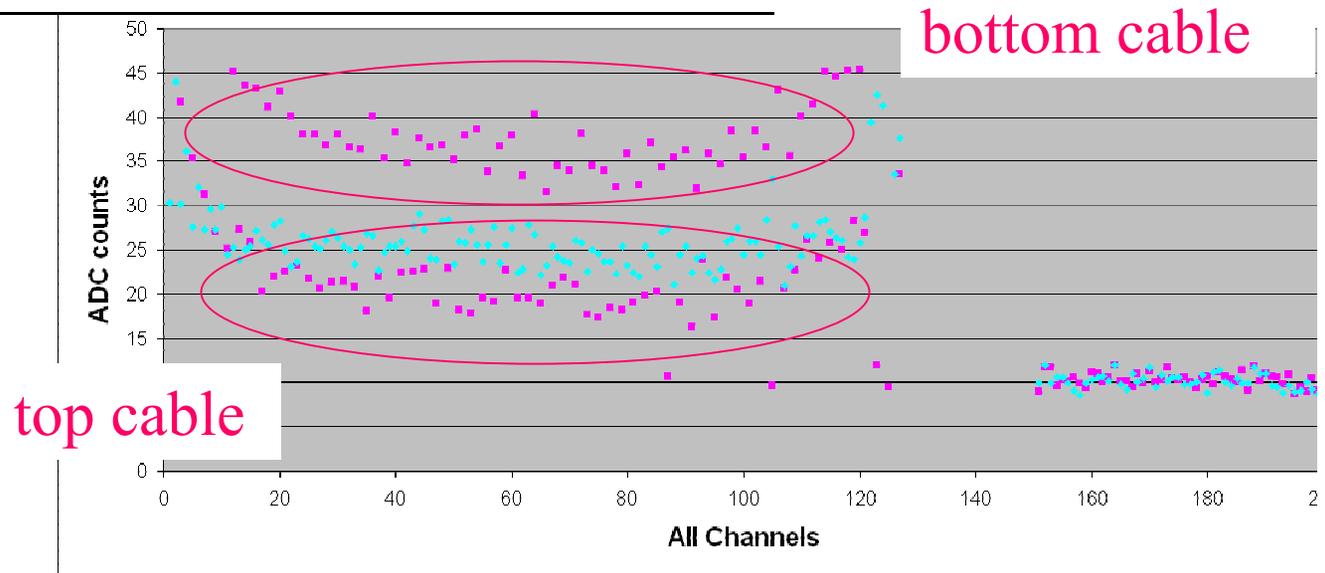
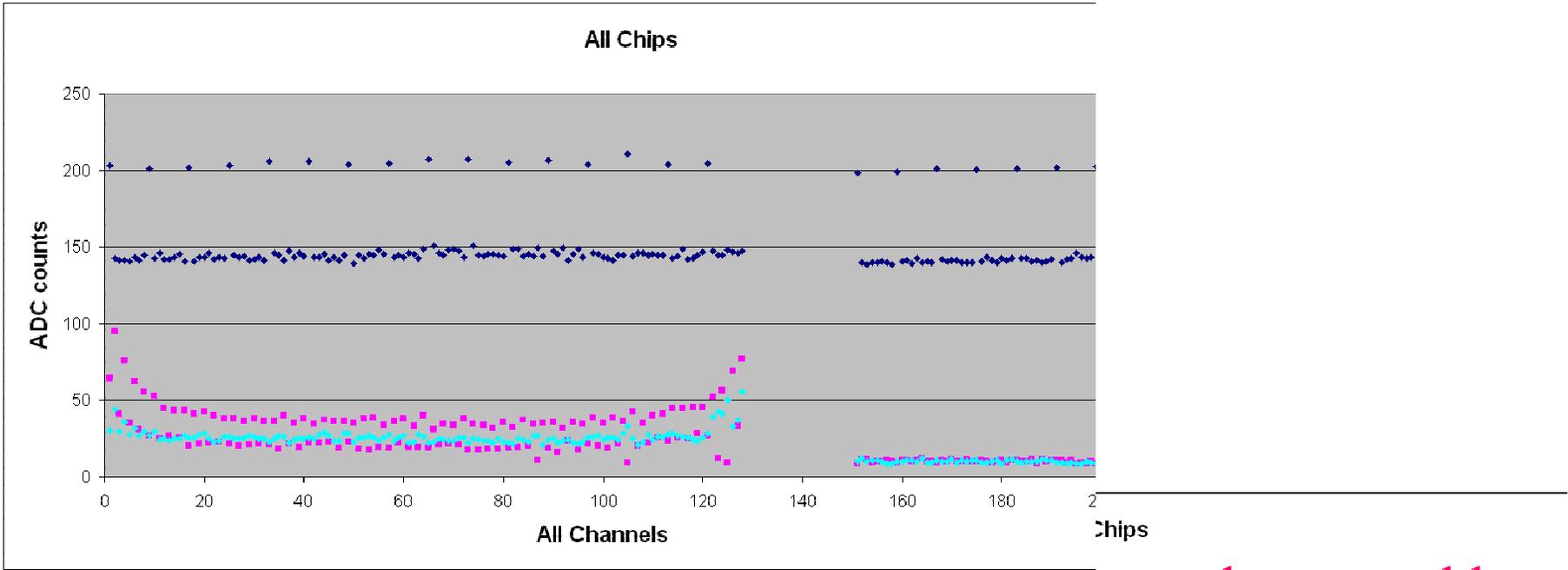
## L0 prototype modules

- L0#3 --- both sensor and cable are bonded. AVDD and DVDD tied together.
- L0#4 --- only cable is bonded.
- L0#5 --- ch1-64: only cable bonded. ch65-128 both sensor and cable bonded. Kapton backing for grounding is done.
- Firmware ready for testing (thanks to Mike).
  - bug fix for the preamp reset.
  - capability to choose one pipeline cell (cal\_sr in init).
  - ensure all pipeline cell reset by extra 46 clocks.

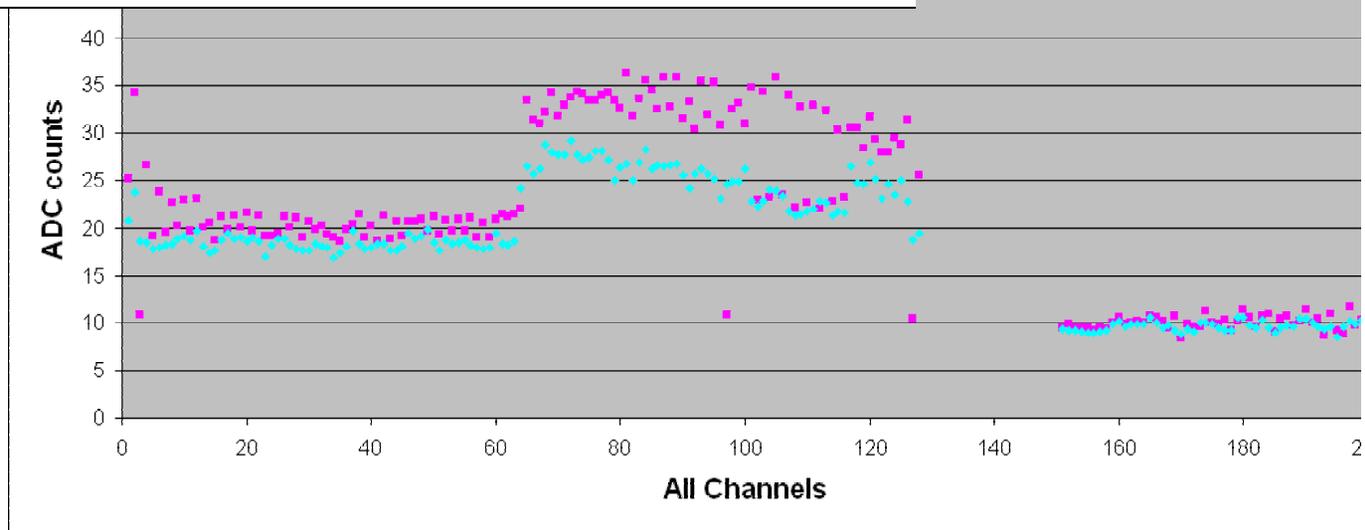
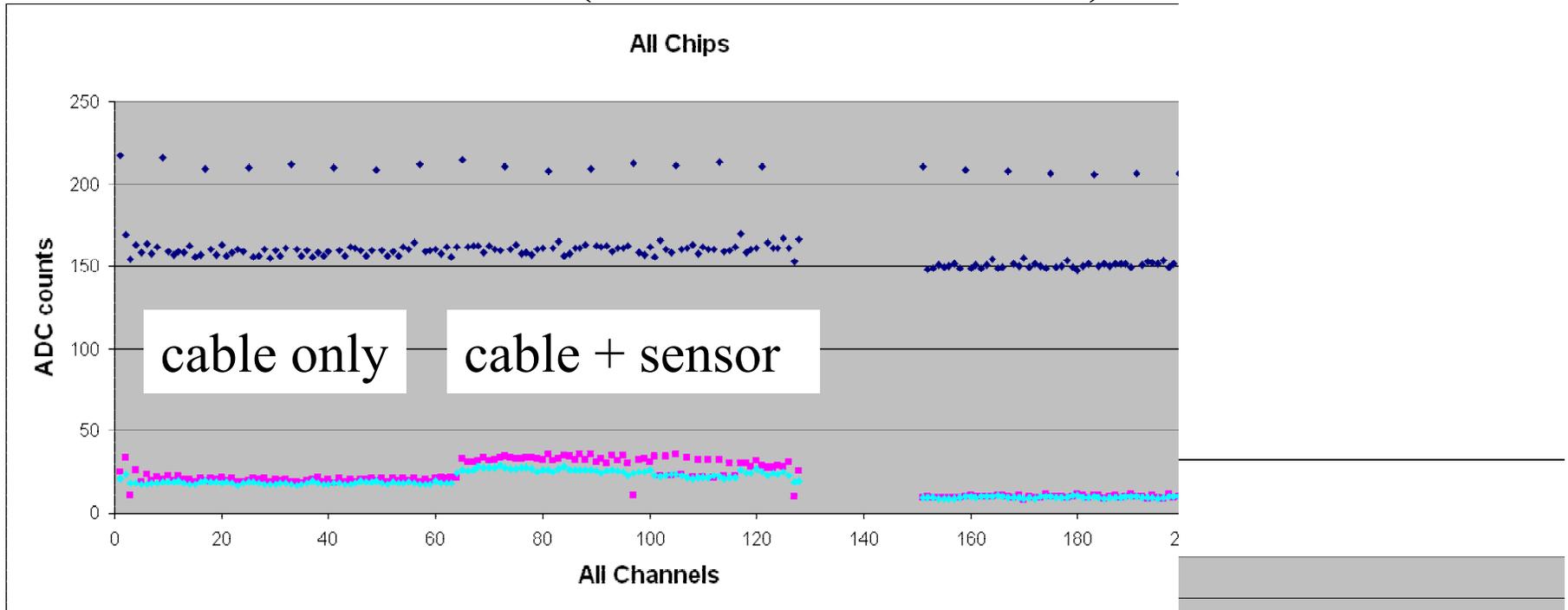
# L0#3 (cable and sensor)



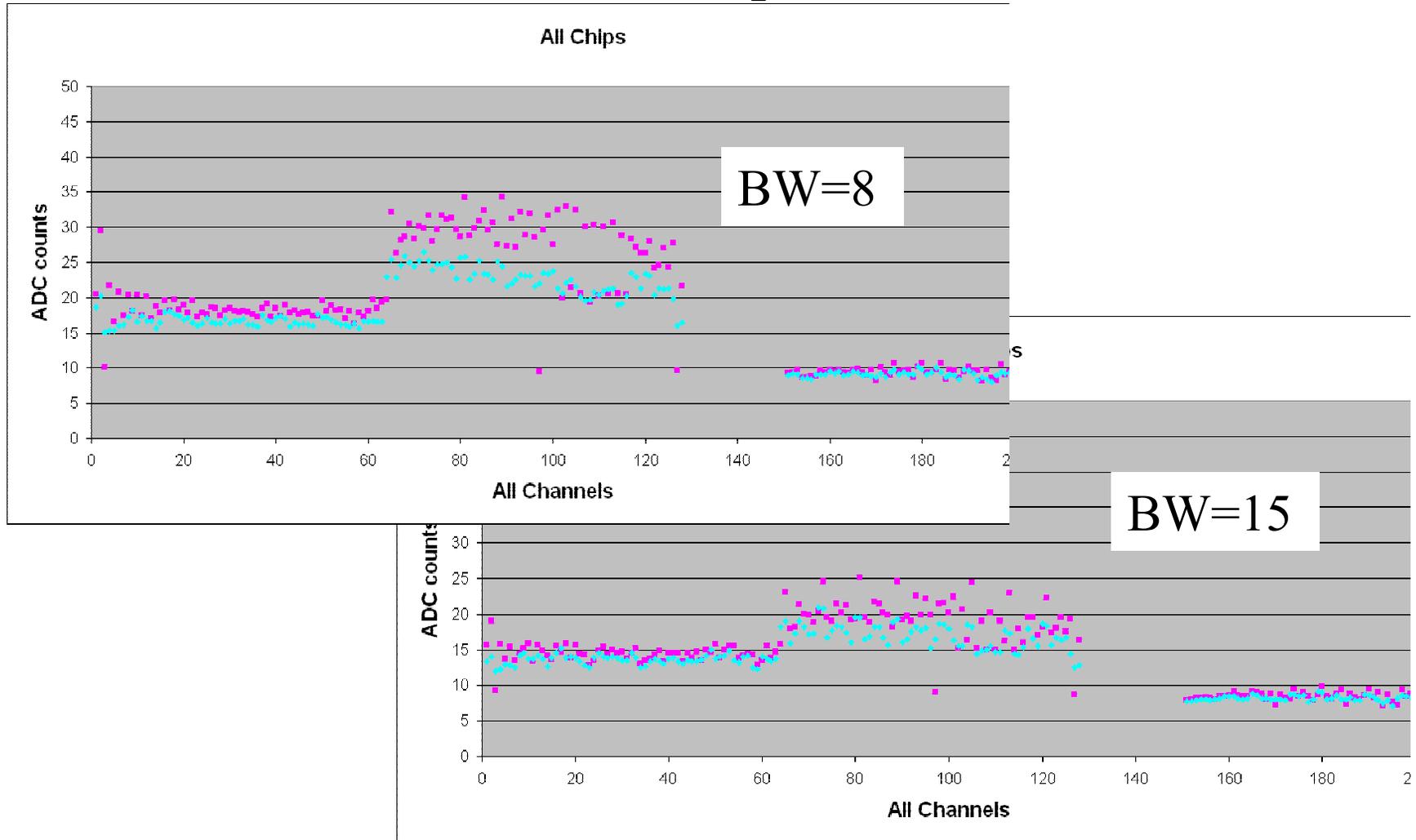
# L0#4 (only cable)



# L0#5 (cable and/or sensor)



# Band Width dependence



All three modules reasonable response!

# Status Summary

- BW=4, ramp slope=1 for this summary.
- L0#3 and L0#5(sensor part) have similar noise level.  
~2.2 ADC counts (1500e) of noise increase relative to the bare chip. Random noise by ~1.6 ADC (1100e).
- L0#5 (only cable part): ~1.0 ADC counts (700e) of noise increase relative to the bare chip. Random noise by ~0.9 ADC (600e).

cf.  $ENC = 300 + 41C @40pF$

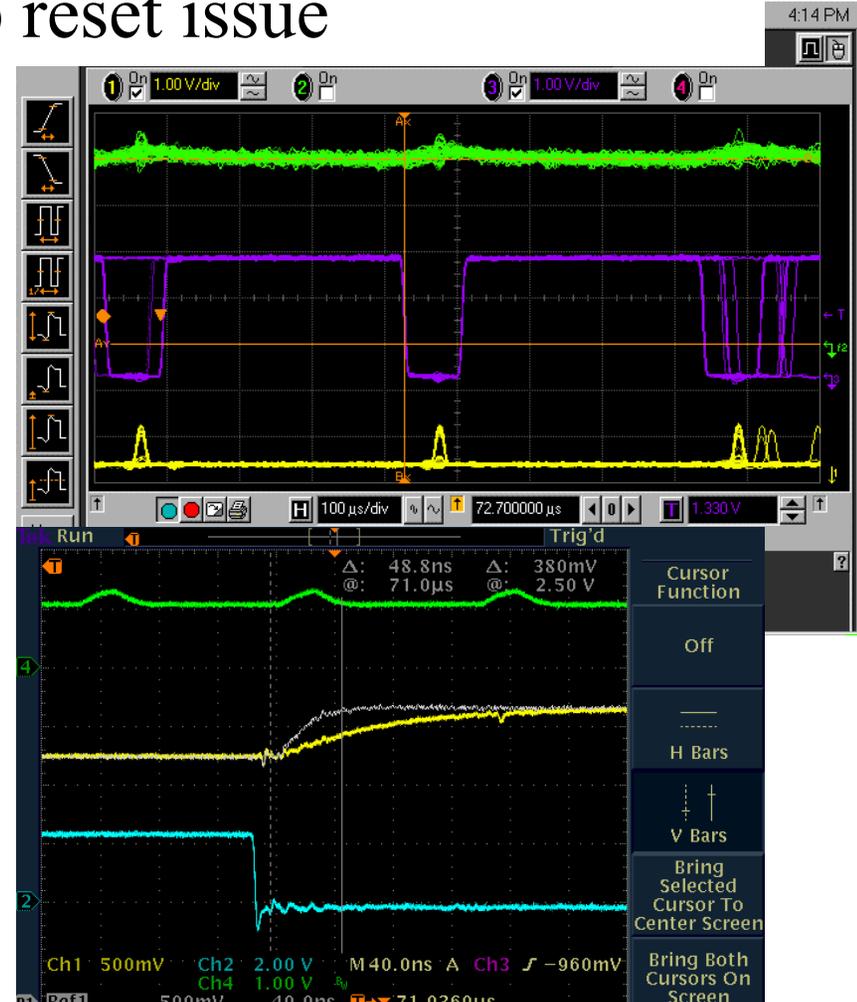
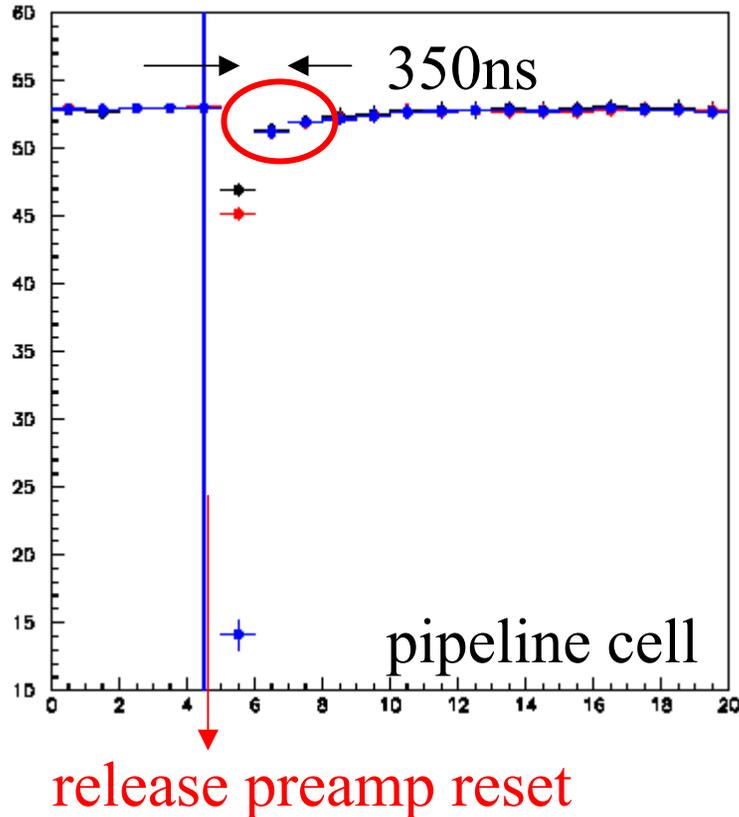
1100e  $\rightarrow$  27pF(cable+sensor), 600e  $\rightarrow$  15pF(cable)

- L0#4 has higher noise for the bottom cable.
- All has reasonable bandwidth dependence.
- Common mode noise when sensor bonded (?).

# Plan

- L0#5 put on the L0 structure.
- Test and compare the result with the current status.
  
- Kapton (grounding mesh) backing for L0#3.
- Test before putting it onto the L0 structure.
- L0#3 put on the L0 structure.
  
- Simultaneous read out of L0#5 and L0#3 on the structure.

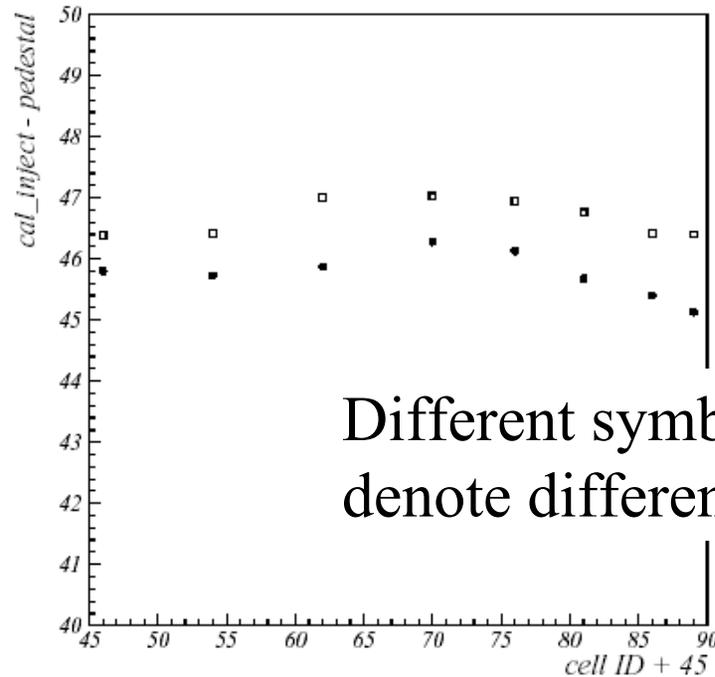
# SVX4 preamp reset issue



- This is quite small effect at the front end. ← acceptable. cf. 4.4mV/fC at preamp, voltage gain of 3.4 at pipeline.
- Should gone by the real time pedestal subtraction.

## Pipeline cell dependence of gain

- Sara sees pipeline cell dependence of gain (2 or 3%) in her hybrid/module testing.
- The same effect has been observed in single chip (1 or 2% variation).



- Wafer dependence???