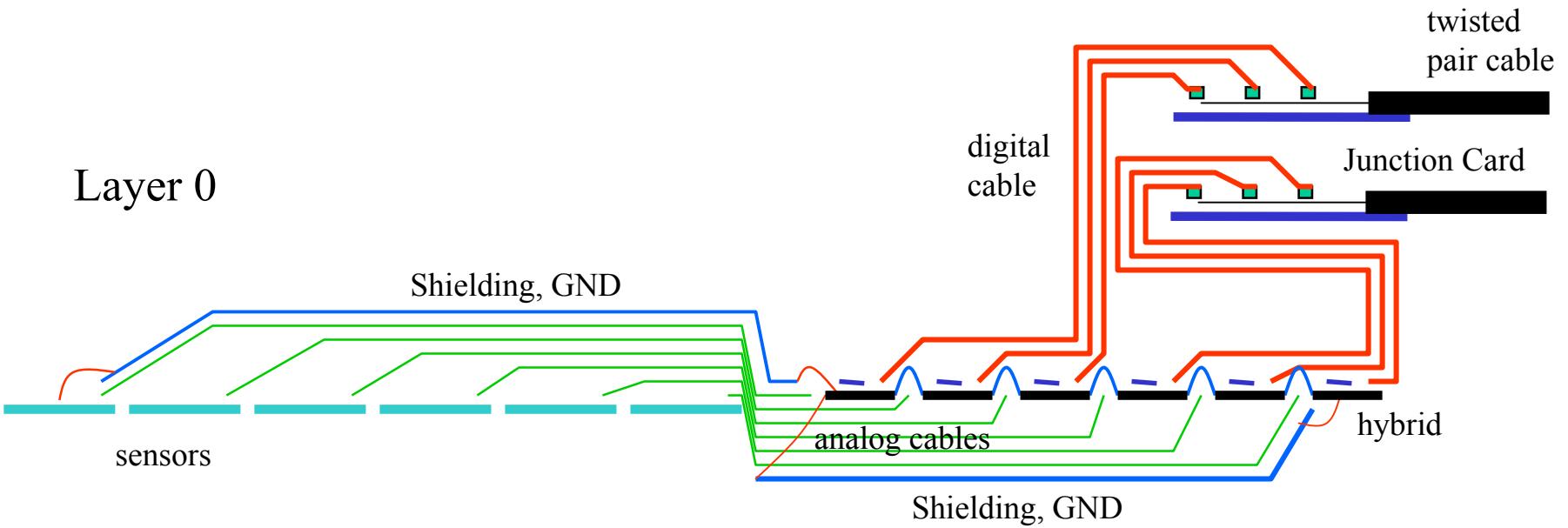


Analog cable

Andrei Nomerotski 1/15/02

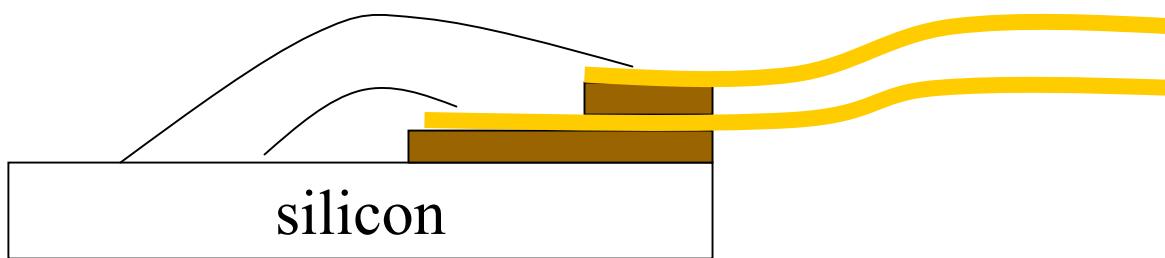
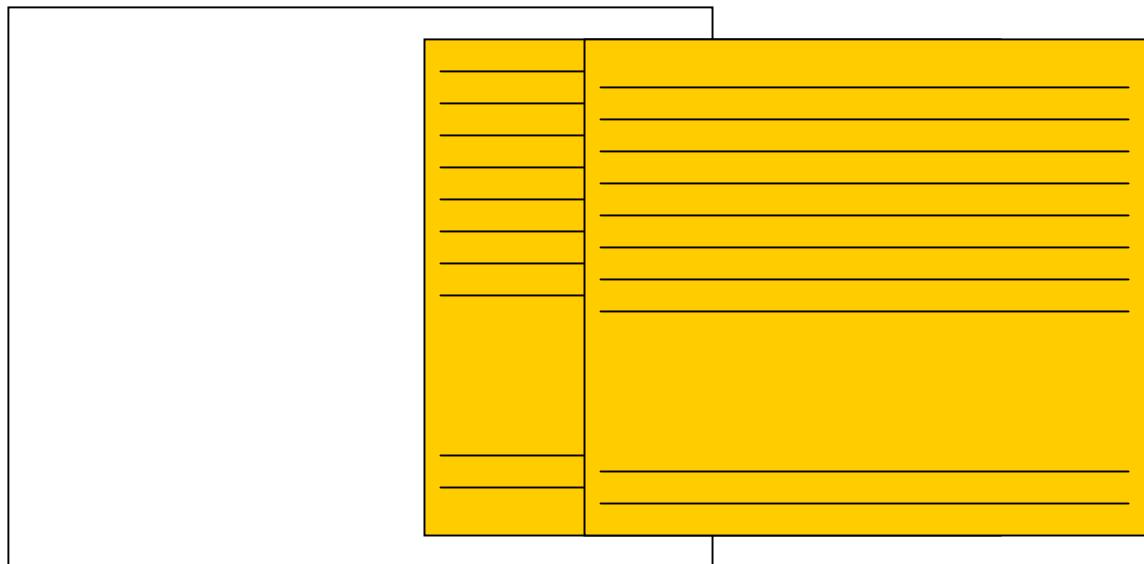
- L0 readout
- Shielding considerations
- Capacitance considerations
- HV connections
- Cable design

Layer 0 readout

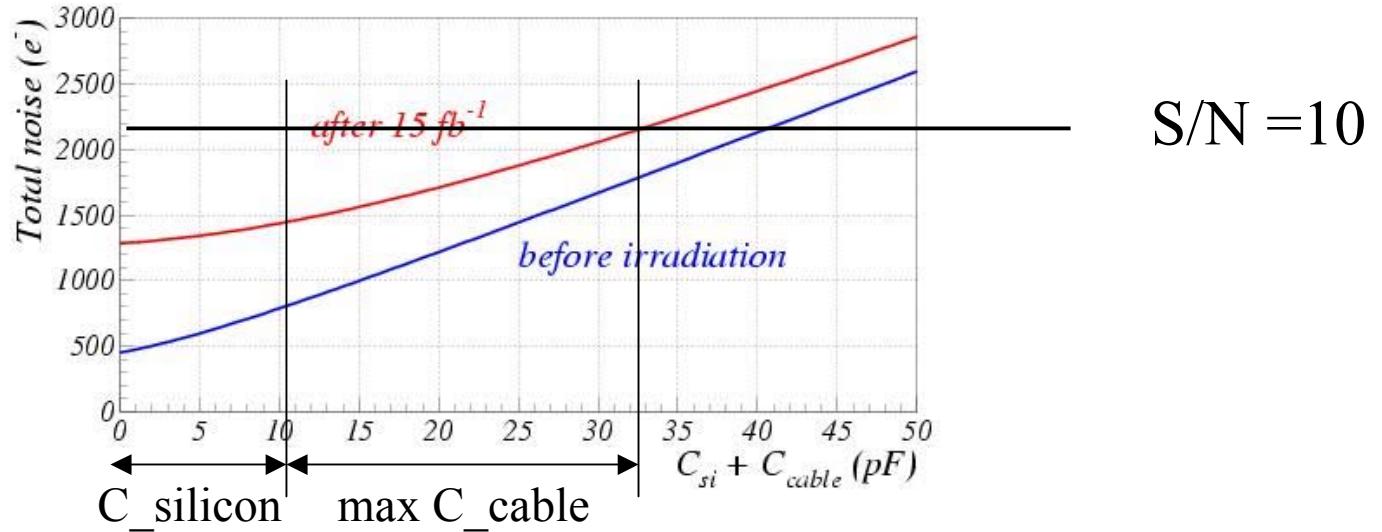


- 6 pairs of analog cables
- 2 chip hybrids
- Common shielding

New design of analog cable



Layer 0 noise



Acceptable cable capacitance is determined by noise performance

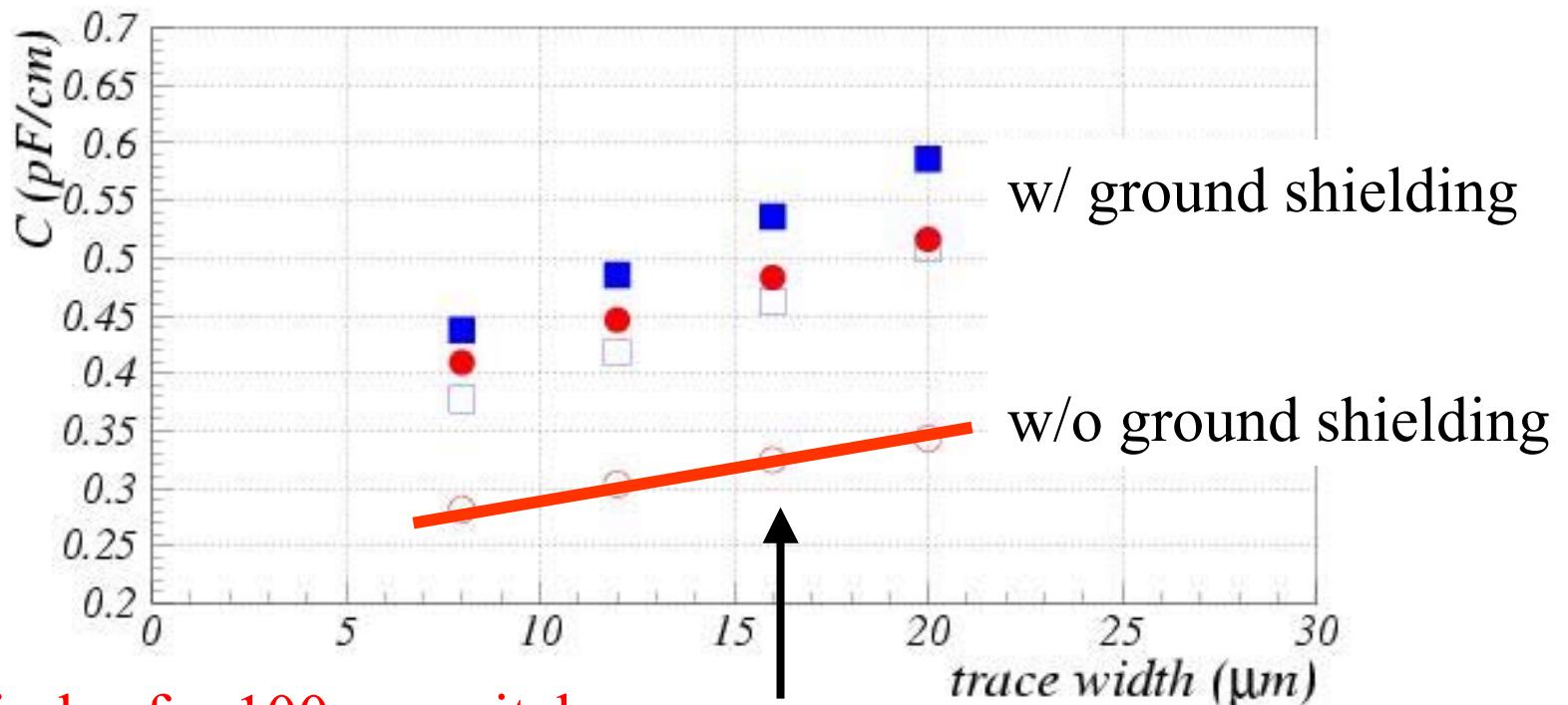
$S/N = 10$ after $15 \text{ fb}^{-1} \Rightarrow$ total noise = 2200

\Rightarrow total capacitance $< 33 \text{ pF} \Rightarrow C_{cable} < 23 \text{ pF}$

$\Rightarrow C_{cable} < 0.55 \text{ pF/cm}$ for 42 cm long cable

Capacitance

- Calculations agree with measurements within 10%
- 50 μm thick substrate with $\epsilon_r = 3.5$
- Settled on $\sim 100 \mu\text{m}$ pitch and 16 μm trace width



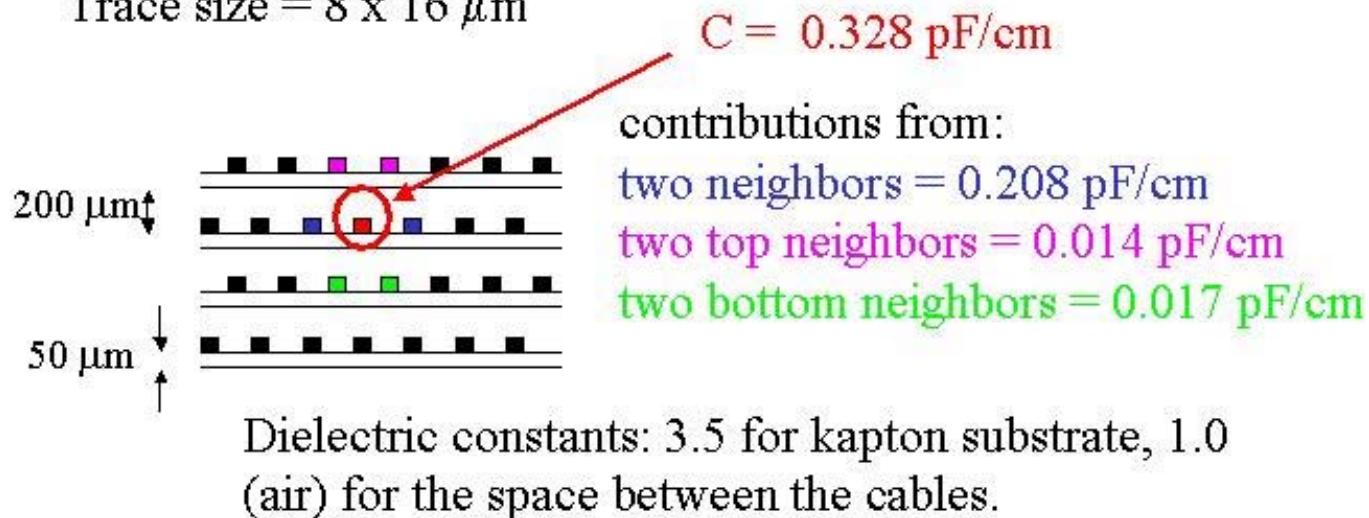
Red circles for 100 mm pitch
Blue squares for 50 mm pitch

16 $\mu\text{m} \Rightarrow 0.32 \text{ pF/cm}$

Capacitance

Trace pitch = 100 μm

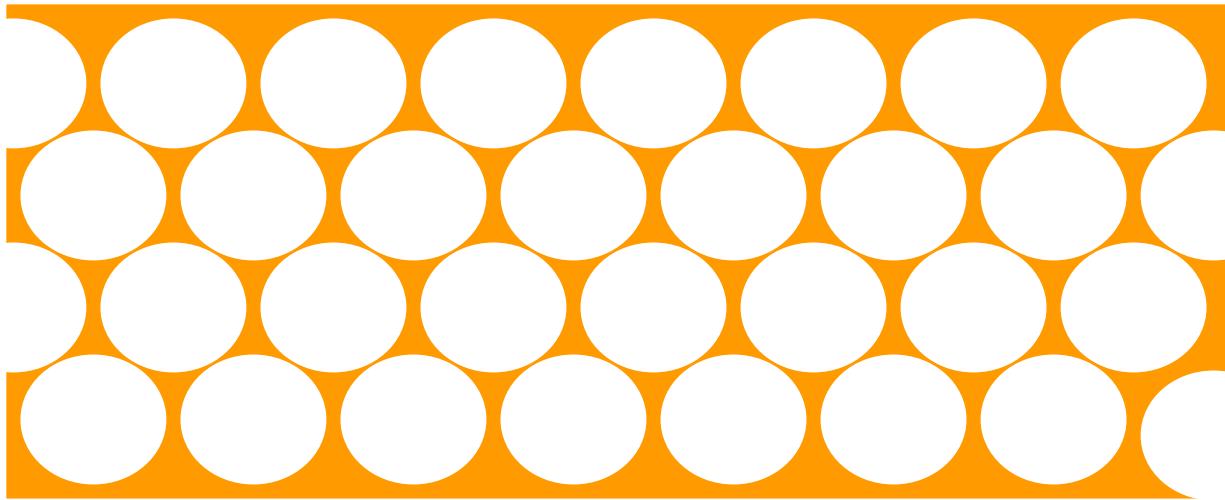
Trace size = 8 x 16 μm



ϵ_r (spacer)	C(pF/cm)
1	0.328
2	0.449
3	0.566

kapton's ϵ_r
fixed to 3.5

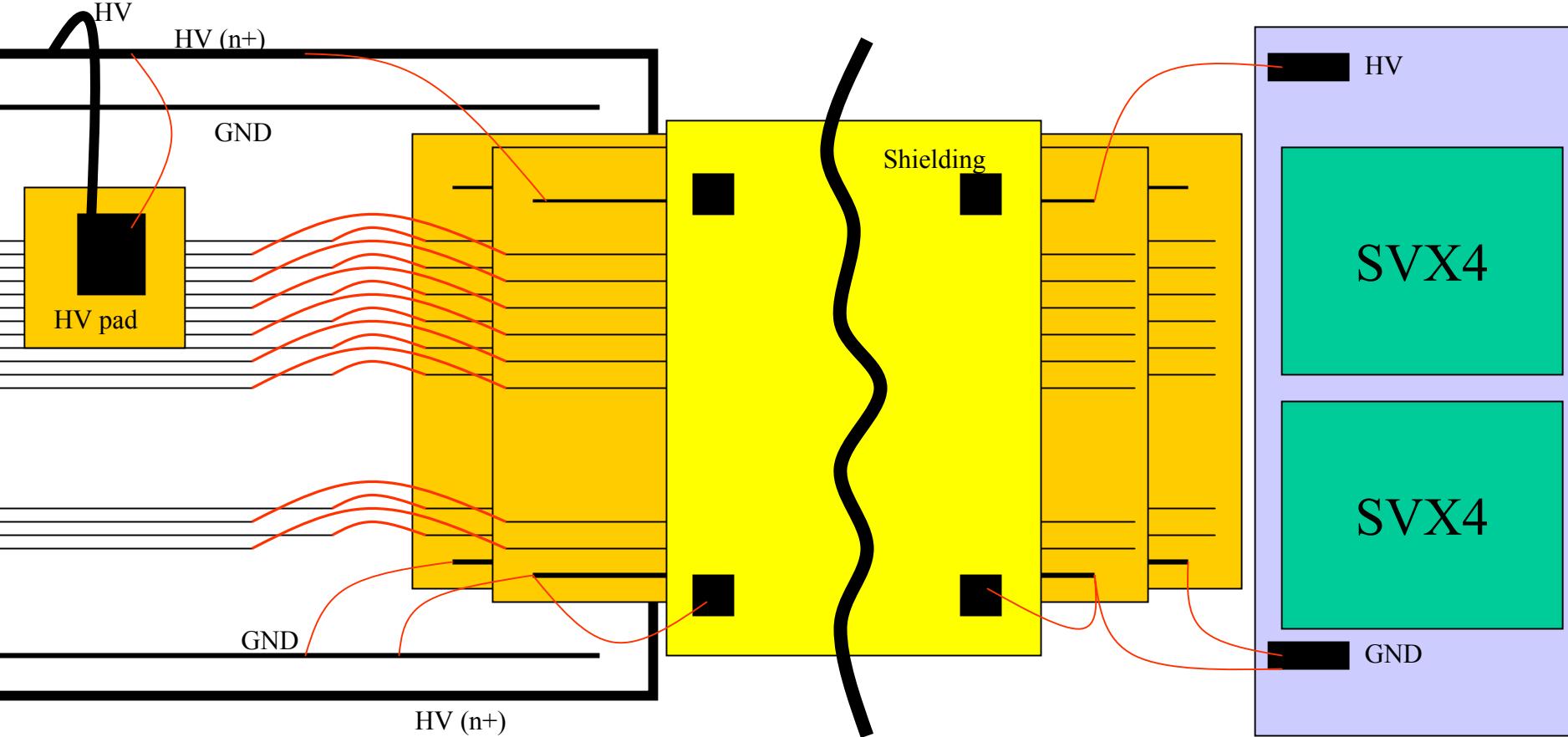
Spacer between cables



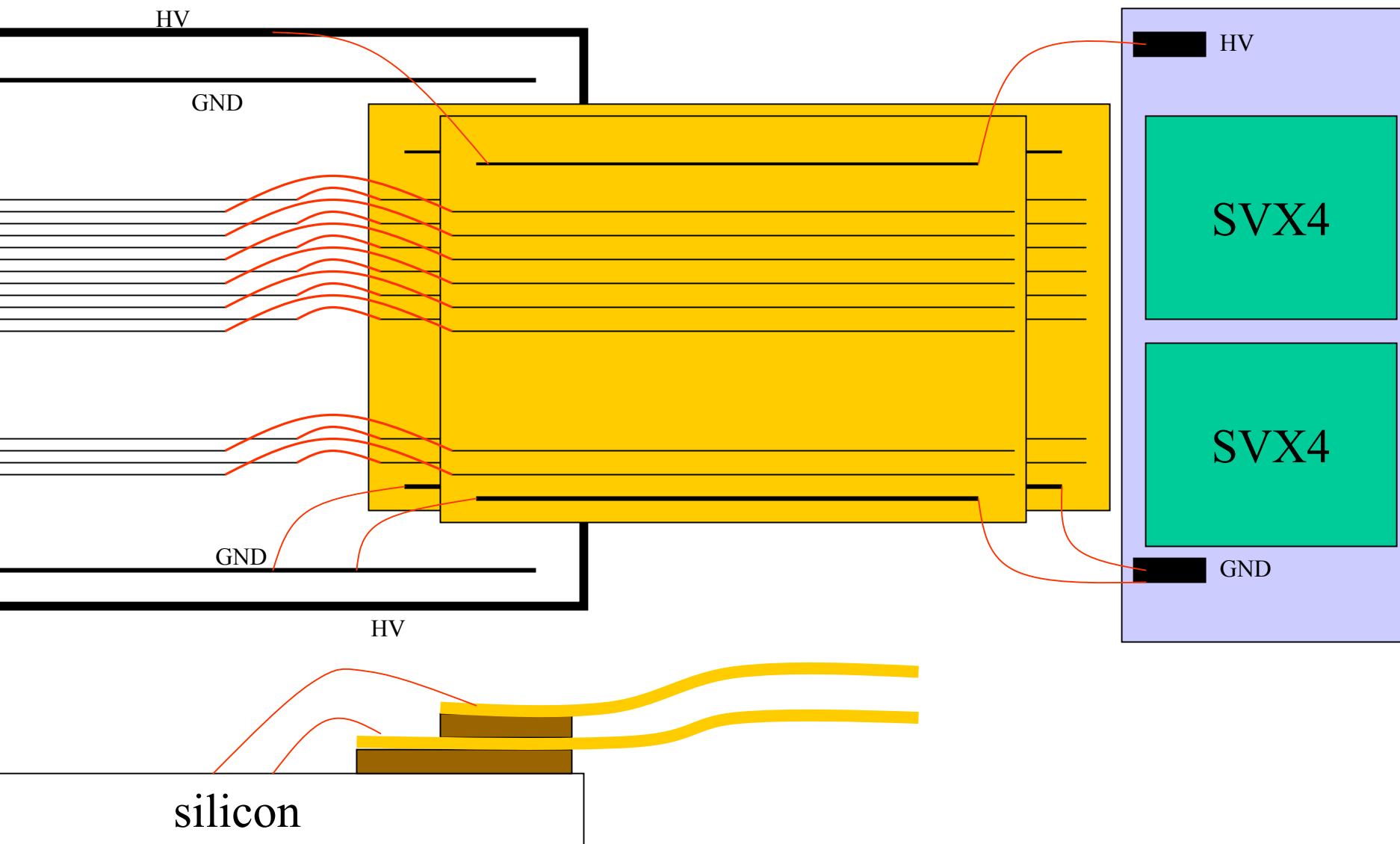
$$\text{Epsilon} = 0.7 * 1 + 0.3 * 3.5 = 1.75$$

Capacitance < 0.45 pF/cm

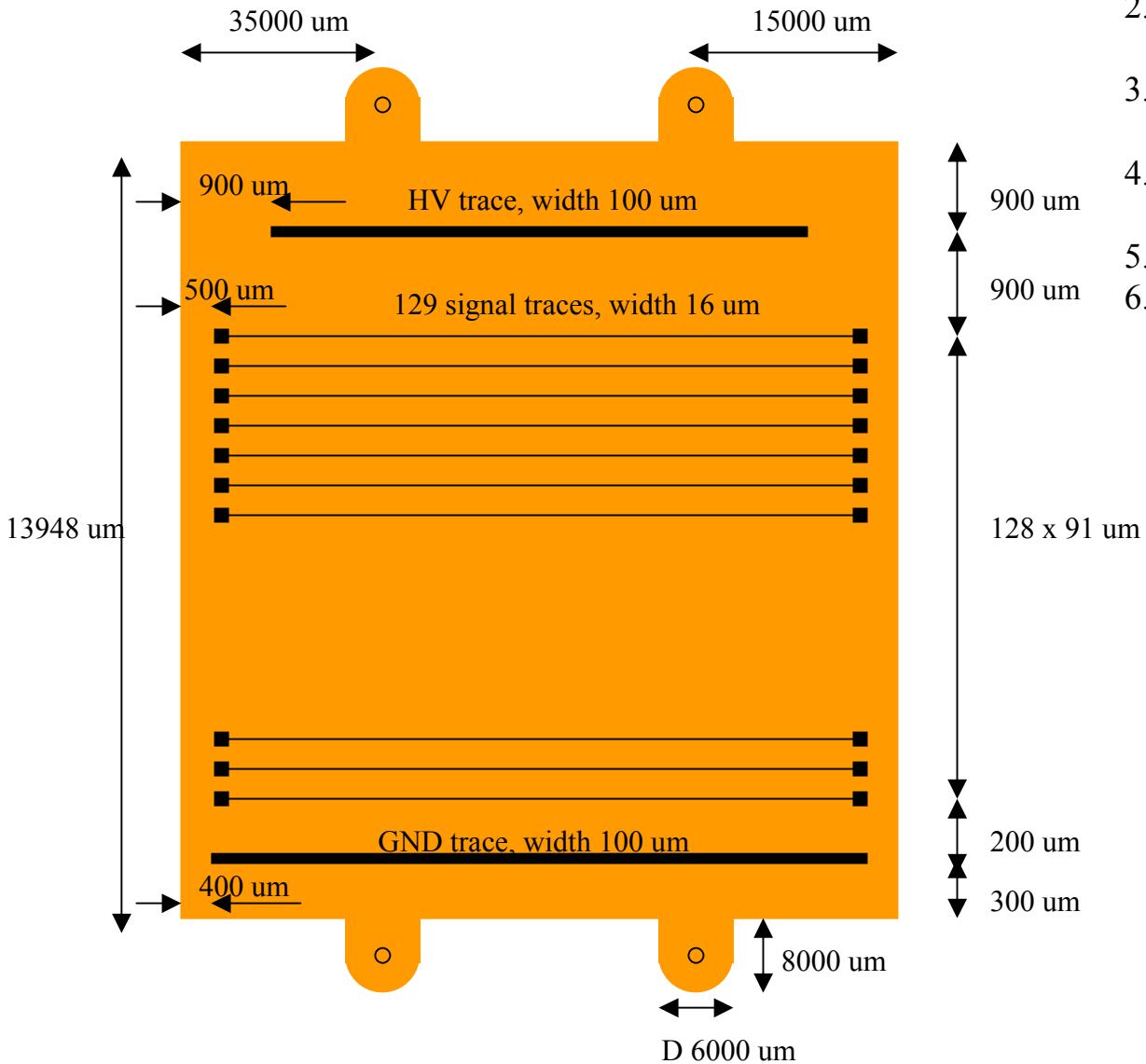
L0 connections



1. Metallization on n+ implant at the edge is used to route HV to HV pad
2. HV pad has a foil wrapped around the edge to the backplane
3. HV pad may also have a low pass filter



Analog cable design



1. Length 420 mm
2. Cable is symmetric left-right for the exception of “ears”
3. All distances are defined to centers of lines and pads
4. Bond pad size on signal traces is 150x60 um
5. “Ears” have fiducials in the center
6. HV trace has round shape at the ends

