

PROTOTYPE FLEX STRIPLINES FOR D0 SILICON READOUT

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Overview

An upgrade for the silicon detector system for the D0 experiment at Fermilab is now in the design and prototyping stage. This upgrade will require approximately 1000 flex circuit striplines of up to about 100 cm in length to carry signals and power. The production flex cables will be operated at normal indoor room temperature, pressure and humidity, but in a high radiation environment with an expected total exposure as large as several tens of Megarads. At least two lengths (maximum length ~ 100 cm) and at least two design versions will be required.

Both design versions will require prototyping. This document addresses prototyping for one of these versions, called "L1-5". The other version, called "L0", is now in the design stage, and will require a similar prototyping program commencing 1-2 months later.

A preliminary layout of the L1-5 flex cable is provided in the attached Word and Excel files. A CAD layout is available in several formats, including CADKEY .prt, and AUTOCAD .dwg, and .dxf.

The L1-5 flex cables have signal and power traces of 1-ounce copper on both sides of a Kapton dielectric of 5 mil total thickness. The standard trace width over most of the cable is 0.125 mm (4.9 mils). The smallest gap between traces is 0.150 mm (5.9 mils). One isolated trace will be run at up to 1000 V. Approximately 100 vias are required near the cable ends. The smallest via pads are ovals 0.8 mm x 1.6 mm, with vias separated by 0.8 mm. Two to four vias are used on each pad for redundancy. At each end of the cable are 46 gold-plated pads of pitch 0.5 mm for attachment of a miniature connector. Both sides of the cable will have a 1 to 2 mil coverlay; the coverlay over the gold pads will later be removed by laser ablation.

Scope and schedule of L1-5 prototyping

1. A run of 10 prototypes of length ~50 cm, i.e. short enough to be made with readily-available panels. These will be used to test overall design and to validate vendors for ablation and connector attachment.

Desired completion date: 15 March 2002 or sooner.

2. A run of 20 prototypes of 100 cm length, incorporating any changes mandated by (1).

Desired completion date: 1 June 2002.

3. A run of 40 prototypes of final design, to be used in test fixtures for other components in the silicon readout system.

Desired completion date: 15 November 2002.

Specifications

Number of flex lines required: Quotes on quantities of 10, 20 and 40 as described above are requested.

Length: 10 @ ~50 cm, 20+40 @ 100 cm

Dielectric: Kapton without fire retardant (e.g. Rogers R/flex 2001) 3.0 mils thick with 1.0 mil adhesive on each side, for a total of 5.0 mil dielectric thickness.

Thickness of copper: Standard 1 ounce (1.3 mil nominal thickness) on both sides.

Cover layers: Kapton cover layers top and bottom, each 1-2 mils thick including adhesive. The cover over the high-voltage trace must hold off 1000 V.

Width of signal traces: The nominal width of long traces is 0.125 mm (4.9 mils). For controlled impedance, the average width of each trace should be within $\pm 15\%$ of this value. Local variations in width along the length of a given line can be larger, $\sim \pm 25\%$. A simple measurement of the DC resistance of each line will be a sufficiently good measure of its average width.

Voltage holdoffs and accidental shorts: The broad power traces will carry currents of up to 1.0 A at 2.5 V. The single high-voltage line, which is separated by ~ 1 mm from the others, will be run at up to 1000 V. Shorts or arcing between lines or layers, or to neighboring grounded objects, must not occur.

Registration of layers: Transverse registration of the top and bottom copper layers over the full length should be maintained to ± 7 mils or better. Registration near the ends should be sufficient to allow reliable placement of vias.

Diameter of plated-through holes: A drill diameter of 8 to 12 mils is acceptable if consistent with the pad size (1.6 mm x 0.8 mm oval).

Resistance of plated-through holes: Resistance of the plated-through holes between top and bottom layers should contribute no more than an additional 0.025 ohms to the resistance of each trace. Note that 2-4 plated-through holes are used at each end of these traces to lower this resistance. A solid fill of the plated-through holes is acceptable and may be preferred.

Trimming: The flex cable is to be cut into a strip not exceeding 14.7 mm. The nominal gap between the outer edge of the dielectric and the nearest copper is 0.65 mm. It is desirable to maintain this gap as 0.65 mm (+0.0 –0.2) mm on the edge near the high-voltage trace, and as 0.65 mm (+0.0 –0.3 mm) on the other edge.

Connector pads

Subminiature 50-pin connectors (AVX 5046) will be installed on both ends by soldering to gold-plated pads on the flex. The manufacturer's specs on these pads are given below. Extensions of the pads beyond the gold-plated area are captured under the coverlay to help hold the pads down

Pitch of connector pads: 0.50 ± 0.05 mm

Width of connector pads: 0.30 ± 0.05 mm

Length of connector pads: 2.1 ± 0.1 mm

Testing by vendor

Visual inspection will be performed by the vendor over the full length of each line with a magnification sufficient to find serious defects and variations in trace width. It is expected that experience with the prototypes will generate testing procedures for the final cables.

After installation of connectors, each cable will be tested by us for shorts and opens, line resistance and impedance, and high-voltage holdoff.