

Specification of the Layer 2-5 Axial Hybrid for the upgraded D0 Silicon Microstrip Detector (Part 3823-112-EB-330380 Rev.2)

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Overview

The hybrid is to be constructed of alternating thick film layers of gold and dielectric built up onto a Beryllia substrate. There are six conductor layers and five dielectric layers on the top side. Layers of dielectric may be added to the backside of the substrate in order to keep the finished hybrid flat. In addition to these layers, a special dielectric pattern (glue channels) is to be applied to the backside. This layer facilitates control of epoxy to prevent run-out when the hybrid is glued to the silicon sensors. The top metal layer will consist of two different finishes. Some pads will be compatible for aluminum-wedge bonding while other pads must be solderable. The solderable layer will be represented by a separate layer drawing. The layout of all the layers is defined in both .dxf format and Gerber and accompany this specification together with a general hybrid drawing.

Specifications

Dimensions and Flatness

1. Laser cutting should produce a final outline of 50mm +/-0.05mm by 41.9mm +/-0.05mm (1.968" +/- 0.002" by 1.649" +/- 0.002"). Cut edge location should be accurate to +/-0.05mm (+/- 0.002") to the overall artwork pattern, Layer 1 Conductor Top. Fiducial marks will be referenced to aid in accomplishing this alignment. See drawing 3823.220-MD-399797.
2. Total thickness of the finished hybrid must not exceed 0.95mm (37.4mil) (i.e. the hybrid should lie between two parallel planes separated by not more than 0.95mm)
3. Flatness of the top and bottom surfaces of the finished hybrid must be within 0.15 mm (i.e. all points on the surface lie between two parallel planes separated by 0.15 mm or less)
4. Minimum thickness of the 99.5% BeO substrate is 0.305mm (12 mil)
5. Glue channels on backside of substrate should have a minimum depth of 0.05mm (2.0 mil) and the cross-sectional area of the channels is to be not less than 0.070 square mm at all locations along a channel. See drawing 3823.220-MD-399797.

Electrical

6. Dielectric layer thickness is to be 25 um (1 mil) minimum, with a dielectric strength of 500V/mil or better.
7. Thickness of metal trace layers is recommended to be 6 um (0.236 mil) minimum, 10 um (.394 mil) maximum.
8. Flying Probe resistance measurements for all nets for each hybrid is requested. The output can be hard copy or files. As a minimum requirement, resistance measurements of the clock lines is to be made, and the resistance of the clock lines is to be smaller than 10 Ohms. See section "Resistance Measurement of Clock Lines" below.

9. Vendor must test 100% all nets for continuity, which includes opens and shorts
10. Ground and power plane layer thickness is to be 4 um (0.157mil) minimum, 8 um (0.315 mil) maximum..

Miscellaneous

11. Bond pads should be thick film gold formulated for aluminum wedge bonding with a typical thickness of 7-11um (0.275-0.433 mil).
12. Solder pads should be of Platinum Palladium Gold Pt/Pd/Au with a minimum thickness of 15um and should be formulated for soldering with Sn62 solder.
13. Surface area under each of the ten SVX chips must be conductive, open on the solder mask layer and should accept silver epoxy.
14. Soldermask on vias is preferred.
15. Silkscreen is to be applied for component identification

Standards of Testing shall be according to these Mil-Specs

Vendor must adhere to standards of fabrication and testing as described in the following specs.

- MIL-STD 883E Method 2011.7 Bond Strength (Destructive Bond Pull Test)
- MIL-STD 977 Method 4500 Metalization Adherence (Tape Test)
- MIL_STD_883E Method 2019.5 Die Shear Strength

Documentation

Vendor should provide a Quality Inspection Test document for each lot of product that is manufactured.

This document should provide tests and procedure references as follows:

- | | |
|---|---|
| • Visual inspection | Test sample 100% |
| • Physical Dimensions (including thickness) | Test sample 100% |
| • Electrical Tests | Test Sample 100% |
| • Film Adhesion | Test sample 5% but at least two pieces. |
| • Wirebond Evaluation | Test Sample 5% but at least two pieces. |
| • Die Shear | Test Sample 5% but at least two pieces. |
| • Solder Pad Evaluation | Test Sample 5% but at least two pieces. |
| • Warp and Camber | Test Sample 10% but at least four pieces. |
| • Glue channel depth | Test Sample 5% but at least two pieces. |

Beryllia (Beo) Decontamination and Handling

Fermilab standards require that the hybrids be decontaminated for Beryllia dust.. Vendor should thoroughly wash with hotwater and rinse with alcohol and handle the hybrid to assure minimal beryllia dust contamination.

Vendor can verify his decontamination process through this third party source.

Consult Natlscs Loss Control of Long Grove for further details.

1 Kemper Dr, Long Grove, IL 60049
 Bill Walsh 847.320.7188

Resistance Measurement of Clock Lines

Two lines are to be measured for proper maximum resistance, CLK, and /CLK. The table below shows coordinate locations for either end of these nets. Resistance for each line is to be 10 ohms maximum.

Net	ProbeA (inches)	ProbeB (inches)	ProbeA (mm)	ProbeB (mm)
CLK	(1.06, 1.2)	(1.395, .644)	(26.92, 30.5)	(35.43, 16.36)
/CLK	(1.04, 1.2)	(1.37, .644)	(26.42, 30.5)	(34.80, 16.36)

Delivery Schedule

- Partial deliveries are accepted.

Contacts

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Build Files Gerber And AutoCad

Manufacturing Files contained in hdi-10c_axial_061103_mfg.zip.zip

- Note Gerber files 274X extension *.GBX
- AutoCAD files in DXF format R12
- This page refers only to layers on the top side of the substrate
- Note that Layer 11 is closest to the substrate

06/13/2003	10:12a	2,799,457	hdi-10c_axial_061103_mfg.zip.zip
06/11/2003	04:35p	232,714	DRD.GBX
06/13/2003	09:44a	7,796,976	hdi-10c_axial_061103_DRD.dxf
06/11/2003	04:35p	44,597	FAB.GBX
06/13/2003	09:40a	1,612,394	hdi-10c_axial_061103_FABdrw.dxf
06/13/2003	09:02a	8,374,247	hdi-10c_axial_061103_L1.dxf
06/11/2003	04:35p	243,144	LAYER 1 CONDUCTOR TOP.GBX
06/13/2003	10:02a	183,830	hdi-10c_axial_061103_L10.dxf
06/11/2003	04:35p	13,507	LAYER 10 DIELECTRIC.GBX
06/13/2003	09:23a	736,568	hdi-10c_axial_061103_L11.dxf
06/11/2003	04:35p	26,682	LAYER 11 CONDUCTOR BOTTOM.GBX
06/13/2003	09:28a	233,559	hdi-10c_axial_061103_L2.dxf
06/11/2003	04:35p	21,796	LAYER 2 DIELECTRIC.GBX
06/13/2003	09:48a	3,096,359	hdi-10c_axial_061103_L3.dxf
06/11/2003	04:35p	98,144	LAYER 3 CONDUCTOR.GBX
06/13/2003	09:50a	227,949	hdi-10c_axial_061103_L4.dxf
06/11/2003	04:35p	21,642	LAYER 4 DIELECTRIC.GBX
06/13/2003	09:52a	1,110,420	hdi-10c_axial_061103_L5.dxf
06/11/2003	04:35p	41,428	LAYER 5 CONDUCTOR.GBX
06/13/2003	09:54a	203,788	hdi-10c_axial_061103_L6.dxf
06/11/2003	04:35p	17,296	LAYER 6 DIELECTRIC.GBX
06/13/2003	09:56a	2,546,486	hdi-10c_axial_061103_L7.dxf
06/11/2003	04:35p	80,824	LAYER 7 CONDUCTOR.GBX
06/13/2003	09:59a	193,993	hdi-10c_axial_061103_L8.dxf
06/11/2003	04:35p	14,868	LAYER 8 DIELECTRIC.GBX
06/13/2003	10:01a	436,374	hdi-10c_axial_061103_L9.dxf
06/11/2003	04:35p	19,812	LAYER 9 CONDUCTOR.GBX
06/13/2003	09:31a	7,380,656	hdi-10c_axial_061103_SMT.dxf
06/11/2003	04:35p	222,240	SMT.GBX
06/13/2003	09:33a	310,001	hdi-10c_axial_061103_SPT_PPT.dxf
06/11/2003	04:35p	16,163	PPT.GBX
06/13/2003	09:35a	310,008	hdi-10c_axial_061103_SPT_PPT2.dxf
06/11/2003	04:35p	16,163	SPT.GBX
06/13/2003	09:38a	808,266	hdi-10c_axial_061103_SST.dxf
06/11/2003	04:35p	25,761	SST.GBX

