Full chain tests at DAB

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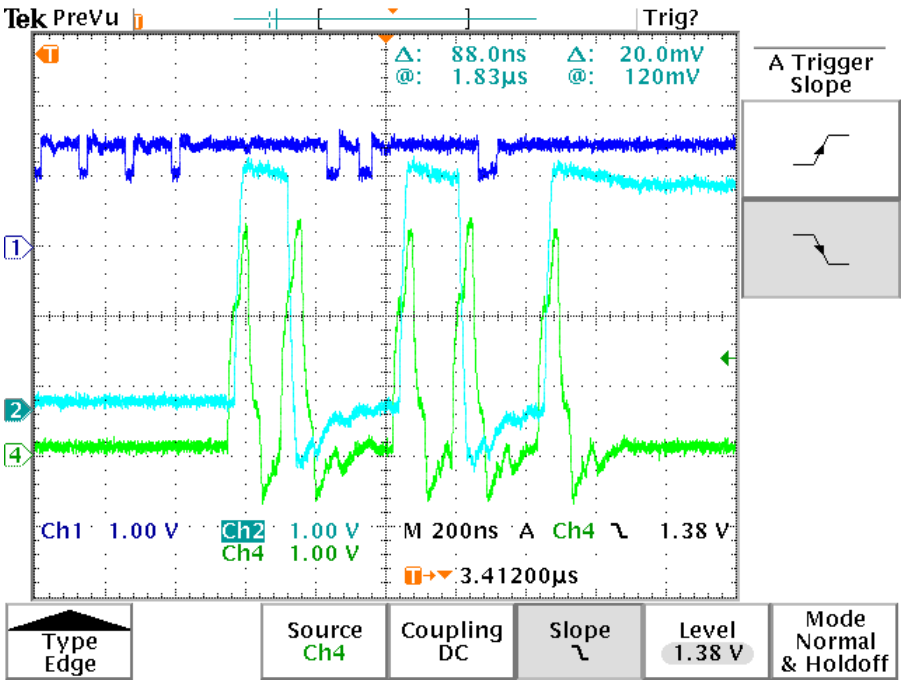
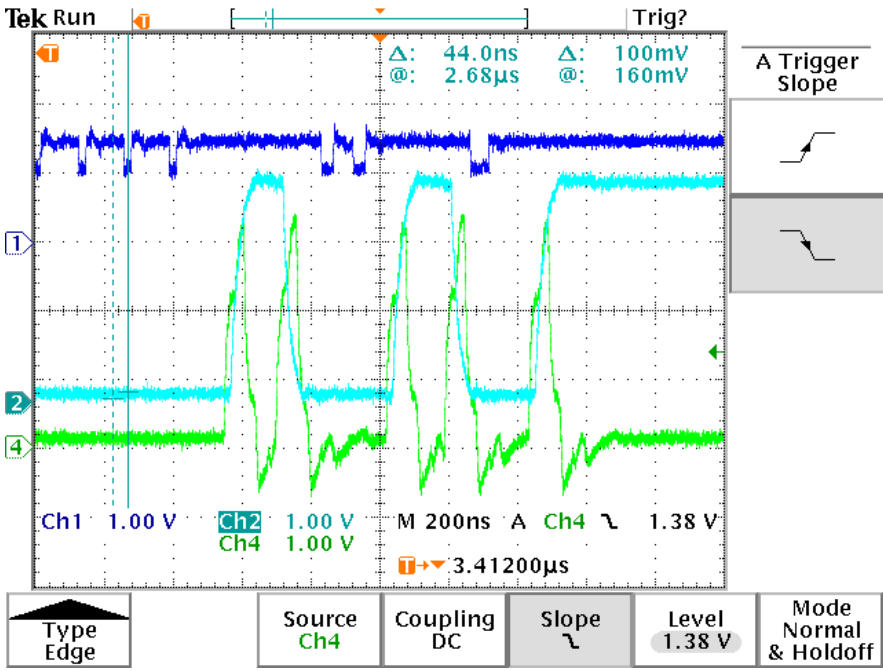
Configuration : Hybrid –Jumper Cable – Junction Card – Twisted Pair Cable – Adapter Card – Interface Board – SASEQ

- Studied:
  - Signal propagation through twisted pair cable + jumper cable
  - Signal levels to/from SVX4/AC/IB adequate?
  - Can clock bypass AC ?

Full chain test

- Signals at the hybrid : FE_MOD, CH_MOD
  - Also shown /CLK at AC
  - Transition between Acquire and Digitize (D0 mode)
  - 90 Ohm at AC shorted
  - 90 Ohm at AC for FE_MOD

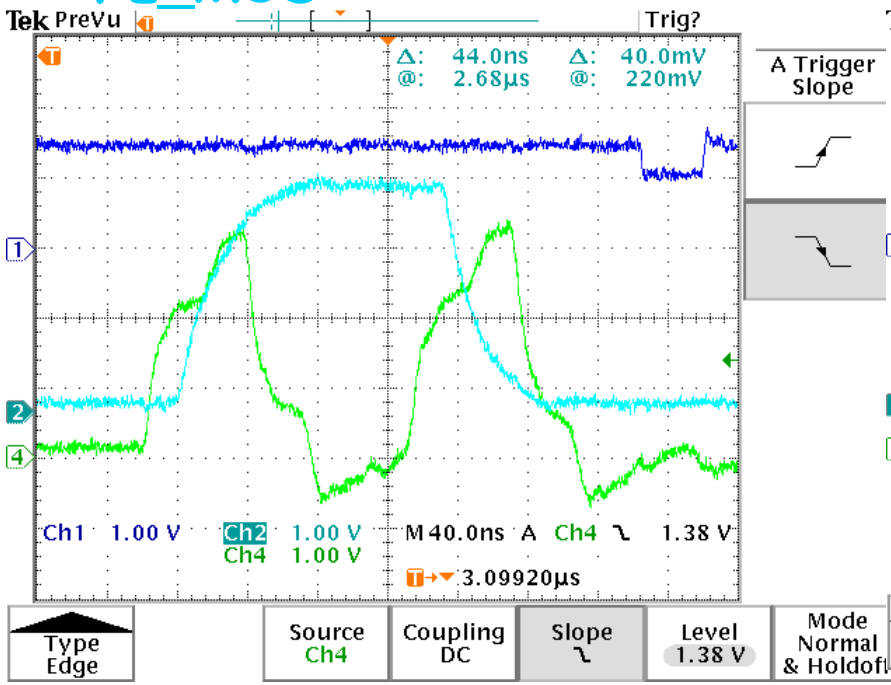




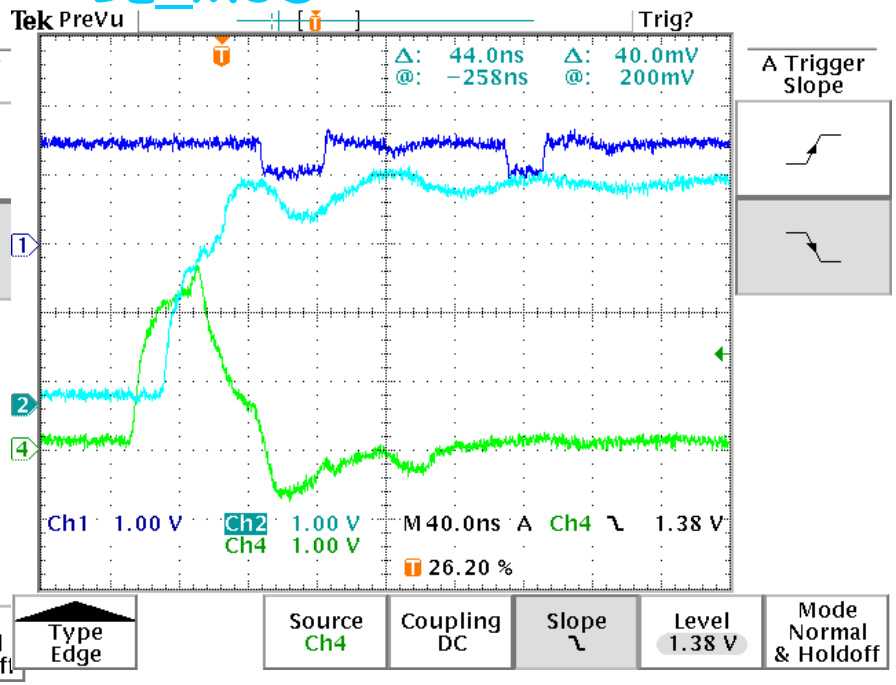
Full chain test

- Signals at the hybrid : FE_MOD & BE_MOD, CH_MOD
  - Also shown /CLK at AC
  - 90 Ohm at AC for FE_MOD & PRI_IN

FE_MOD



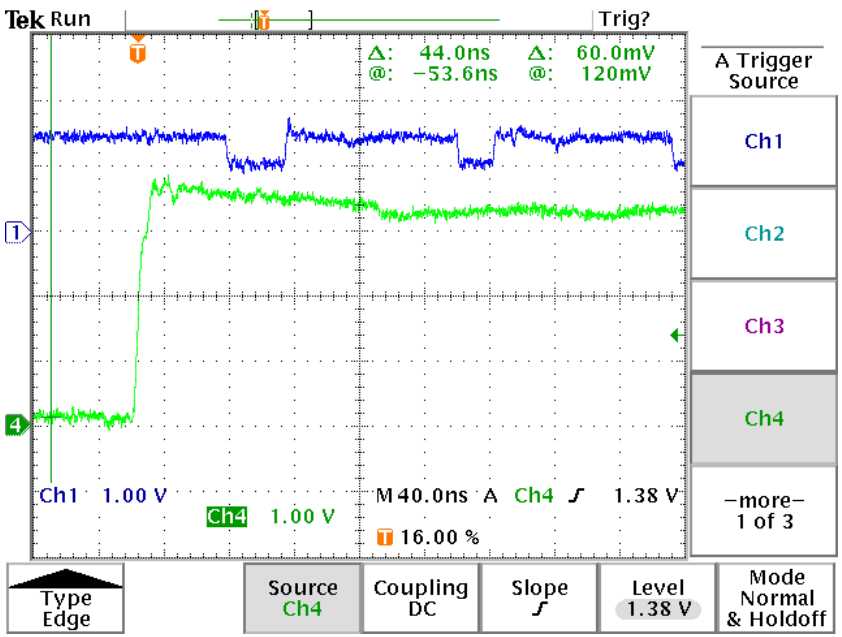
BE_MOD



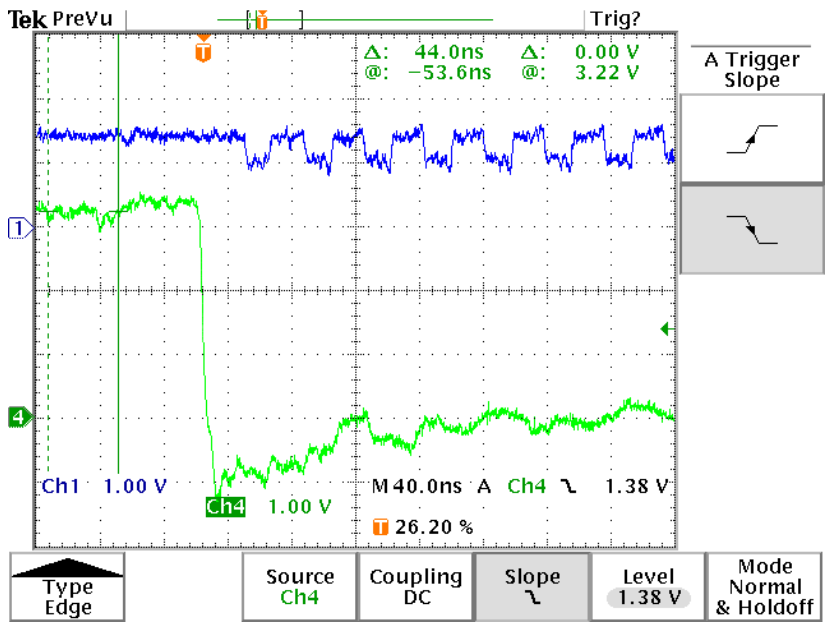
Full chain test

- Signals at the hybrid : PRI_IN
  - Also shown /CLK at AC
  - All 90 Ohm at AC shorted

PRI_IN rising

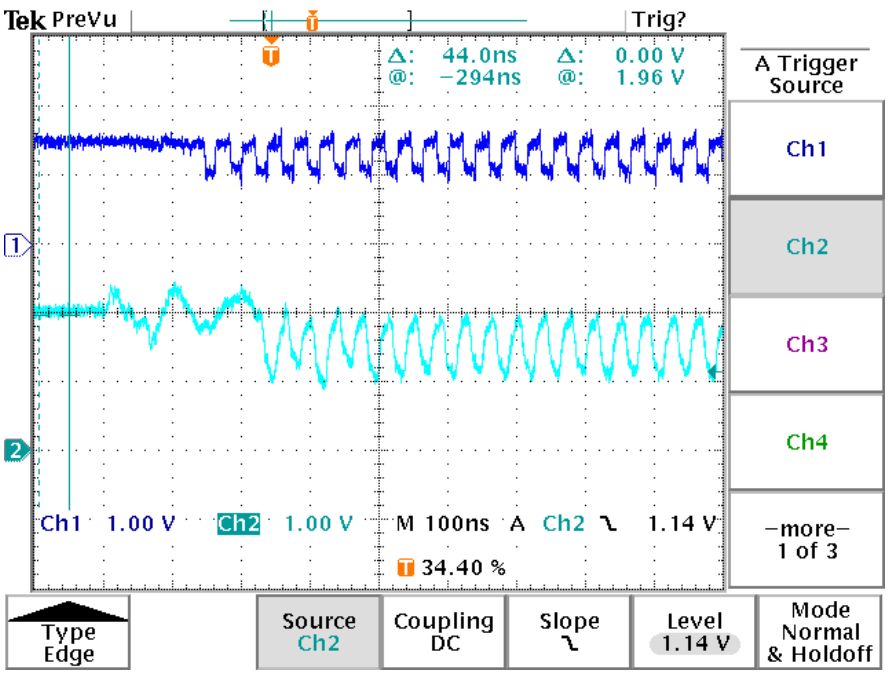


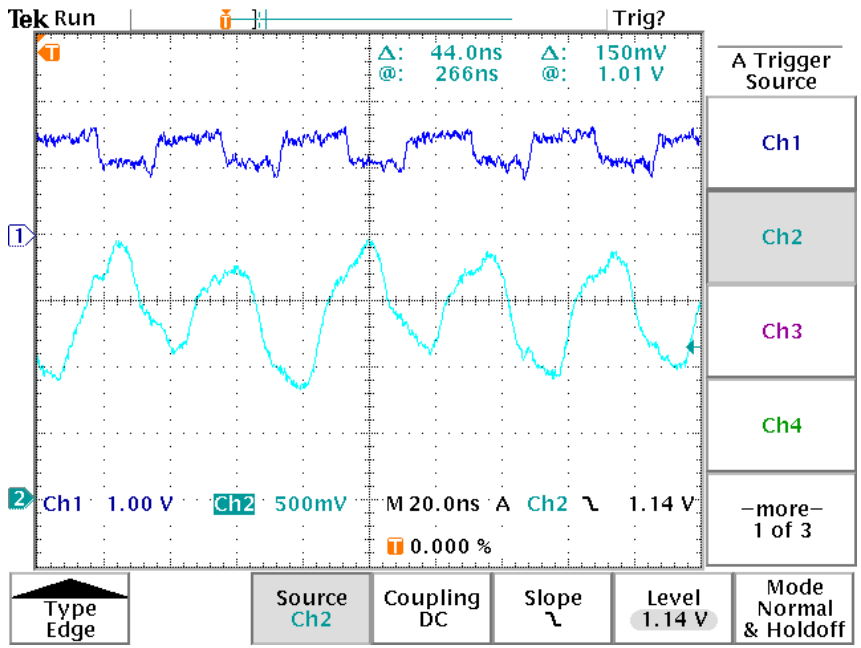
PRI_IN falling



Full chain test

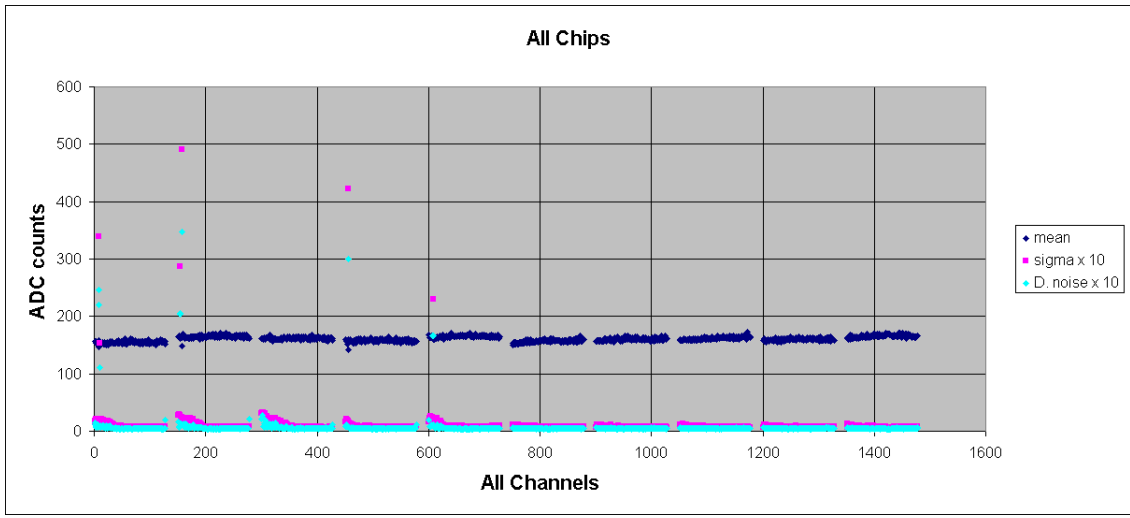
- Signals at Adapter Card : /DVALID
  - Also shown /CLK at AC



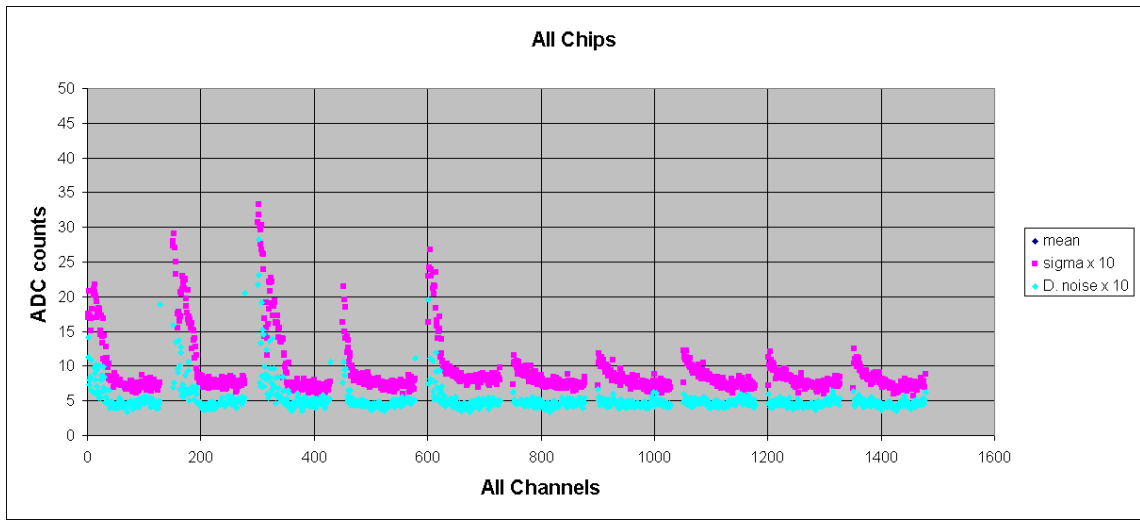


Full chain test

- Pedestals and noise
  - No corrupted data seen (in ~1000 events)
  - Noise structure in first 5 chips

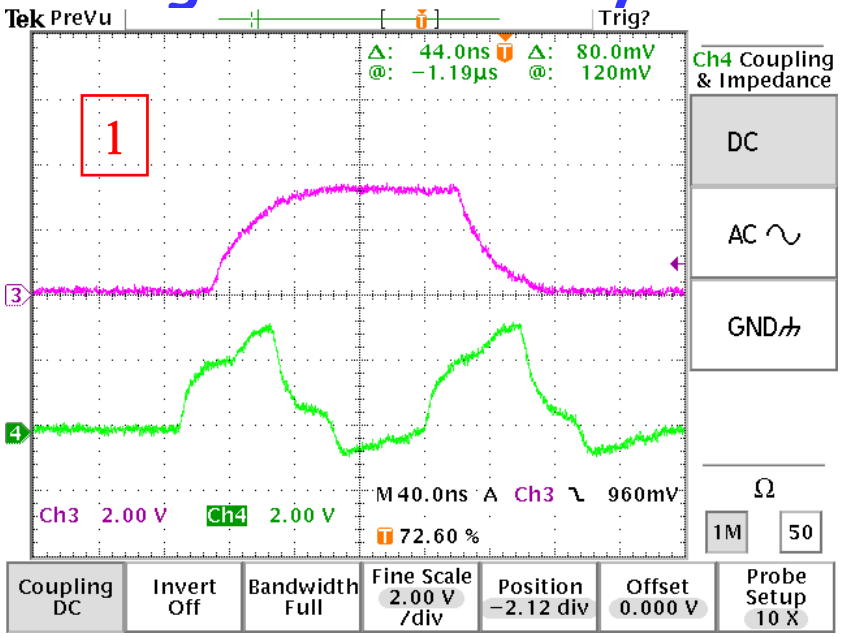


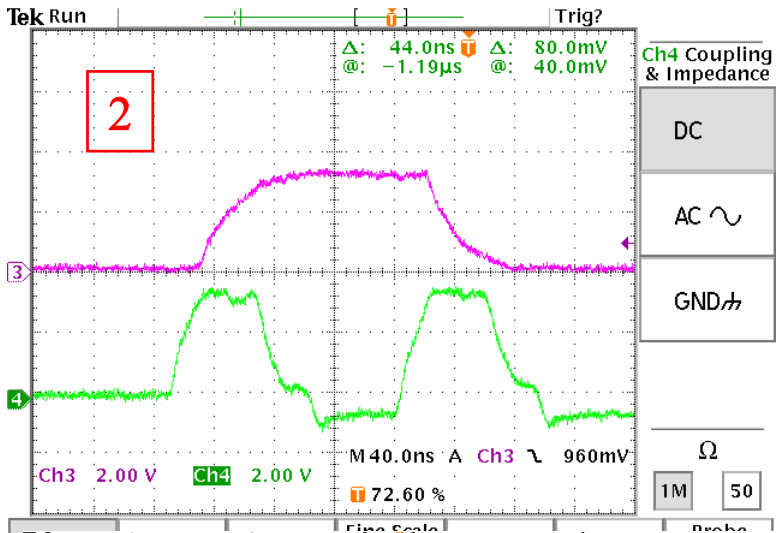
  - Attempt to bypass clock failed so far
    - Data corrupted

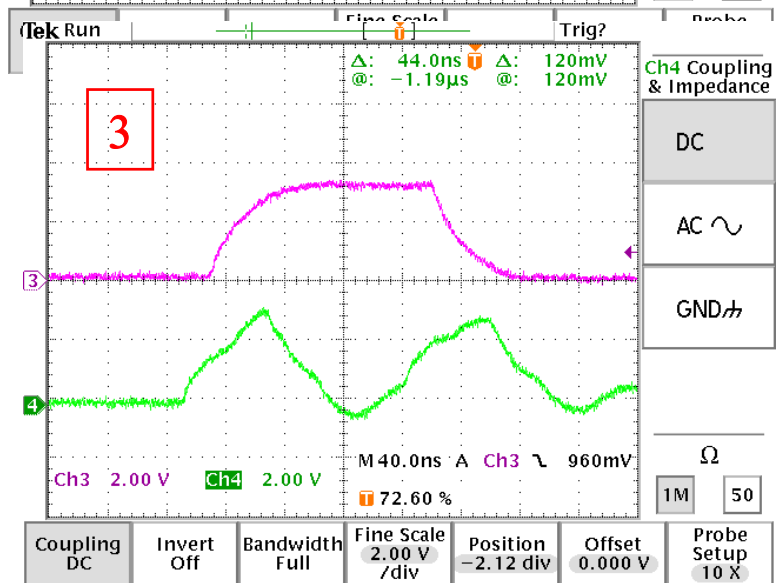


Full chain test

- Signals at the hybrid : FE_MOD & CH_MOD







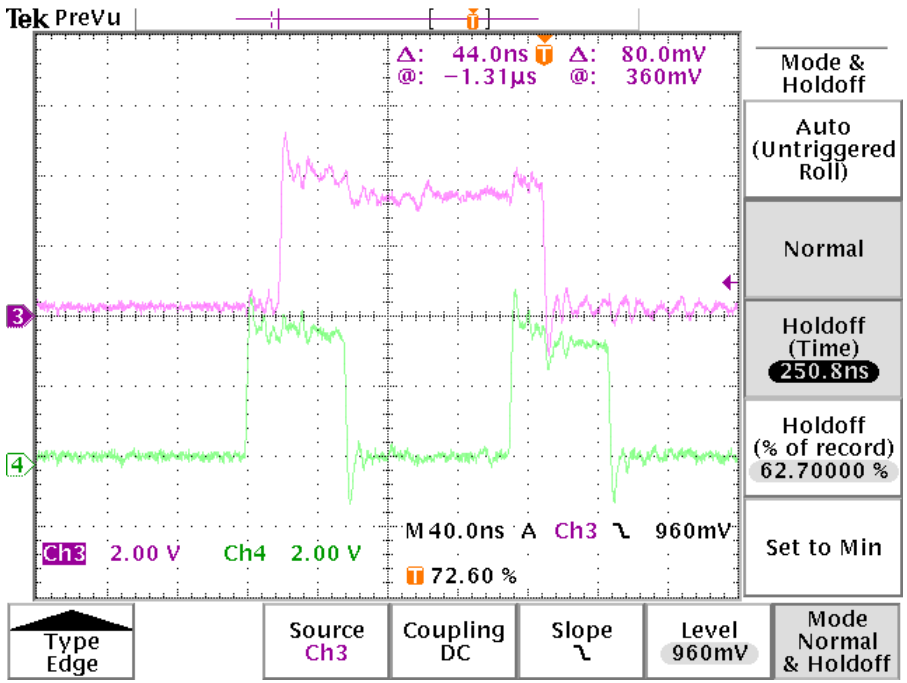
1. CH_MOD : 0 ohm AC, 110 ohm hybrid
2. CH_MOD : 0 ohm AC, open @ hybrid
3. CH_MOD : 90 ohm AC, open @ hybrid

- Everywhere : FE_MOD 90 ohm AC, open @ hybrid

Full chain test

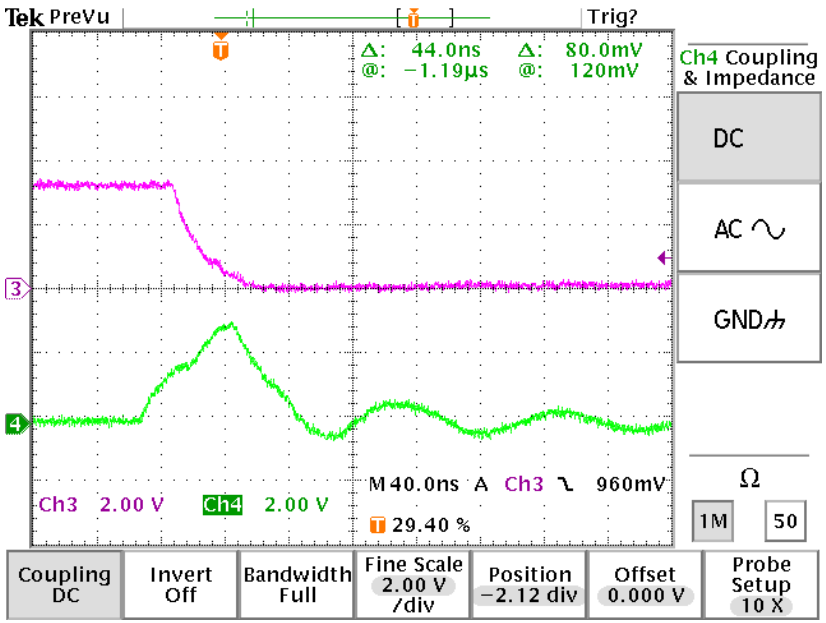
- Signals at SASEQ – just to show correct timing:

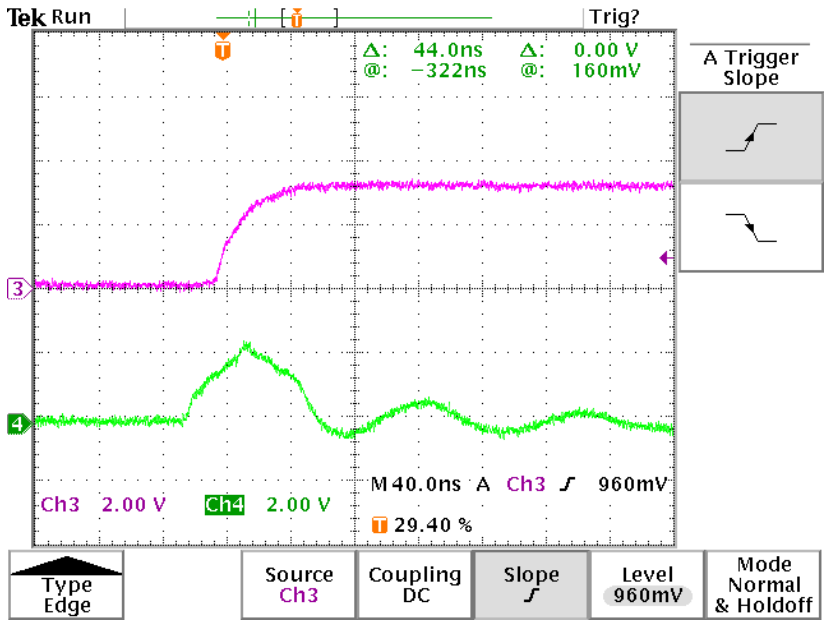
  FE_MOD & CH_MOD



Full chain test

- Signals at the hybrid : BE_MOD & CH_MOD

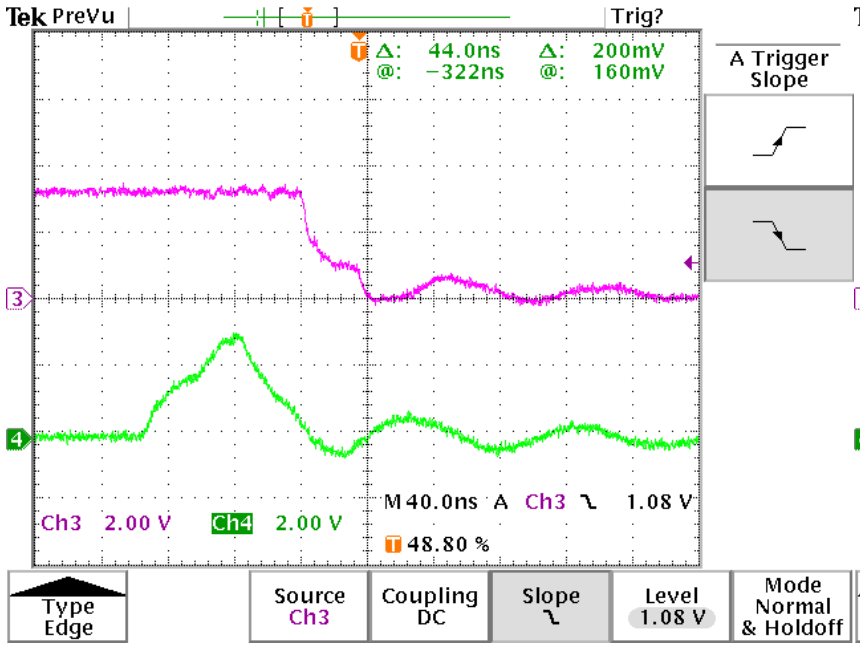


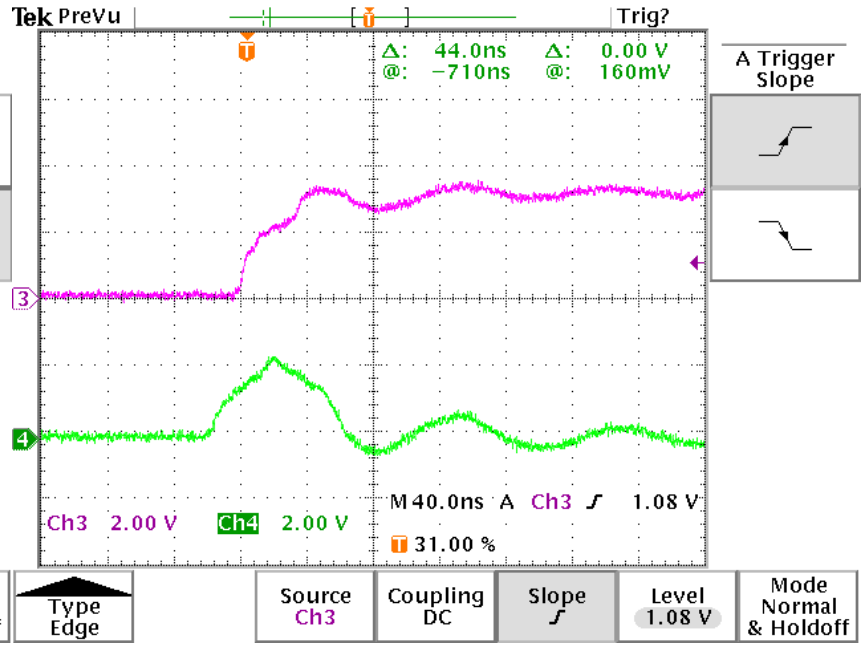


- CH_MOD : 90 ohm AC, open @ hybrid
- FE_MOD 90 ohm AC, open @ hybrid - two edges

Full chain test

- Signals at the hybrid : PRI_IN & CH_MOD





- CH_MOD : 90 ohm AC, open @ hybrid
- PRI_IN 90 ohm AC, open @ hybrid - two edges