



DZero Silicon Tracker for Run IIb at the Tevatron

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Abstract

The DZero silicon tracker is planned to be upgraded after 2005 to withstand the increased luminosity of the Tevatron collider. The new tracker will have 6 layers of single-sided silicon sensors read out with the radiation hard SVX4 chip. This contribution describes the design of the new tracker and some results of prototype testing. © 2001 Elsevier Science. All rights reserved

Keywords : silicon detector; analog cable, SVX4 readout chip

1. Introduction

The DZero collaboration proposed to upgrade its silicon microstrip tracker (SMT) to meet challenges of the increased luminosity for the Tevatron collider at Fermilab. The upgraded tracker will be based on the single-sided silicon sensors and will be read out with a newly developed SVX4 chip. Both the sensors and the chips have sufficient radiation hardness to withstand up to $\sim 20 \text{ fb}^{-1}$ of integrated luminosity. The currently employed tracker, SMT, was designed to last $\sim 2 \text{ fb}^{-1}$.

The innermost layer of the new tracker is positioned closer to the interaction point (20 mm versus 27 mm in SMT) resulting in the improved impact parameter resolution. The higher instantaneous luminosity motivated the increase in the number of layers from four to six with the outer radius increased from 100 to 165 mm. This allowed to improve the pattern recognition and momentum resolution of tracking. Two innermost layers (Layer 0-1) of the tracker have axial only readout while the four outer layers (Layer 2-5) have both axial and small angle stereo readout.

In the following only some selected topics and results of the prototype testing will be presented. The

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full review of the design parameters and the physics program of Run IIb can be found elsewhere [1], [2].

2. Analog cable in Layer 0

In the innermost layer of the tracker the sensors are connected to the readout chips via analog cable. While very attractive because of the material and heat removal from the sensitive volume this approach represents a considerable technical challenge because of the fine strip pitch of the cable. Addition of the analog cable deteriorates the noise performance both because of the additional load capacitance and potential environmental noise pick-up.

In the proposed design two cables with constant $91\mu\text{m}$ pitch are laminated together with a lateral shift of $45.5\mu\text{m}$ to achieve the effective strip pitch of $45.5\mu\text{m}$. The cable is printed on the kapton substrate with maximum length of 464 mm and the trace width of $16\mu\text{m}$. The total capacitance of the cable assembly is approximately 0.5 pF/cm . The cables were successfully prototyped at Dyconex (Switzerland) with essentially 100% yield for the last batches.

Several Layer 0 module prototypes have been prepared using 7.9 cm long, $50\mu\text{m}$ readout pitch silicon sensors with intermediate strips from ELMA (Russia), 420 mm long analog cables and new SVX4 readout chips. The detailed description of SVX4 specifications and modes of operation can be found elsewhere [3]. The signal-to-noise ratio for the modules was measured to be equal to 11:1. The capacitive coupling between cables and surrounding ground is essential to understand the random noise and pick-up noise behavior. The additional pick-up noise is small if the distance from the ground surfaces to the traces is $500\mu\text{m}$ or more. Good, low inductance ground connections are also important to mitigate the pick-up noise. More information on the shielding and grounding issues for the D0 analog cable can be found in [4] and [5].

3. Layer 2-5 Module Prototyping

Layer 2-5 modules consist of a hybrid with sensors attached from two sides. The length of each sensor segment can be 10 cm or 20 cm. In the latter

case two 10 cm long sensors are ganged together by bonding. Sensors from Hamamatsu (Japan) are employed with $60\mu\text{m}$ readout pitch and intermediate strips. The sensors have a radiation hard layout inspired by the sensors used by the CMS collaboration. The hybrids accommodate ten daisy chained SVX4 chips, five to read out each side of the module.

The 20 cm long silicon strips represent a considerable capacitive load on the input of the preamplifier. Several module prototypes have been assembled to measure the noise performance of the irradiated and non-irradiated sensors. In the case of non-irradiated sensors the noise can be described as $\text{ENC} = 800\text{ e} + 600\text{ e/sensor}$, resulting in the signal-to-noise ratio of 16:1 for 10 cm long detectors and 11:1 for 20 cm long detectors.

Some of the sensors have been irradiated to a dose of 0.65 Mrad and then assembled into a Layer 2-5 module with 10 cm long detectors. The noise has been studied as function of temperature. It was found that at -10°C the contribution of the shot noise to the total noise is negligible while at $+20^\circ\text{C}$ the shot noise starts to contribute to the total noise decreasing the signal-to-noise ratio from 16:1 to 13:1. Correspondingly the leakage current increased from $0.13\mu\text{A}/\text{strip}$ at -10°C to $2.3\mu\text{A}/\text{strip}$ at $+20^\circ\text{C}$.

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References

- [1] DZero RunIIb Technical Design Report, FERMILAB-PUB-02-327-E, December 2002.
- [2] J.Fast, 'The DZero Silicon Detector for Run IIb at the Tevatron', Proceedings of 8th Topical Seminar on Innovative Particle and Radiation Detectors, Siena, Italy, October 2002.
- [3] M.Garcia-Sciveres, 'SVX4 chip', Proceedings of Vertex2002, Hawaii, USA, November 2002.
- [4] B.Quinn, 'Silicon Detector Grounding', Proceedings of Vertex2002, Hawaii, USA, November 2002.
- [5] K.Hanagaki, 'Layer 0 in DZero Silicon Tracker for Run IIb', Proceedings of Vertex2002, Hawaii, USA, November 2002.

