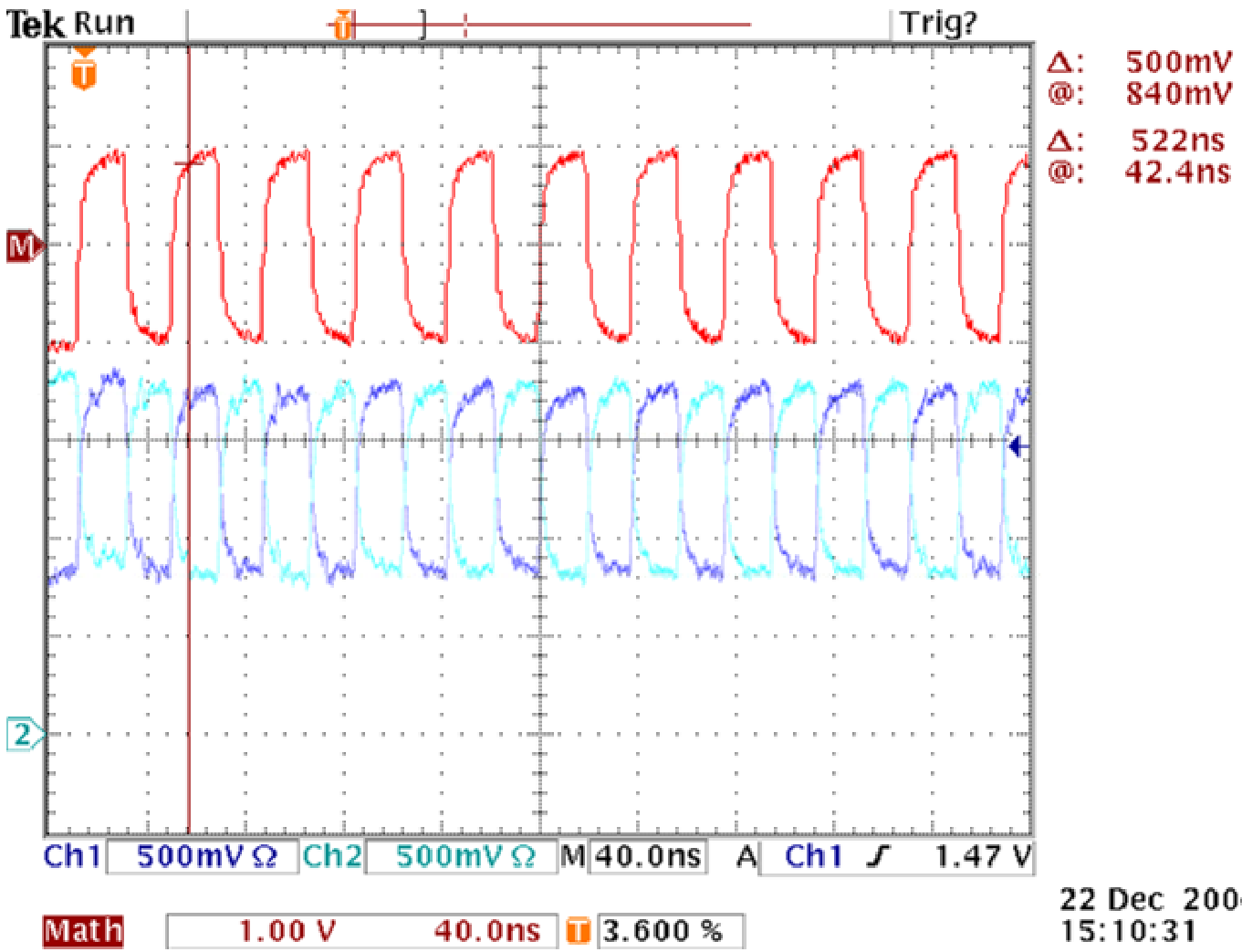
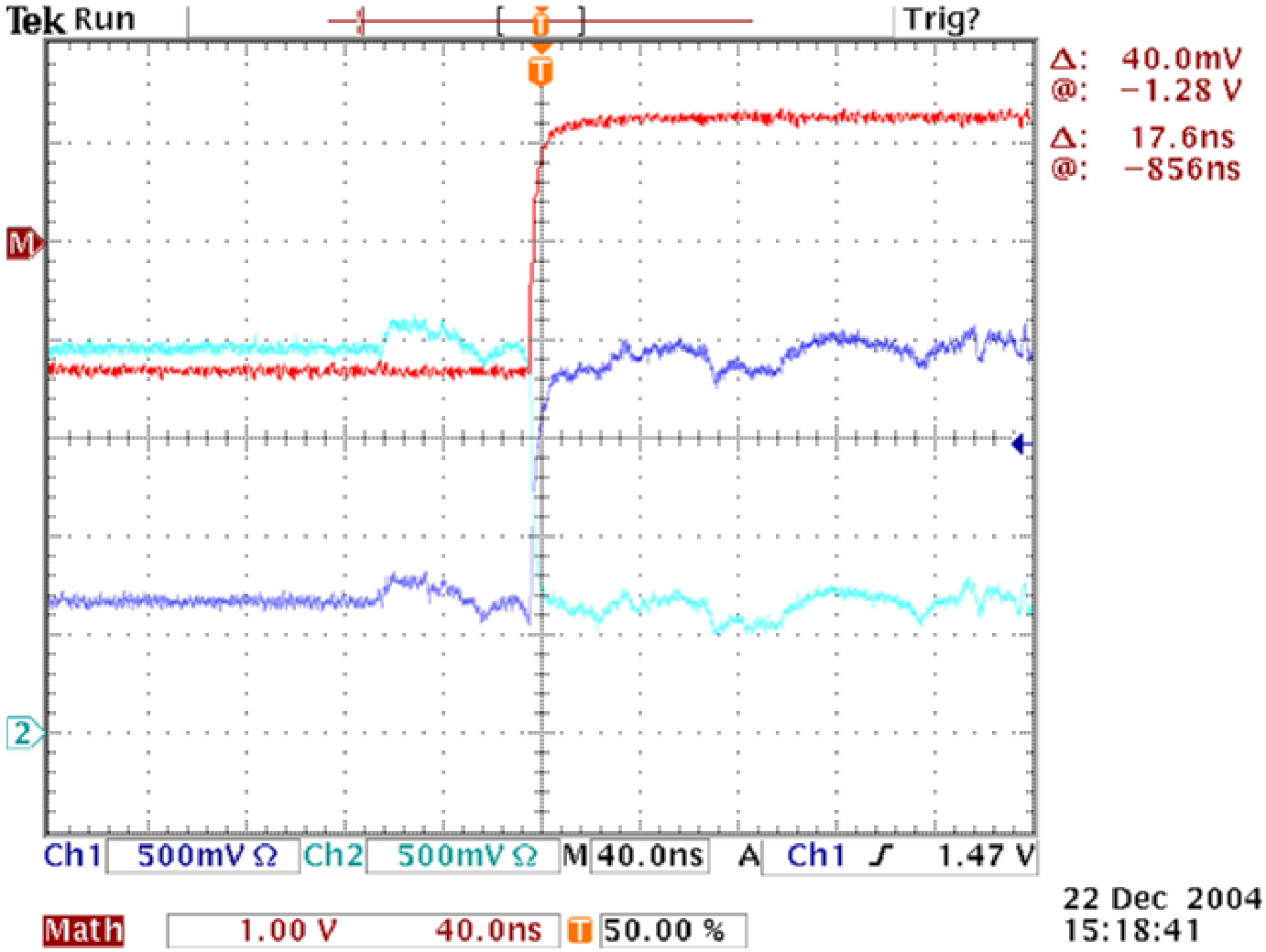
AC-Hybrid Signal Observations

- Purpose: To insure the signals communicated between the Adapter Card and Hybrid are proper.

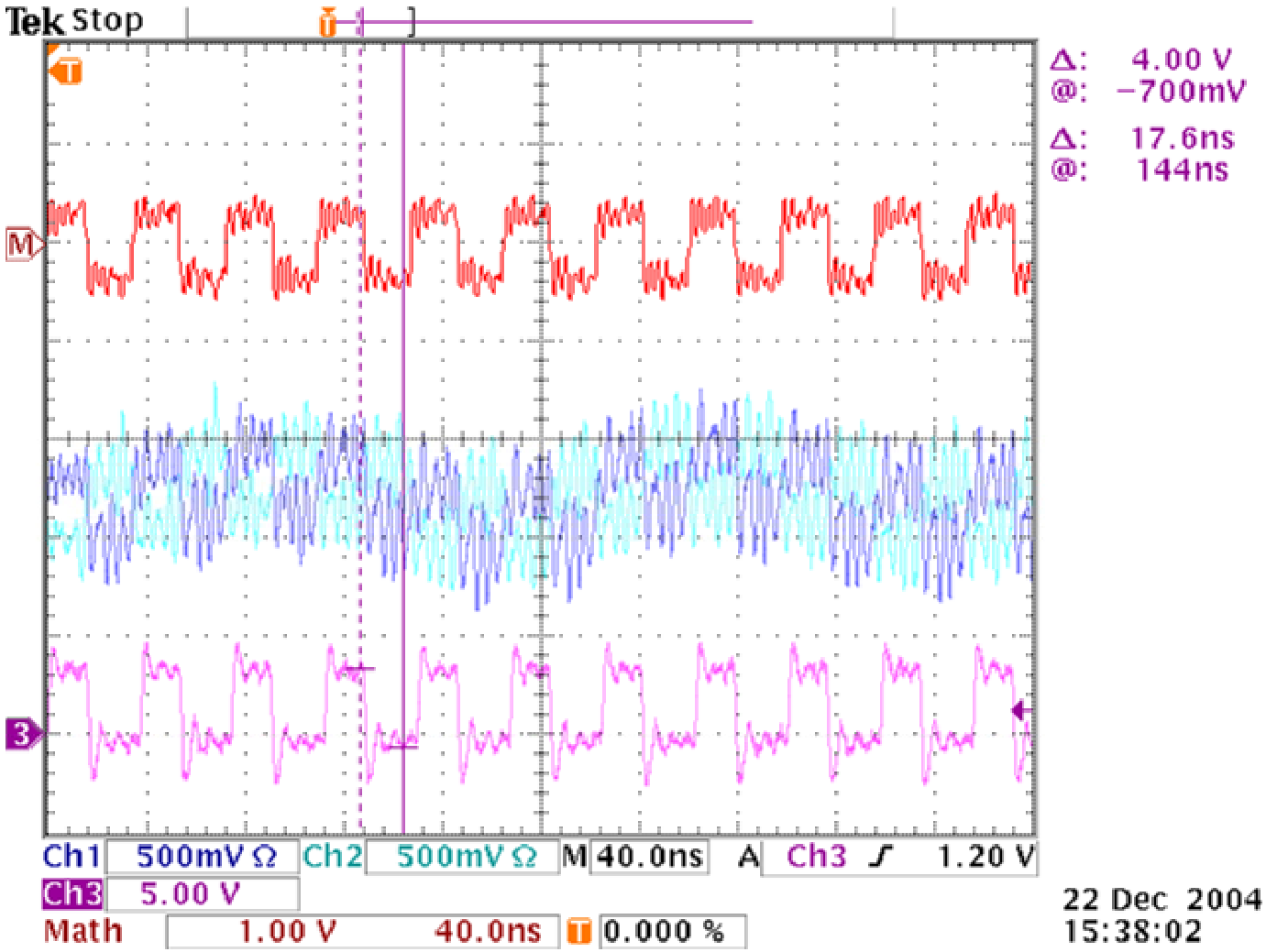
Dvalid signal at the adapter card 44 pin connector.



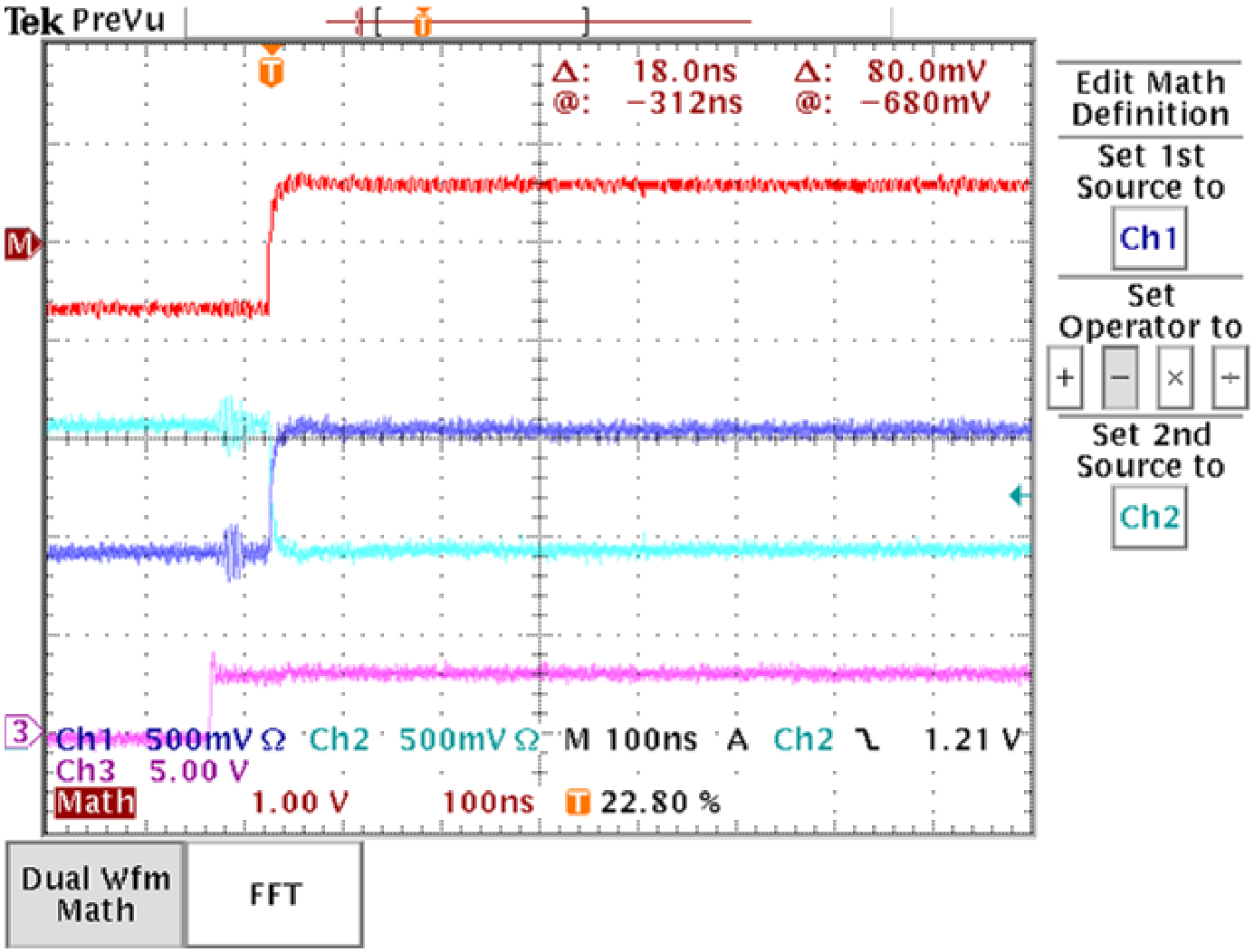
Priority Out at the adapter card 44 pin connector.



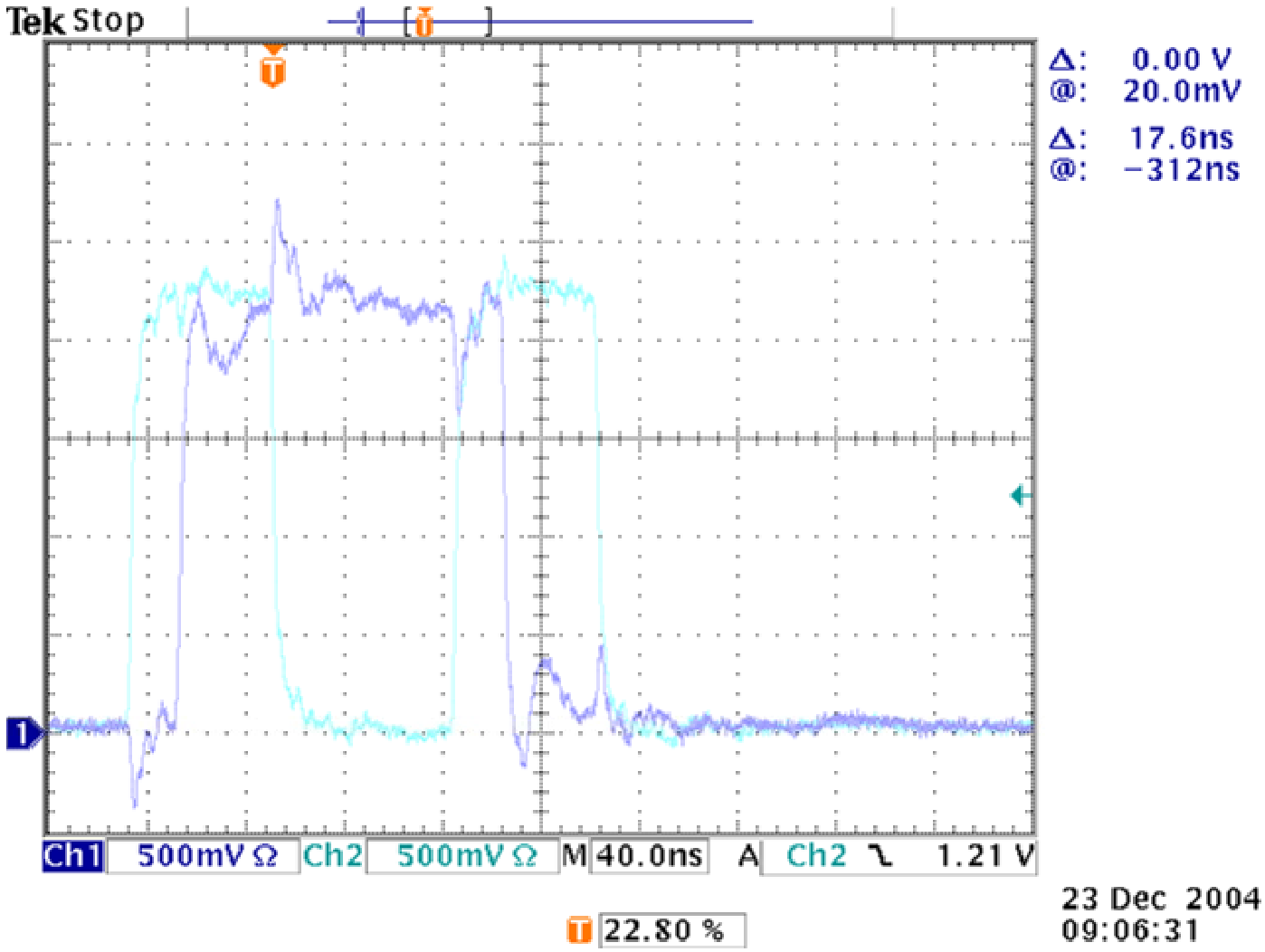
Clock and /Clock at the hybrid. Channel 3 is Data Valid at the interface board.



Data 7 at the hybrid. Channel 3 is Data 7 at the interface board.



Channel 1 is FE Mode, channel 2 is Change Mode at the hybrid.



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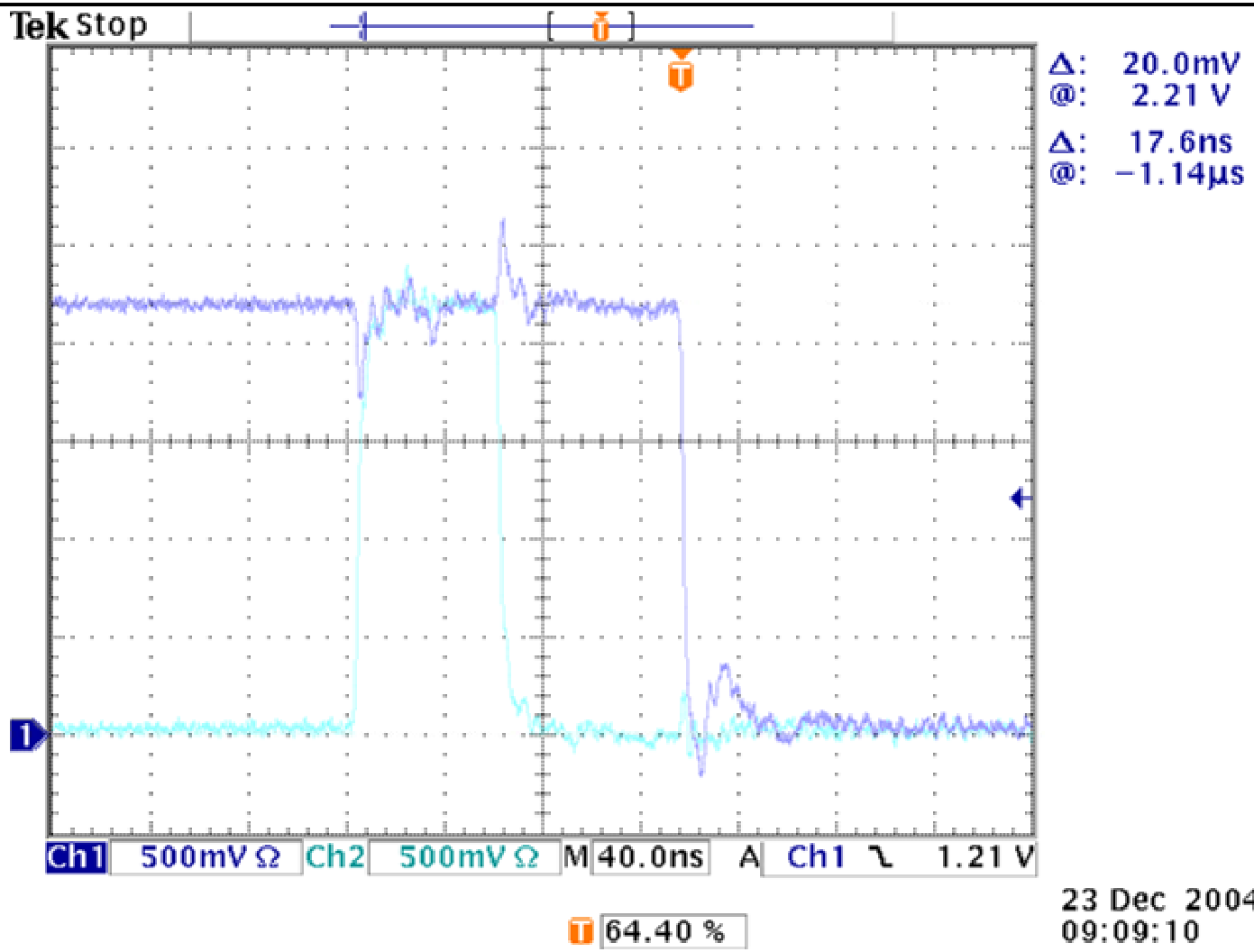
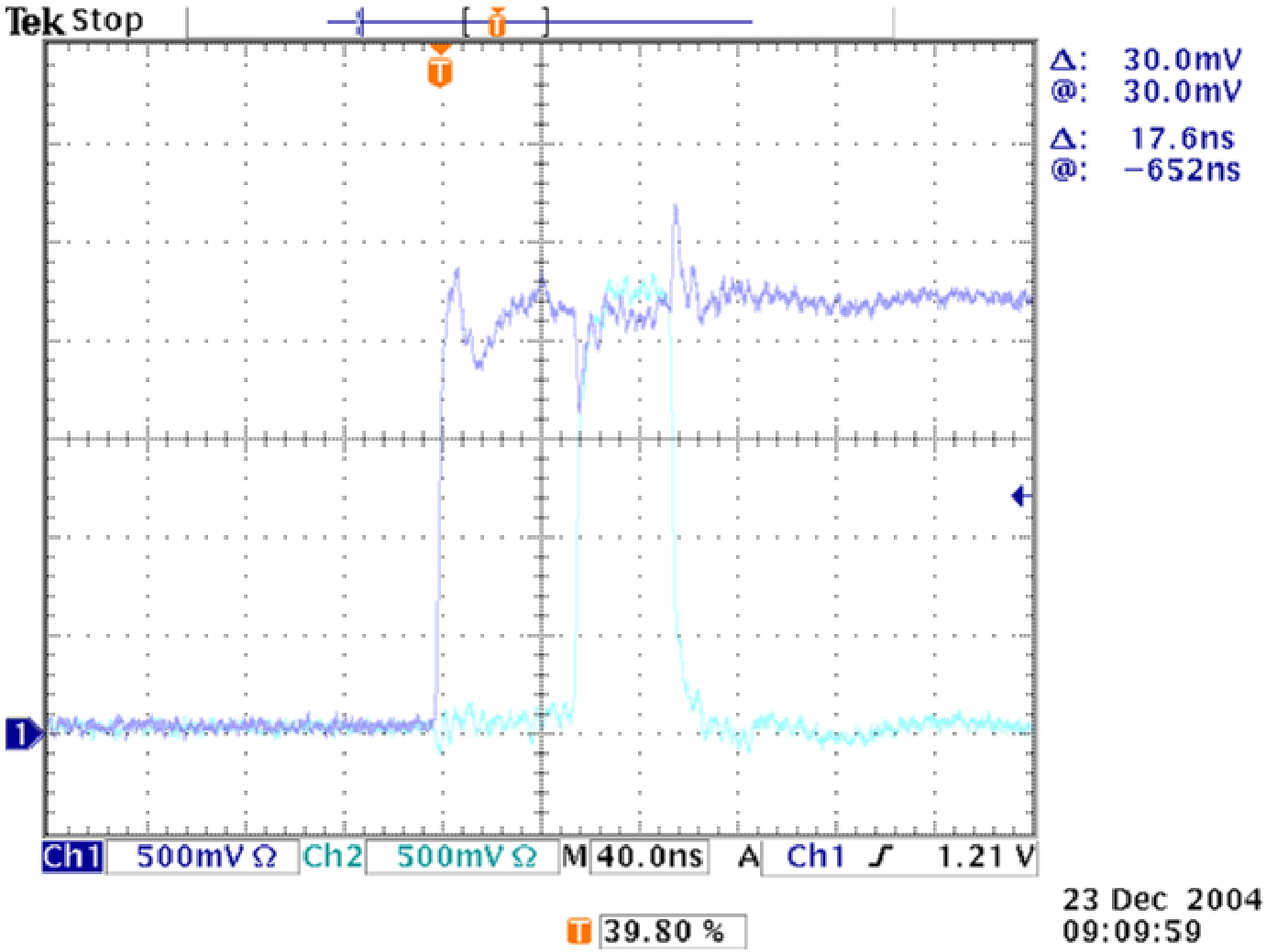
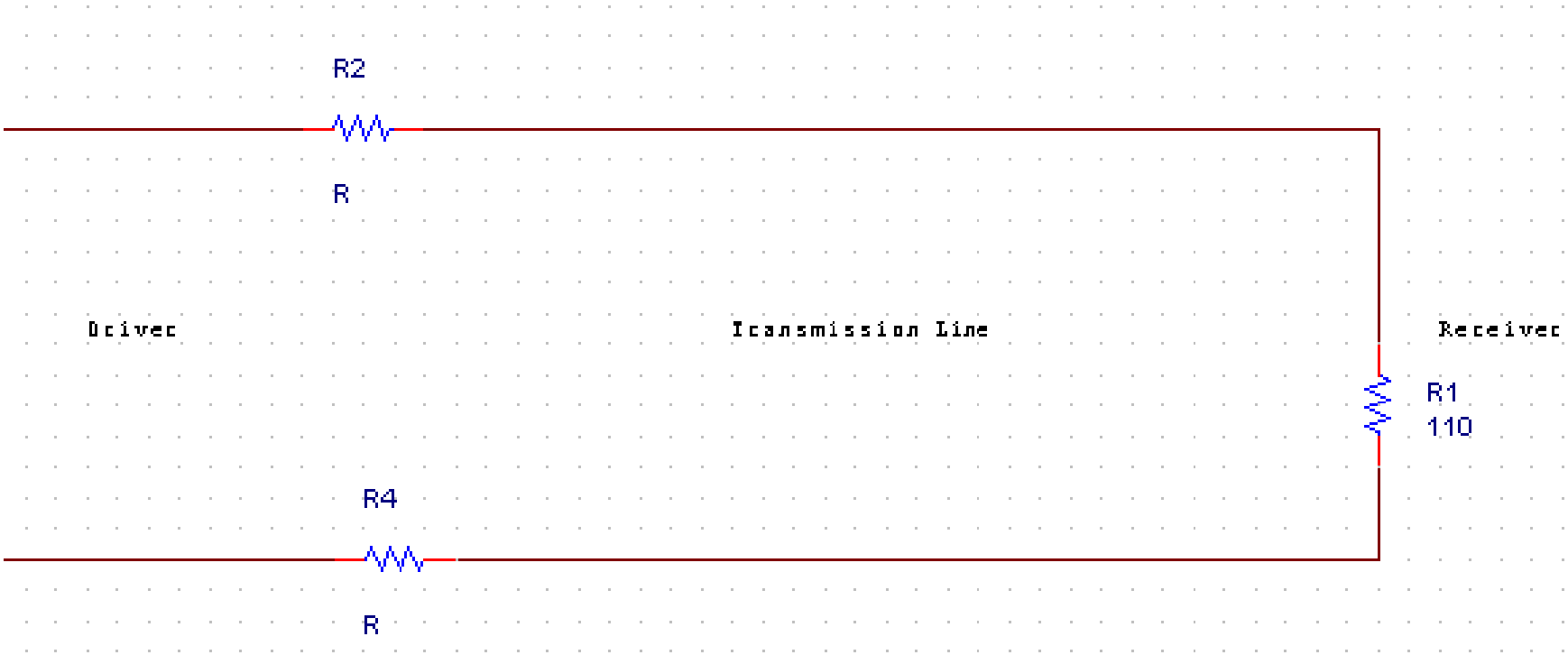
Channel 1 is Priority In, Channel 2 is Change Mode at the hybrid.



Channel 1 is Priority In (rising edge), channel 2 is change mode at the hybrid.



Clock signal attenuation circuit.



Electronics
Design
Laboratory

- A circuit was built with 1k ohm potentiometers for the R values.
- Circuit refreshed signals with the same driver as on the adapter card, but has the ground referenced to the hybrid (as proposed for the next adapter card revision).

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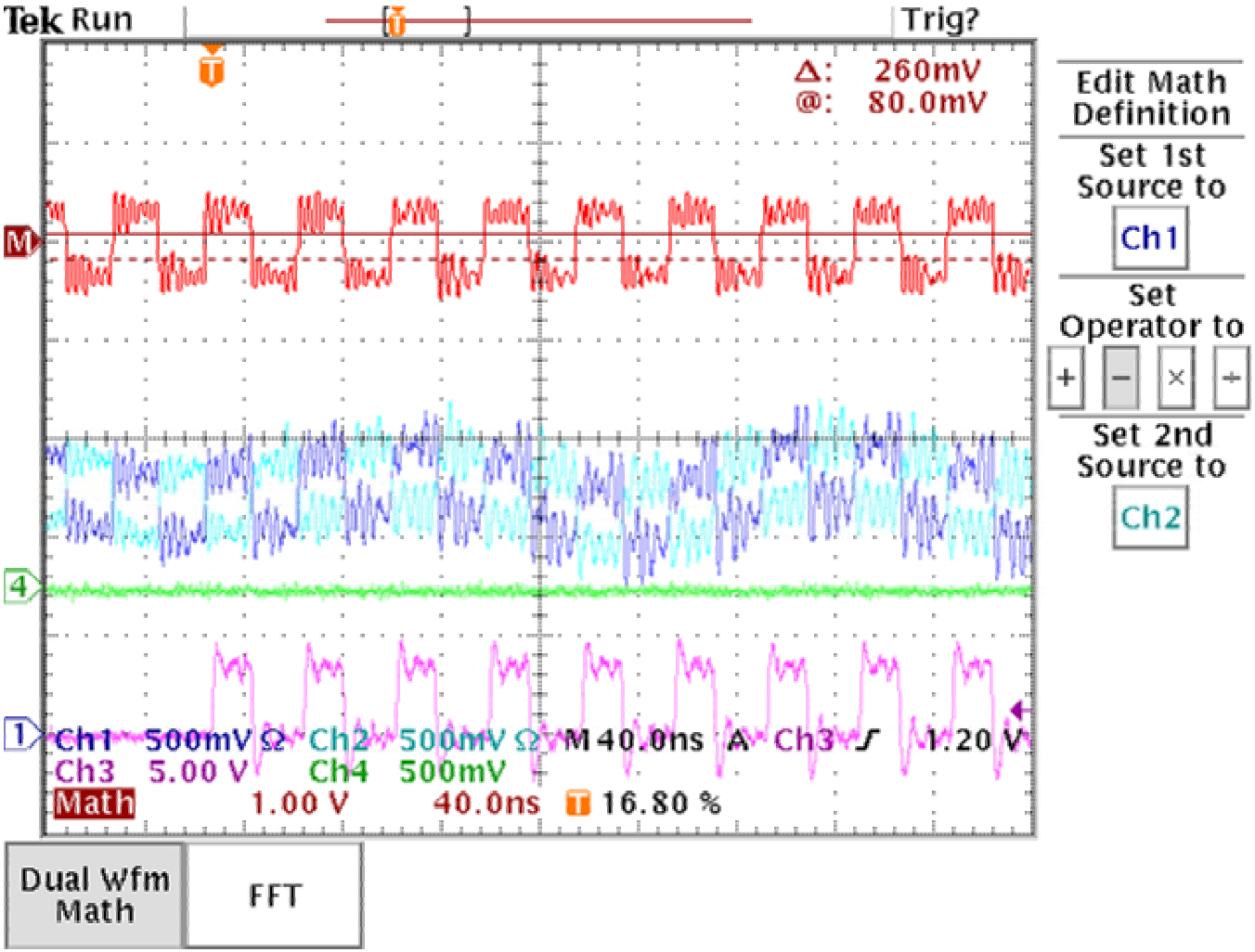
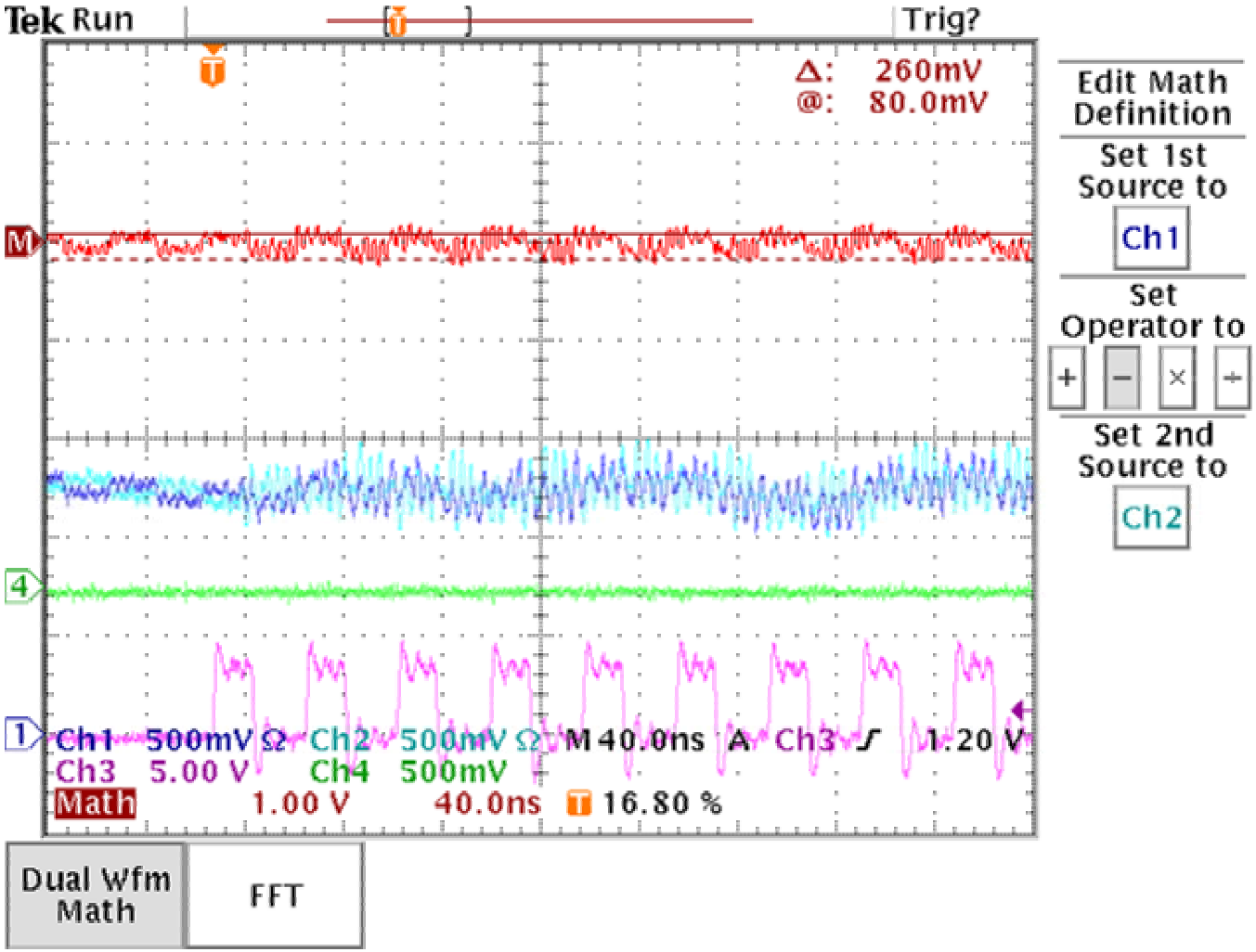
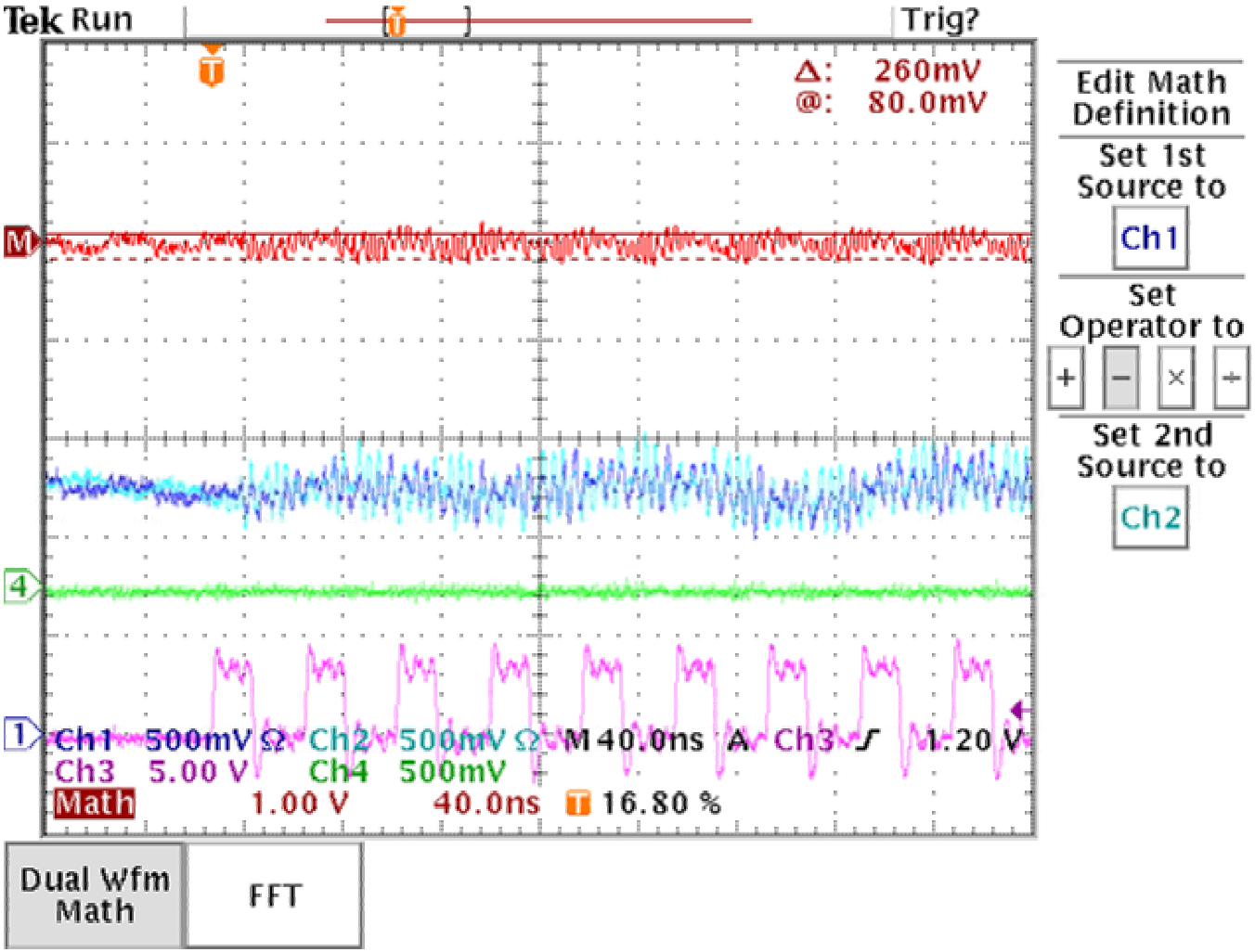
Clock amplitude test, no attenuation (R = 0). Channel 3 is Data Valid at the interface board.



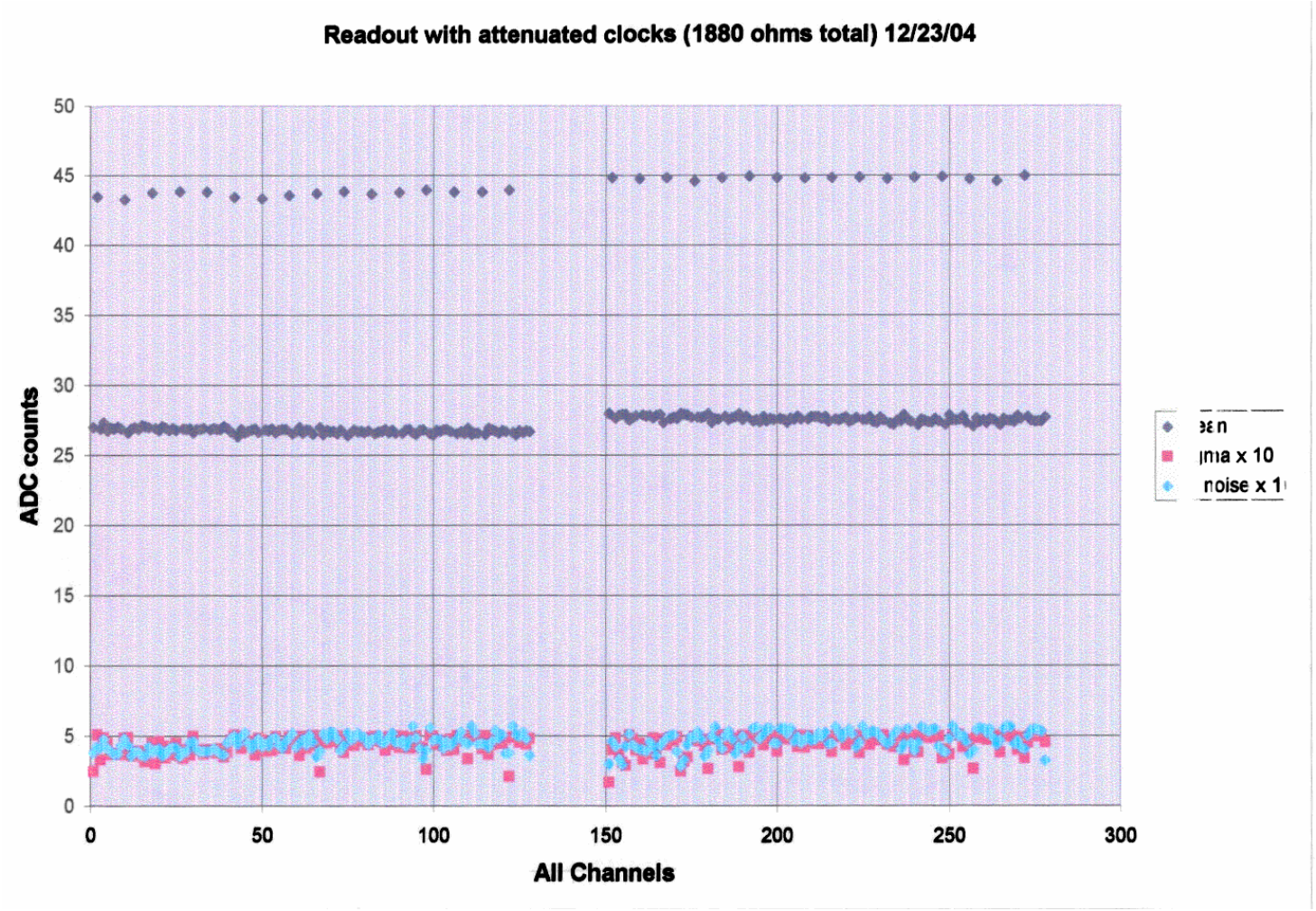
R = 550 ohms. Channel 3 is Data Valid at the interface board.



R = 940 ohms. Channel 3 is Data Valid at the interface board.



Readout with R = 940 ohms.



Electronics Design Laboratory

Conclusion.

- In setting the clock attenuation, we must be conservative enough to account for part to part variations in both the driver an the SVX IV receiver circuits.

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