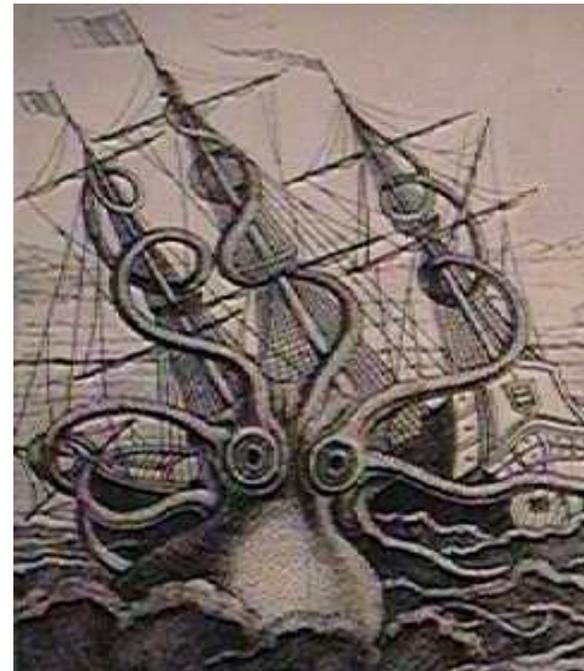




Run2b Datapath 17 Dec Update

Bill Reay, Ron Sidwell, Noel Stanton,
Russell Taylor, Kansas State University



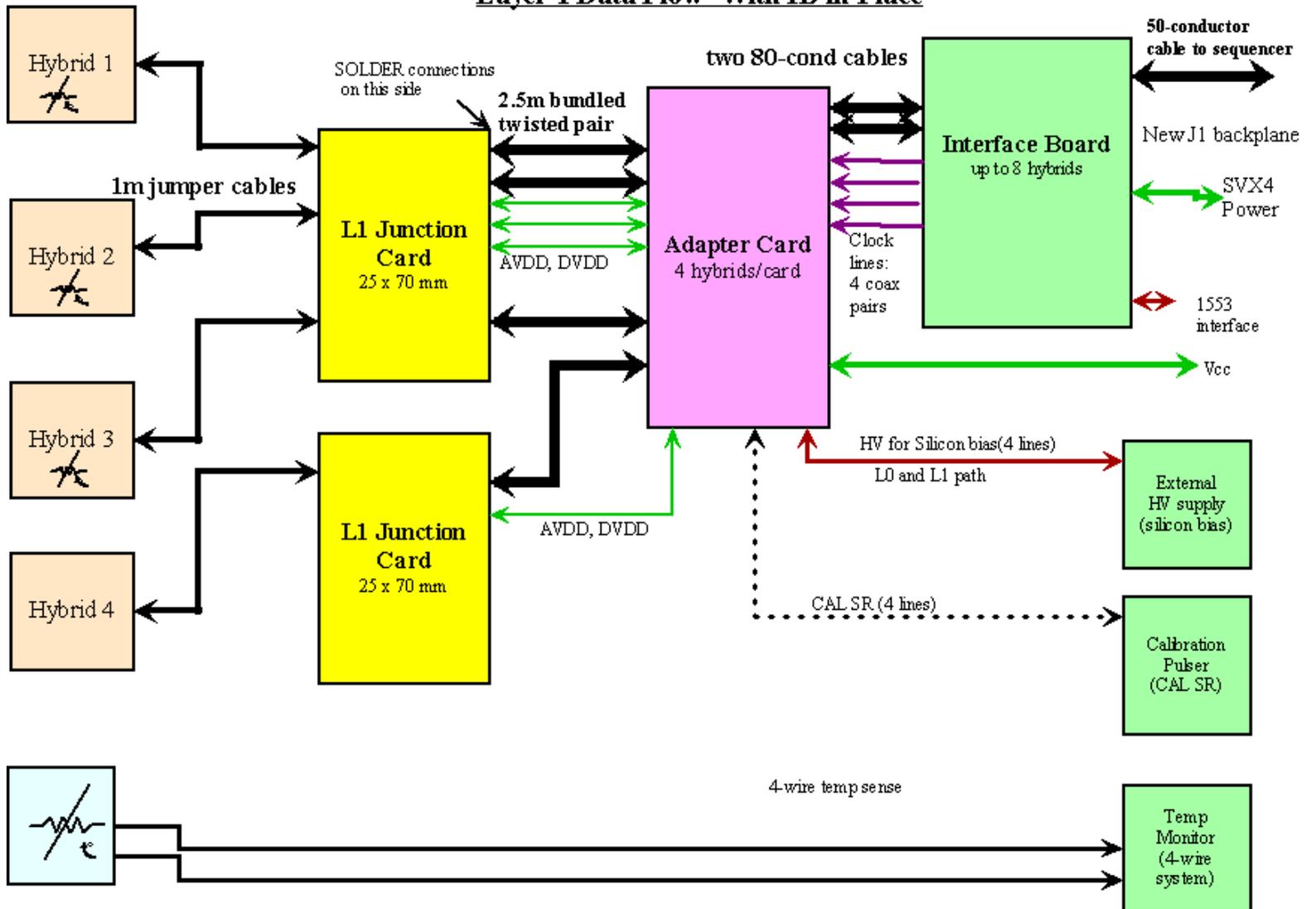


Overall Layout



11/16/01

Layer 1 Data Flow- With IB in Place



12/17/01

Ron Sidwell



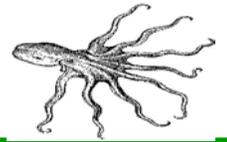
Proposed Baseline(1)



- New adapter card (AC), with 4 hybrid channels per card. 2 X 37 X 3 cards at ends of calorimeter (222 total), one design for **all** silicon layers.
- Need adapter card pairs as in run2a, but **ONLY** for L0, L1. The 2nd card is just a HV pass-thru with LEMO connectors.
- Keep IB for vital functions of clock shaping and PECL conversion, terminations (both ways) for single ended lines), and dvalid shaping and delay.
- SVX4 power will be routed thru the IB, as in Run 2a.



Proposed Baseline(2)



- AVDD and DVDD are each regulated at the AC.
- Run the AC voltage (3.3v) directly to the AC, bypass the IB.
- Leave the clocks and clock cables as is. We know the present signal levels and cables do not perturb the calorimeter.
- Build a new J1 backplane for interface crates to allow simpler power fanout (bussed across multiple slots). Need to supply 4 voltages: AVDD, DVDD, and +15v and +5v for IB. Could combine AVDD and DVDD at this end.
- Leave HV on backplane, but only 8 lines instead of 16 (this path only works for L2-5).
- Retain 1553 connector.



Junction Card Status



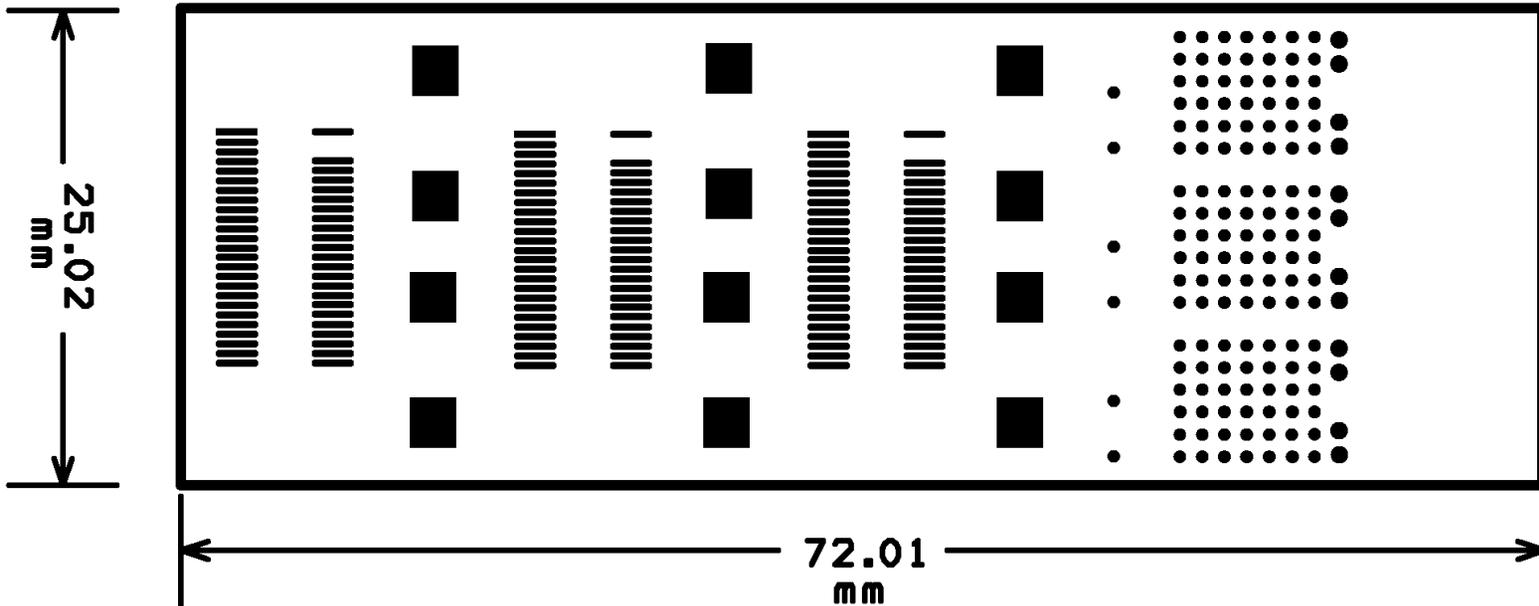
- Minor changes have been made in the conceptual layout (1 mm longer).
- Routing is in progress, expect ORCAD layout by 14 Jan.
- L2-L5 routing should be done by 2/15.
- PO target date- if vendor selected by 3/26/02- first articles by May.
- L0 schedule will trail by ~6 weeks.
- **Critical path item** is soldering of small wires into small holes. Propose to build proto board so FNAL techs can practice with twisted pair samples. Will have pads and holes only (no routing!).
- Need to understand location in experiment, size constraints, and mounting! DRAWINGS!



L1 Junction Card Pads



L1 Junction Card





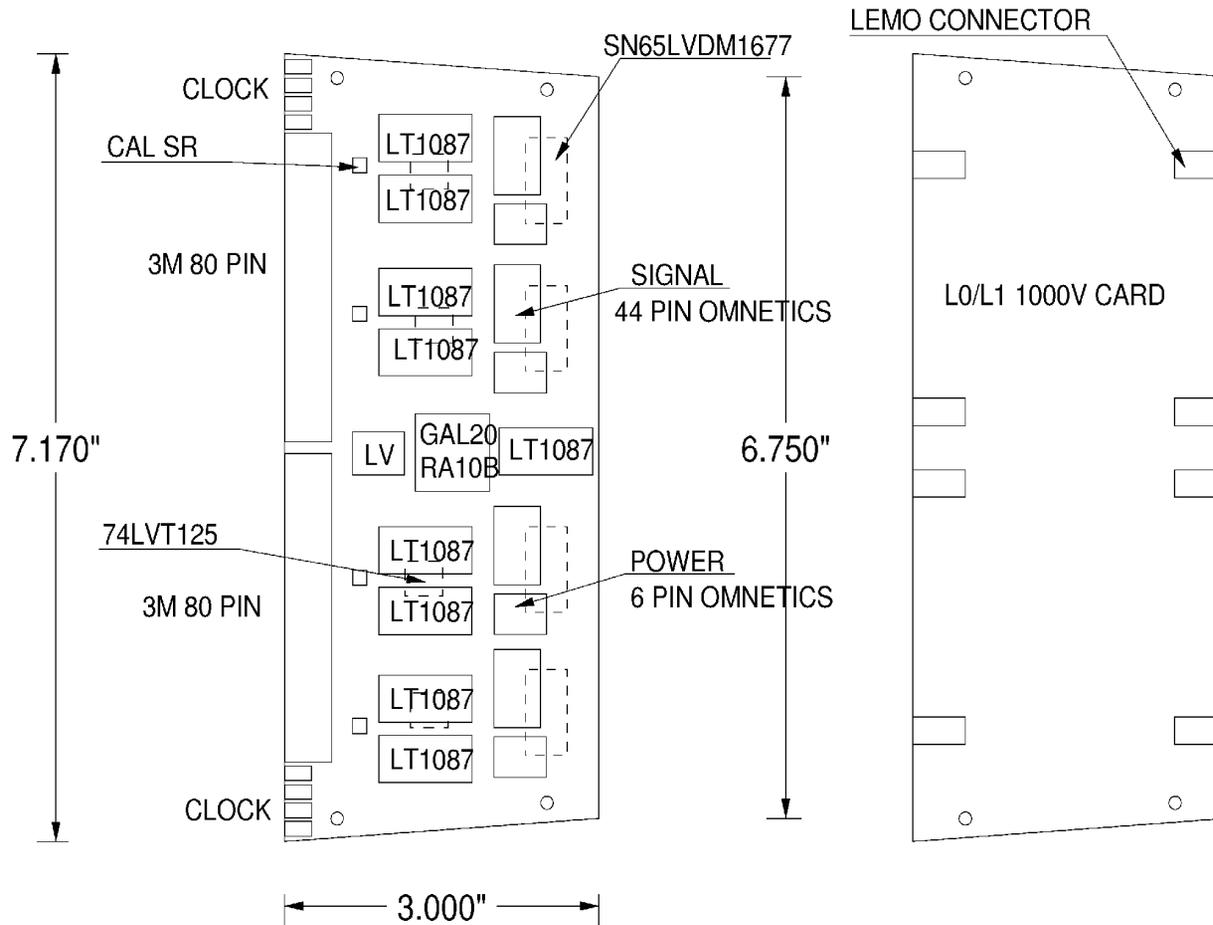
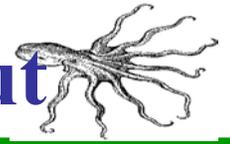
Adapter Card Status



- In LV regulation tests, we still see a 170mV spike when loads are switched. Will try some high value ceramic caps at the JC location next. Also trying to get samples of a surface-mount regulator from ON semiconductor, which has 3A output, and only <math><0.6\text{v}</math> drop, and a control signal. Need \$3K to buy a minimum order of 1500. Maybe CDF interested? Would cut heat load in half.
- Power connector needs to be fixed: propose (for 4-channel design) four 6-pin Omnetics type, with HV for L2-L5 using two of these pins, and SVX4 power the other four.
- HV for L0, L1: use a path independent of the adapter card. Use two-board design for these sensors, due to keep clear space needed at 1KV.

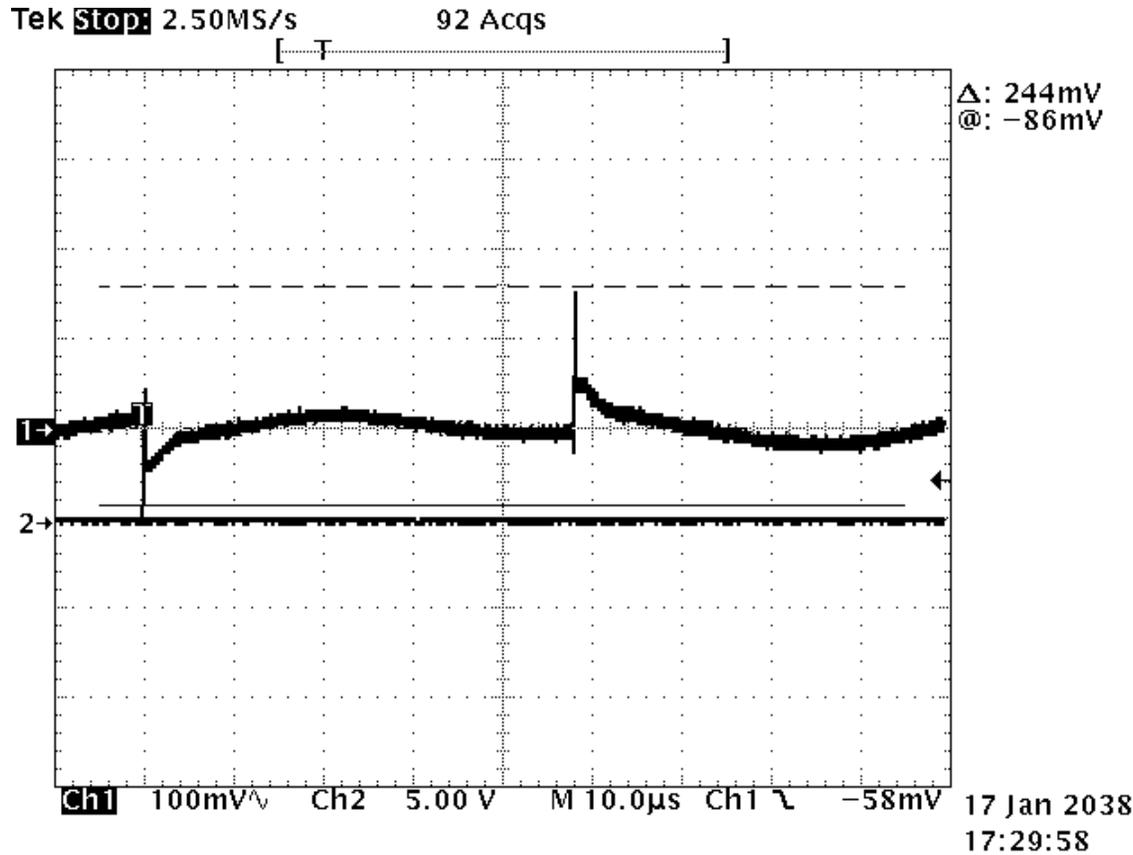
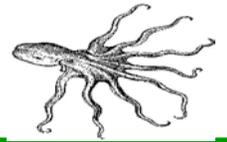


Revised Adapter Card 4-chan Layout





LV regulation so far (R. Taylor)



Current sense
scheme,
LT1087
regulator. Spike
is 244mV p-p.
Need another
factor of ~2 for
safety I think.

Work in
progress-
different caps,
ON regulator.



Purple card (for test stands)



- Cecilia has asked for 75 two-channel cards for the test stands. These would be similar in function to the new adapter card, but with different input and output connectors: 50-conductor cable in from SASEQ; and probably jumper cable out.
- This week- try to establish specification. Do we need to supply analog out for temperature for instance.
- Do we need a staging card (connector adapter module)? Probably, but this costs another \$50K including the cables.