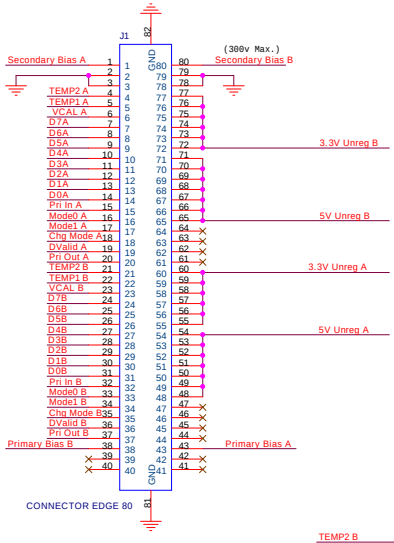
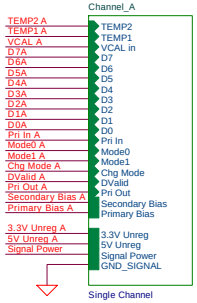
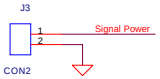
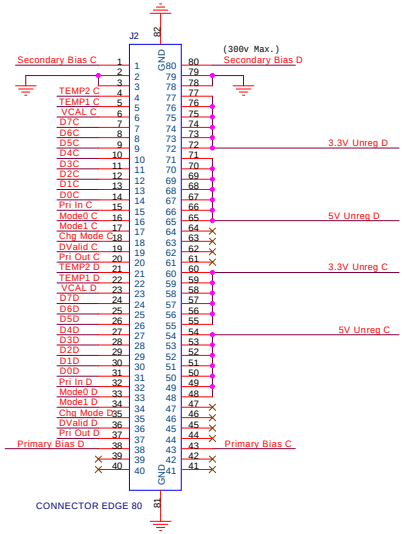
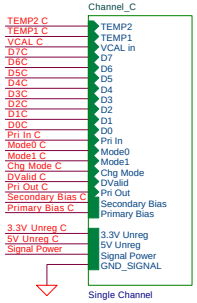




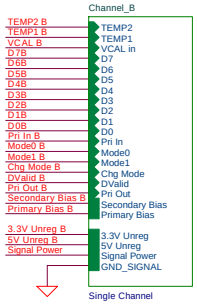


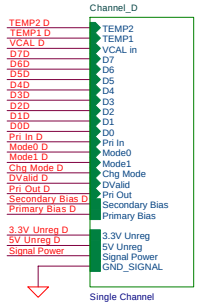
Hybrid refenced ground symbol.

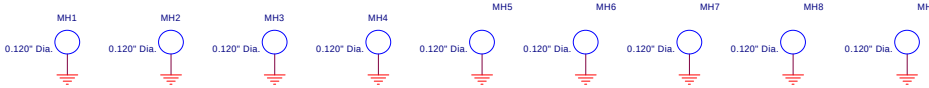




Interface board referenced ground symbol.







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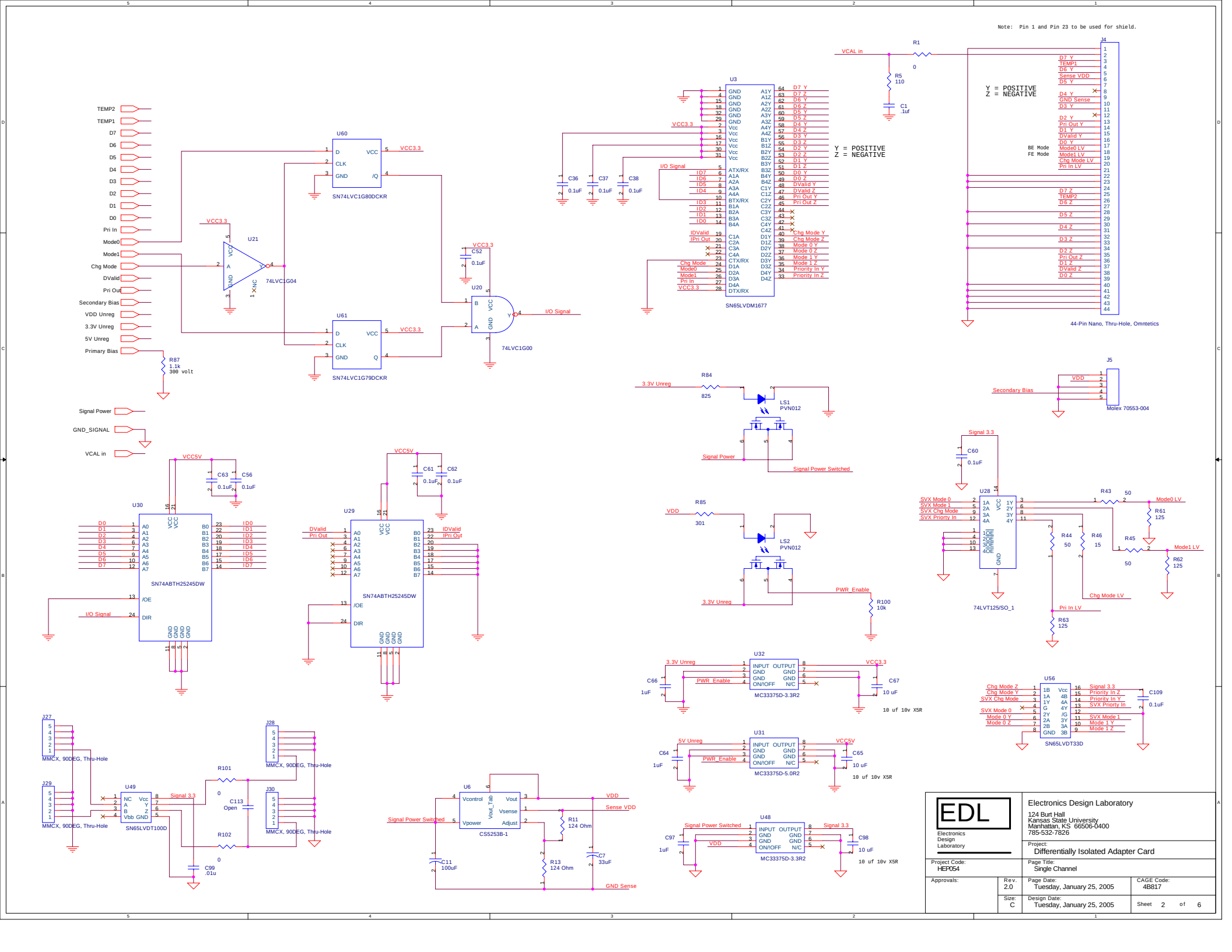
		Project: Differentially Isolated Adapter Card	
Project Code: HEP054		Page Title: 4-Channel	
Approvals:	Rev. 2.0	Page Date: Monday, January 24, 2005	CAGE Code: 4B817
	Size: C	Design Date: Monday, January 24, 2005	Sheet 1 of 6


Note: Pin 1 and Pin 23 to be used for shield.
TEMP2
TEMP1
D7
D6
D5
D4
D3
D2
D1
D0
Pri In
Mode0
Mode1
Chg Mode
DValid
Pri Out
Secondary Bias
VDD Unreg
3.3V Unreg
5V Unreg
Primary Bias
R87
1.1k
300 volt
Signal Power
GND_SIGNAL
VCAL in
U60
SN74LVC1G80DCKR
U61
SN74LVC1G79DCKR
U21
74LVC1G04
U20
74LVC1G00
VCC3.3
I/O Signal
U3
SN65LVDM1677
Y = POSITIVE
Z = NEGATIVE
C36
C37
C38
0.1uF
C52
R1
R5
110
C1
.1uf
J4
44-Pin Nano, Thru-Hole, Omntetics
BE Mode
FE Mode
J5
Molex 70553-004
R84
825
LS1
PVN012
Signal Power Switched
R85
301
LS2
PVN012
PWR_Enable
R100
10k
U30
SN74ABTH25245DW
U29
SN74ABTH25245DW
VCC5V
C63
C56
C61
C62
U28
74LVT125/SO_1
R43
R44
R46
R45
R61
R62
R63
125
Mode0 LV
Mode1 LV
Chg Mode LV
Pri In LV
U32
MC33375D-3.3R2
C66
C67
10 uF
10 uf 10v X5R
U31
MC33375D-5.0R2
C64
C65
U56
SN65LVDT33D
C109
J27
J28
J29
J30
MMCX, 90DEG, Thru-Hole
U49
SN65LVDT100D
R101
R102
C113
Open
C99
.01u
U6
CS5253B-1
R11
124 Ohm
R13
124 Ohm
C11
100uF
C7
33uF
U48
MC33375D-3.3R2
C97
C98
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Project:
Differentially Isolated Adapter Card
Project Code:
HEP054
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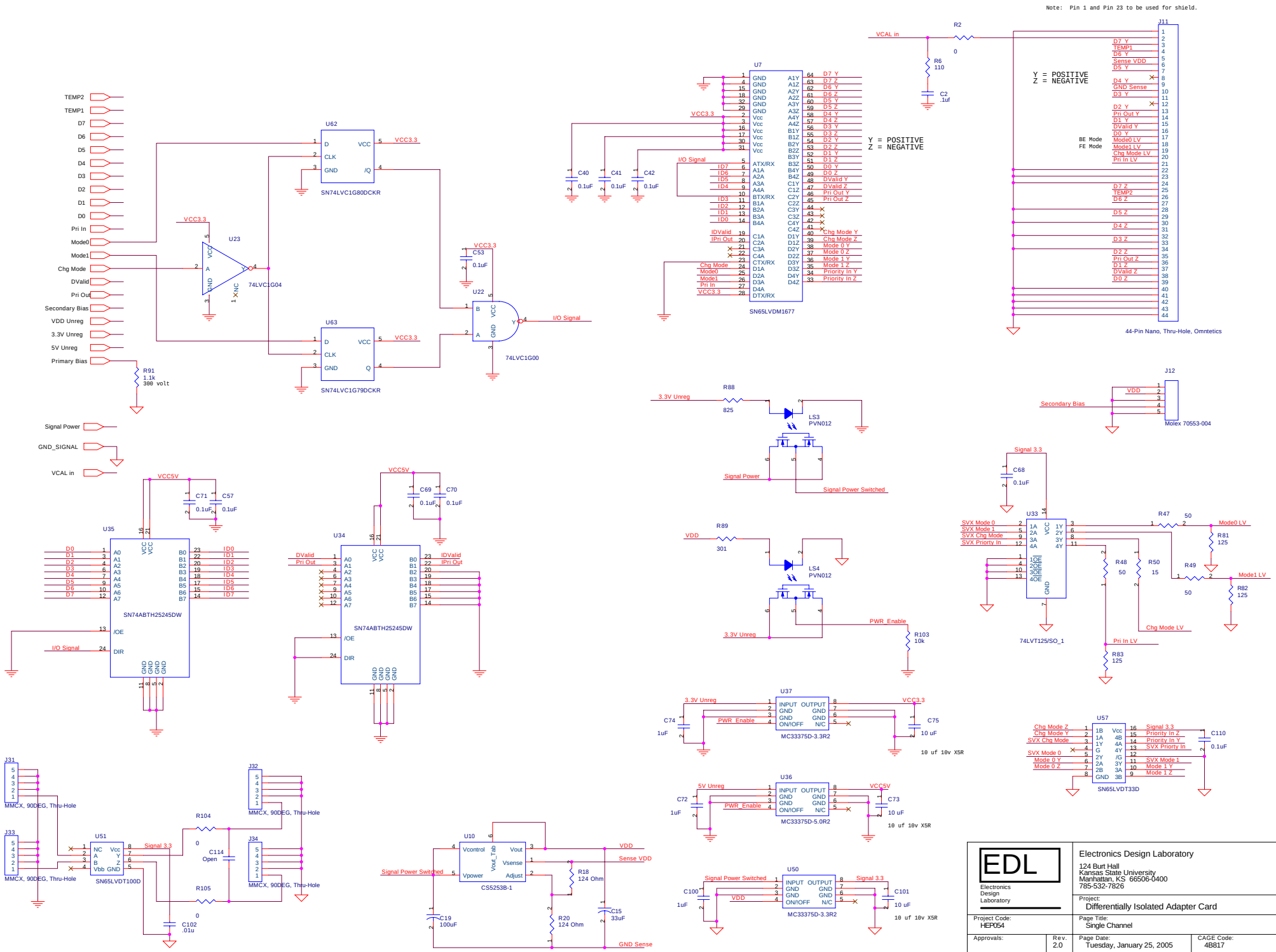
Single Channel
Approvals:
Rev.
2.0
Page Date:
Tuesday, January 25, 2005
CAGE Code:
4B817
Size:
C
Design Date:
Tuesday, January 25, 2005
Sheet 2 of 6


Note: Pin 1 and Pin 23 to be used for shield.
U7
SN65LVDM1677
Y = POSITIVE
Z = NEGATIVE
J11
44-Pin Nano, Thru-Hole, Omntetics
VCAL in
R2
0
R6
110
C2
.1uf
U62
SN74LVC1G80DCKR
U63
SN74LVC1G79DCKR
U23
74LVC1G04
U22
74LVC1G00
C53
0.1uF
C40
0.1uF
C41
0.1uF
C42
0.1uF
R91
1.1k
300 volt
Signal Power
GND_SIGNAL
VCAL in
J12
Molex 70553-004
Secondary Bias
R88
825
LS3
PVN012
Signal Power
Signal Power Switched
R89
301
LS4
PVN012
PWR_Enable
R103
10k
U35
SN74ABTH25245DW
U34
SN74ABTH25245DW
C71
0.1uF
C57
0.1uF
C69
0.1uF
C70
0.1uF
U33
74LVT125/SO_1
R47
50
R48
50
R50
15
R49
50
R81
125
R82
125
R83
125
C68
0.1uF
U37
MC33375D-3.3R2
C74
1uF
C75
10 uF
10 uf 10v X5R
U36
MC33375D-5.0R2
C72
1uF
C73
10 uF
10 uf 10v X5R
U57
SN65LVDT33D
C110
0.1uF
J31
MMCX, 90DEG, Thru-Hole
J32
MMCX, 90DEG, Thru-Hole
J33
MMCX, 90DEG, Thru-Hole
J34
MMCX, 90DEG, Thru-Hole
U51
SN65LVDT100D
R104
0
R105
0
C114
Open
C102
.01u
U10
CS5253B-1
R18
124 Ohm
R20
124 Ohm
C19
100uF
C15
33uF
U50
MC33375D-3.3R2
C100
1uF
C101
10 uF
10 uf 10v X5R
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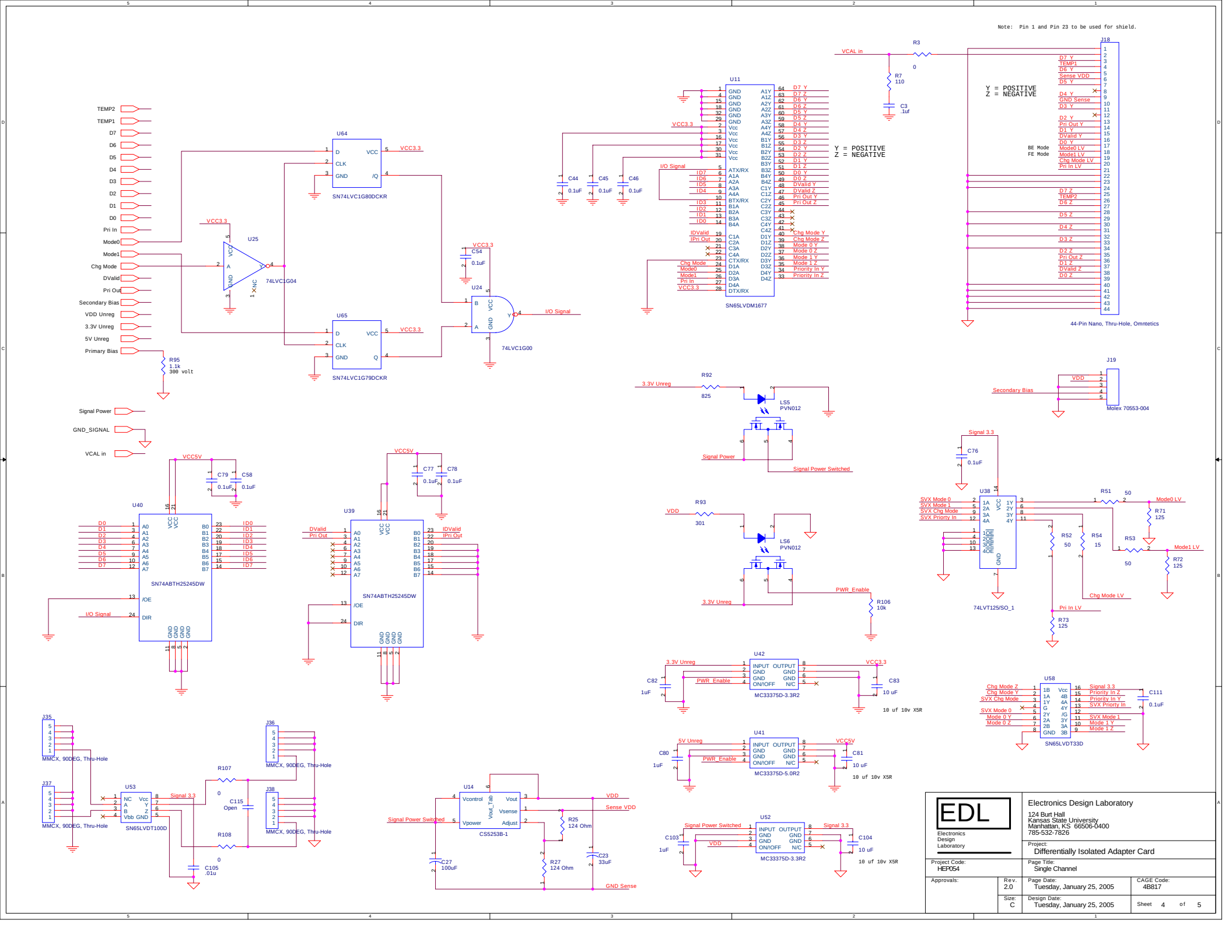
Project: Differentially Isolated Adapter Card
Project Code: HEP054
Page Title: Single Channel
Approvals:
Rev. 2.0
Page Date: Tuesday, January 25, 2005
CAGE Code: 4B817
Size: C
Design Date: Tuesday, January 25, 2005
Sheet 3 of 5


Note: Pin 1 and Pin 23 to be used for shield.
TEMP2
TEMP1
D7
D6
D5
D4
D3
D2
D1
D0
Pri In
Mode0
Mode1
Chg Mode
DValid
Pri Out
Secondary Bias
VDD Unreg
3.3V Unreg
5V Unreg
Primary Bias
R95
1.1k
300 volt
U64
SN74LVC1G80DCKR
U65
SN74LVC1G79DCKR
U25
74LVC1G04
U24
74LVC1G00
VCC3.3
C54
0.1uF
I/O Signal
U11
SN65LVDM1677
Y = POSITIVE
Z = NEGATIVE
C44
C45
C46
0.1uF
VCAL in
R3
0
R7
110
C3
.1uf
J18
44-Pin Nano, Thru-Hole, Omntetics
BE Mode
FE Mode
Signal Power
GND_SIGNAL
VCAL in
R92
825
LS5
PVN012
Signal Power
Signal Power Switched
J19
Molex 70553-004
VDD
Secondary Bias
VCC5V
C79
C58
0.1uF
U40
SN74ABTH25245DW
I/O Signal
C77
C78
U39
DValid
Pri Out
IDValid
IPri Out
R93
301
LS6
PVN012
PWR_Enable
3.3V Unreg
R106
10k
Signal 3.3
C76
U38
74LVT125/SO_1
SVX Mode 0
SVX Mode 1
SVX Chg Mode
SVX Priorty In
R51
50
R52
50
R54
15
R53
50
R71
125
R72
125
R73
125
Mode0 LV
Mode1 LV
Chg Mode LV
Pri In LV
U42
MC33375D-3.3R2
C82
1uF
C83
10 uF
10 uf 10v X5R
U41
MC33375D-5.0R2
5V Unreg
C80
1uF
C81
10 uF
10 uf 10v X5R
U52
MC33375D-3.3R2
Signal Power Switched
C103
1uF
C104
10 uF
10 uf 10v X5R
U58
SN65LVDT33D
Chg Mode Z
Chg Mode Y
SVX Chg Mode
SVX Mode 0
Mode 0 Y
Mode 0 Z
Signal 3.3
Priority In Z
Priority In Y
SVX Priorty In
SVX Mode 1
Mode 1 Y
Mode 1 Z
C111
0.1uF
J35
MMCX, 90DEG, Thru-Hole
J37
MMCX, 90DEG, Thru-Hole
U53
SN65LVDT100D
Signal 3.3
R107
0
R108
0
C115
Open
C105
.01u
J36
MMCX, 90DEG, Thru-Hole
J38
MMCX, 90DEG, Thru-Hole
U14
CS5253B-1
Signal Power Switched
VDD
Sense VDD
R25
124 Ohm
R27
124 Ohm
C27
100uF
C23
33uF
GND Sense
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Project:
Differentially Isolated Adapter Card
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Approvals:
Rev.
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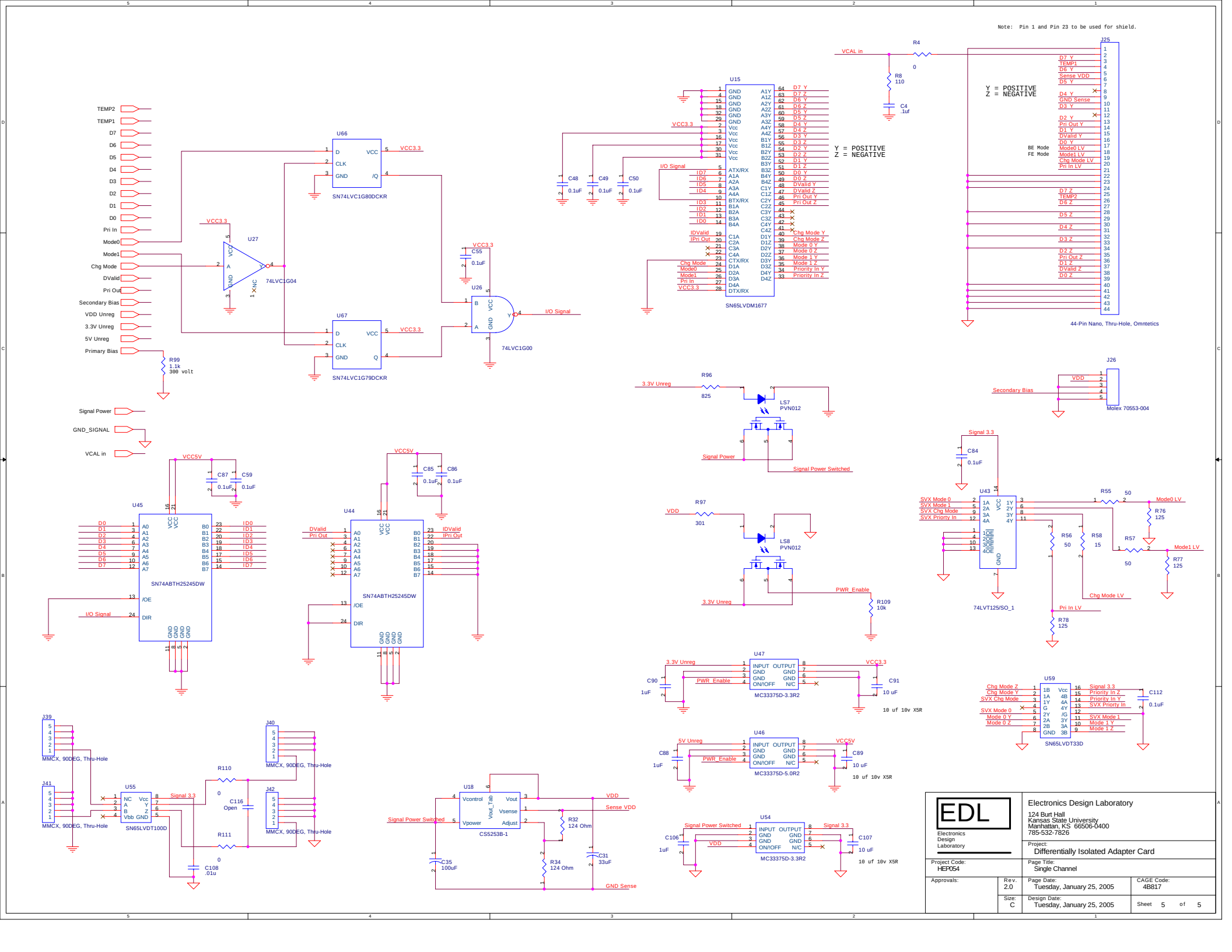
CAGE Code:
4B817
Size:
C
Design Date:
Tuesday, January 25, 2005
Sheet 4 of 5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TEMP1
D7
D6
D5
D4
D3
D2
D1
D0
Pri In
Mode0
Mode1
Chg Mode
DValid
Pri Out
Secondary Bias
VDD Unreg
3.3V Unreg
5V Unreg
Primary Bias
R99
1.1k
300 volt
Signal Power
GND_SIGNAL
VCAL in
U66
SN74LVC1G80DCKR
U67
SN74LVC1G79DCKR
U27
74LVC1G04
U26
74LVC1G00
VCC3.3
I/O Signal
U15
SN65LVDM1677
C48
C49
C50
0.1uF
C55
0.1uF
R4
0
R8
110
C4
.1uf
J25
Y = POSITIVE
Z = NEGATIVE
BE Mode
FE Mode
44-Pin Nano, Thru-Hole, Omntetics
J26
Molex 70553-004
R96
825
LS7
PVN012
Signal Power
Signal Power Switched
R97
301
LS8
PVN012
PWR_Enable
R109
10k
U45
SN74ABTH25245DW
U44
SN74ABTH25245DW
VCC5V
C87
C59
C85
C86
0.1uF
U43
74LVT125/SO_1
C84
0.1uF
R55
50
R56
50
R58
15
R57
50
R76
125
R77
125
R78
125
Mode0 LV
Mode1 LV
Chg Mode LV
Pri In LV
U47
MC33375D-3.3R2
C90
1uF
C91
10 uF
10 uf 10v X5R
U46
MC33375D-5.0R2
C88
1uF
C89
10 uF
10 uf 10v X5R
U59
SN65LVDT33D
C112
0.1uF
J39
J40
J41
J42
MMCX, 90DEG, Thru-Hole
U55
SN65LVDT100D
R110
R111
C116
Open
C108
.01u
U18
CS5253B-1
R32
124 Ohm
R34
124 Ohm
C35
100uF
C31
33uF
U54
MC33375D-3.3R2
C106
1uF
C107
10 uF
10 uf 10v X5R
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Project:
Differentially Isolated Adapter Card
Project Code:
HEP054
Page Title:
Single Channel
Approvals:
Rev.
2.0
Page Date:
Tuesday, January 25, 2005
CAGE Code:
4B817
Size:
C
Design Date:
Tuesday, January 25, 2005
Sheet 5 of 5

Change History:

Revision 2.0:

1. Added 100 ohm resistor between interface board and SVX grounds (R9).
2. Changed Vcal termination resistor to size 2010 (1/2 W) (R5, R6, R7, R8).
3. Extended board dimensions to 7.860" x 3.820".
4. Added latching flip-flops to Mode 0 and Mode 1 lines when determining data bus direction (U60, U61, U62, U63, U64, U65, U66, U67).
5. Added 10k ohm pull down resistor to the enable line of the 5v and 3.3v interface board referenced regulators (R100, R103, R106, R109.
6. Added mounting hole between two 80 pin connectors (MH9).
7. Added clock attenuation resistors to clock lines (R101, R102, R104, R105, R107,R108, R110, R111).
8. Added parallel capacitor to clock lines (C113, C114, C115, C116).
9. Changed SVX power connector from 4 pin molex to 5 pin Molex connectors (J5, J12, J19, J26).
10. Replaced Change Mode termination resistance from 0 ohms to 15 ohms (R46, R50, R54, R58).
11. Clock repeater is now referenced to SVX ground (U49, U51, U53, U55).

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Project: Differentially Isolated Adapter Card			
Project Code: HEP054	Page Title: Change History		
Approvals:	Rev. 2.0	Page Date: Monday, January 24, 2005	CAGE Code: 4B817
	Size: C	Design Date: Monday, January 24, 2005	Sheet 6 of 6