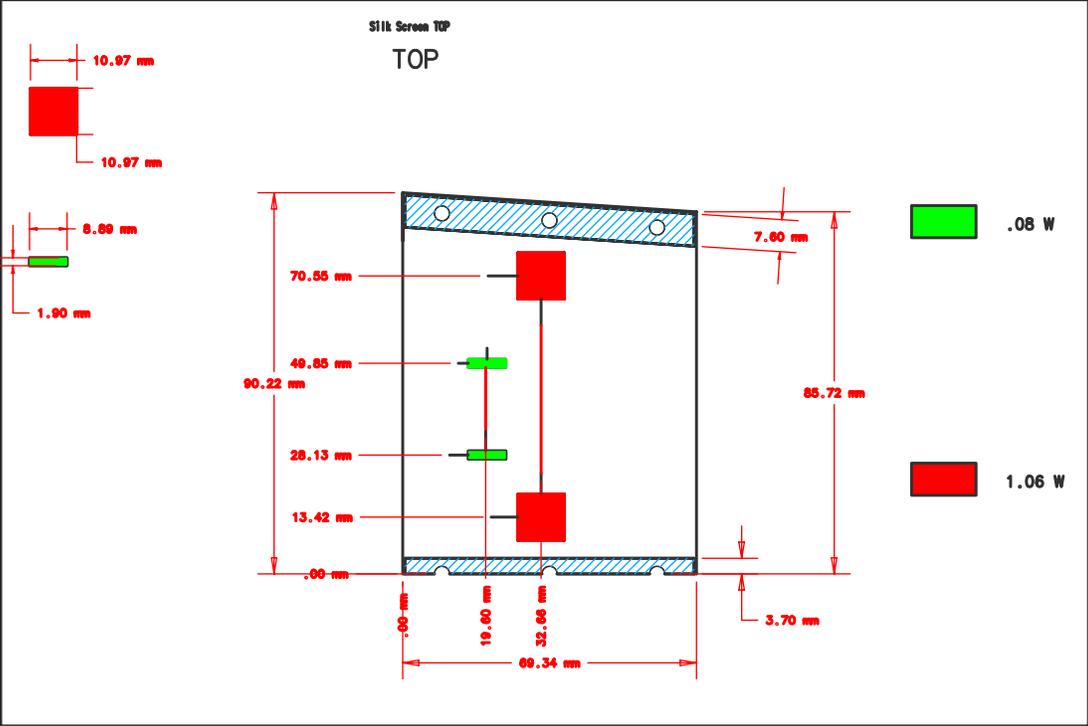
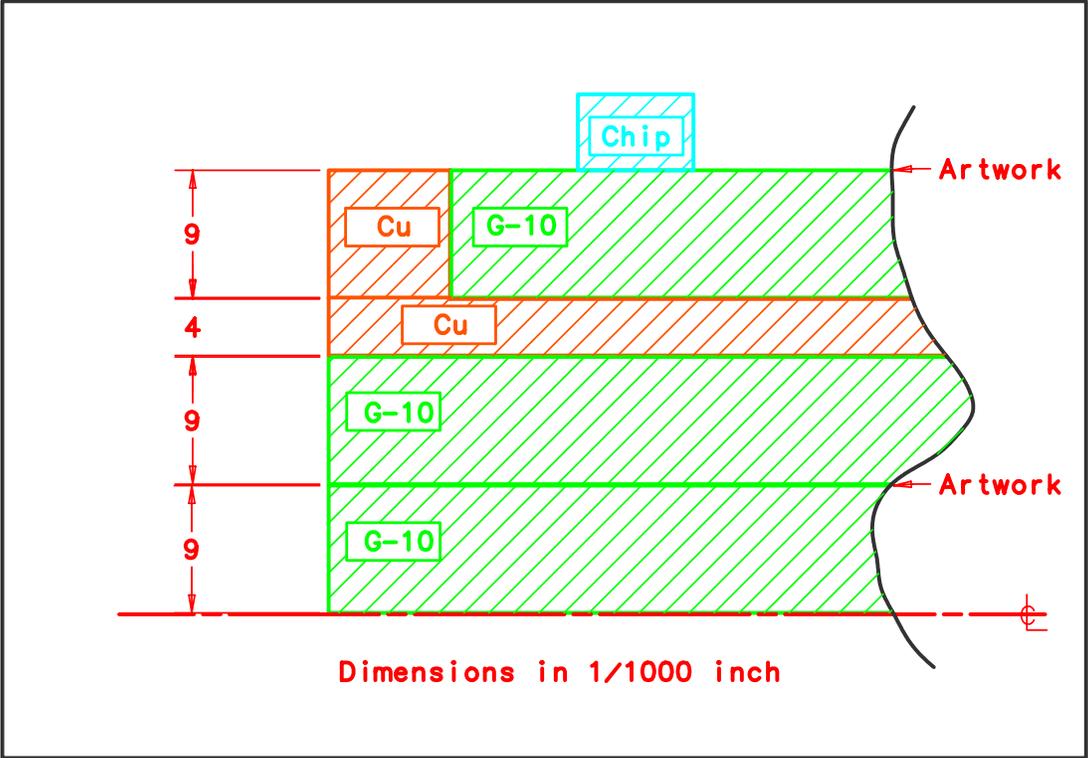
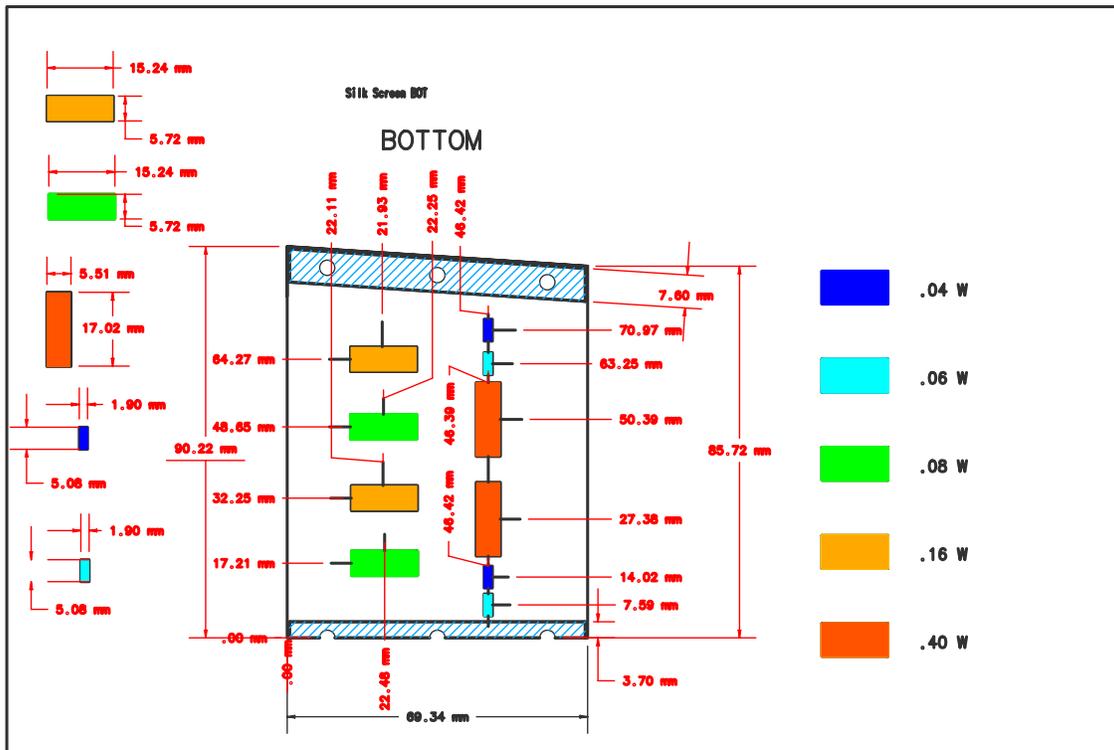


# Temperature of the Chips on Run 2b Adapter Card

FEA analysis by Ang Lee

## Geometry and Heat Sources





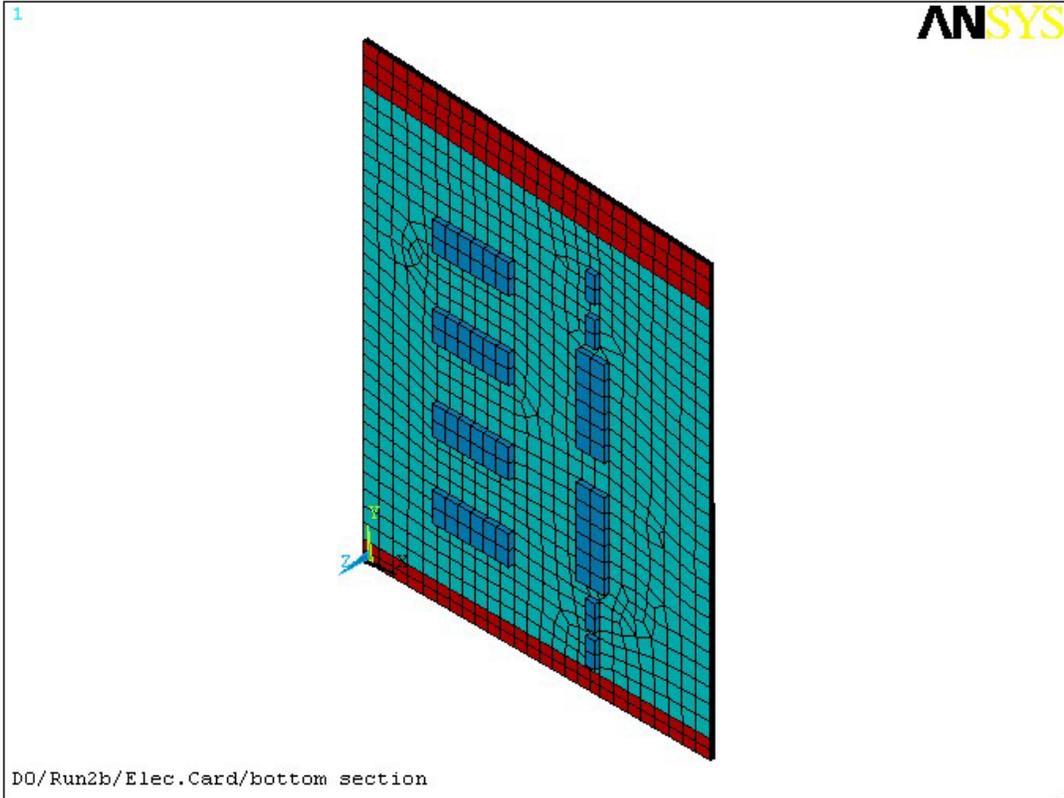
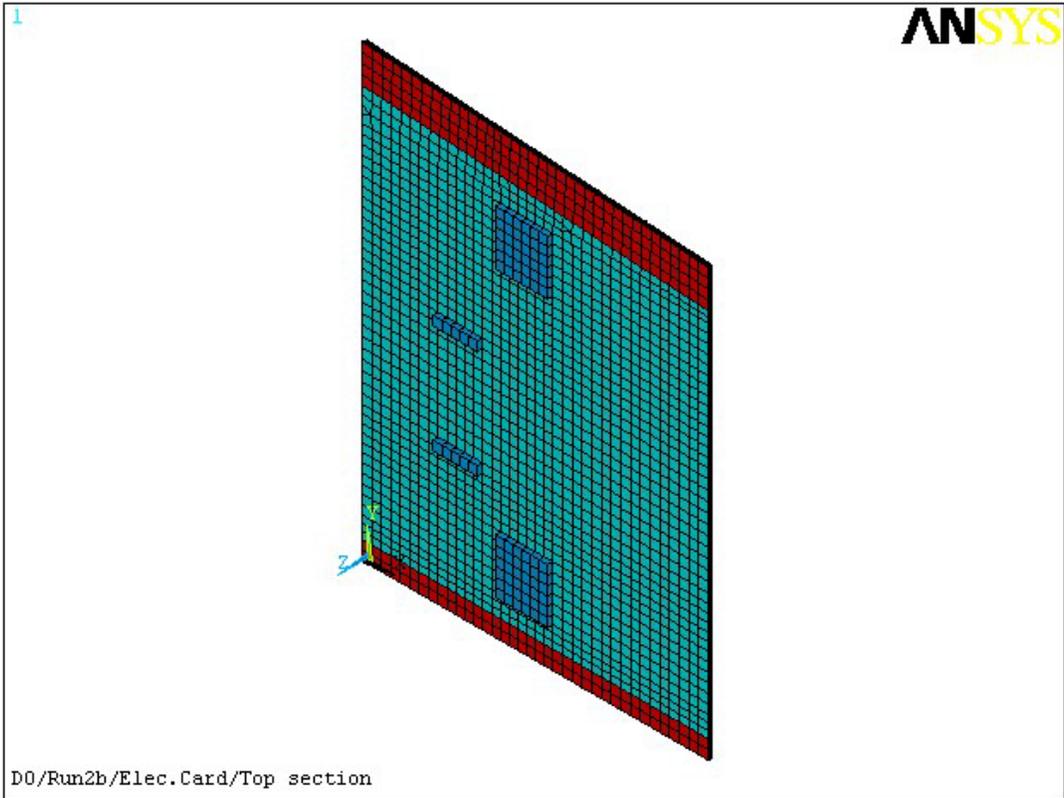
## Boundary Conditions and Properties

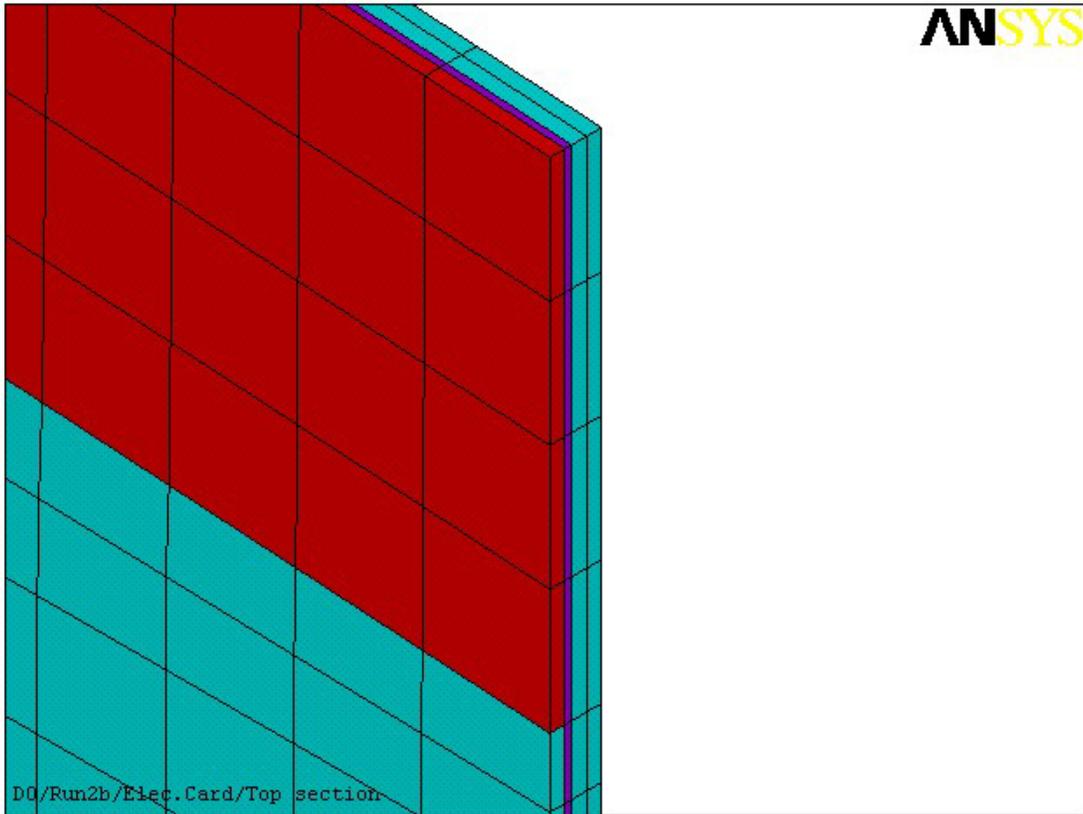
Heat sources were assumed to be in direct contact with G-10 (no air gap), and power was assumed to be uniformly distributed over each source. Top and bottom card layers were modeled independently and the regions cross-hatched in blue at the card edges and at the center were assumed to be held at 22 °C.

Only conduction (no convection or radiation) was assumed. Only the .004 in ground plane copper was used for conduction to board edges and center; copper in other trace layers was ignored. The coefficients of thermal conductivity used were:

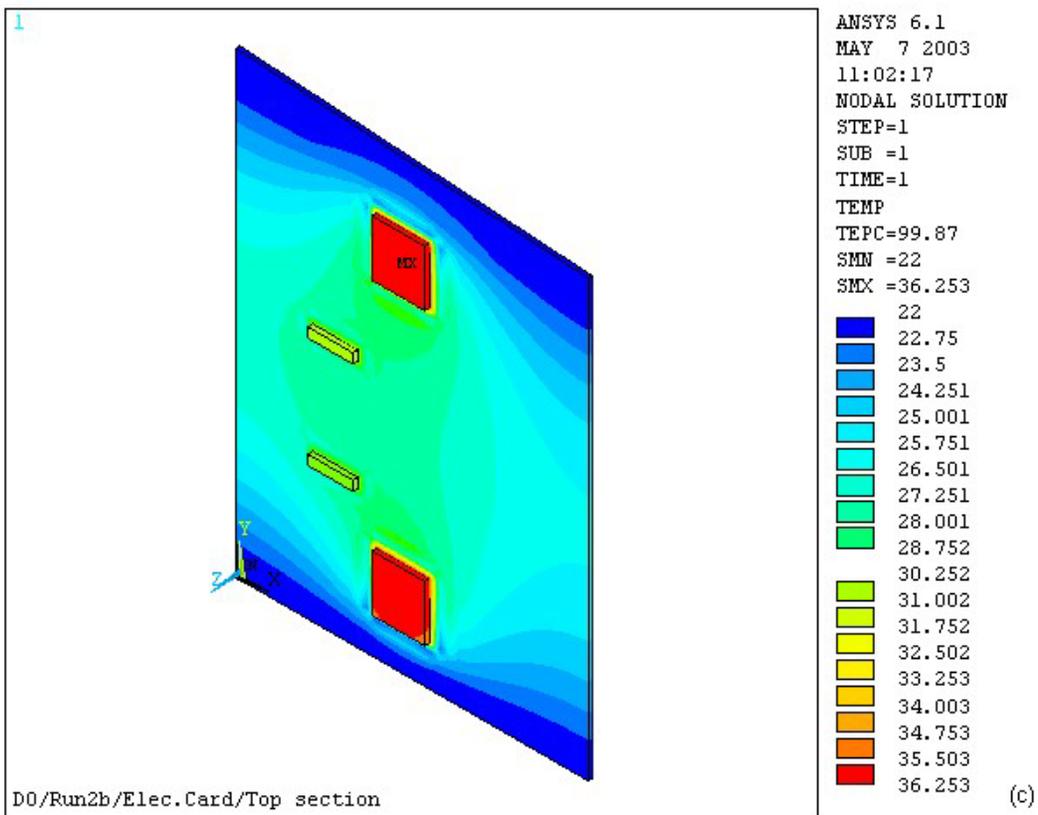
- $k_{G-10} = 0.26 \text{ W/m.}^\circ\text{C}$
- $k_{Cu} = 400 \text{ W/m.}^\circ\text{C}$
- $k_{Chips} = 140 \text{ W/m.}^\circ\text{C}$

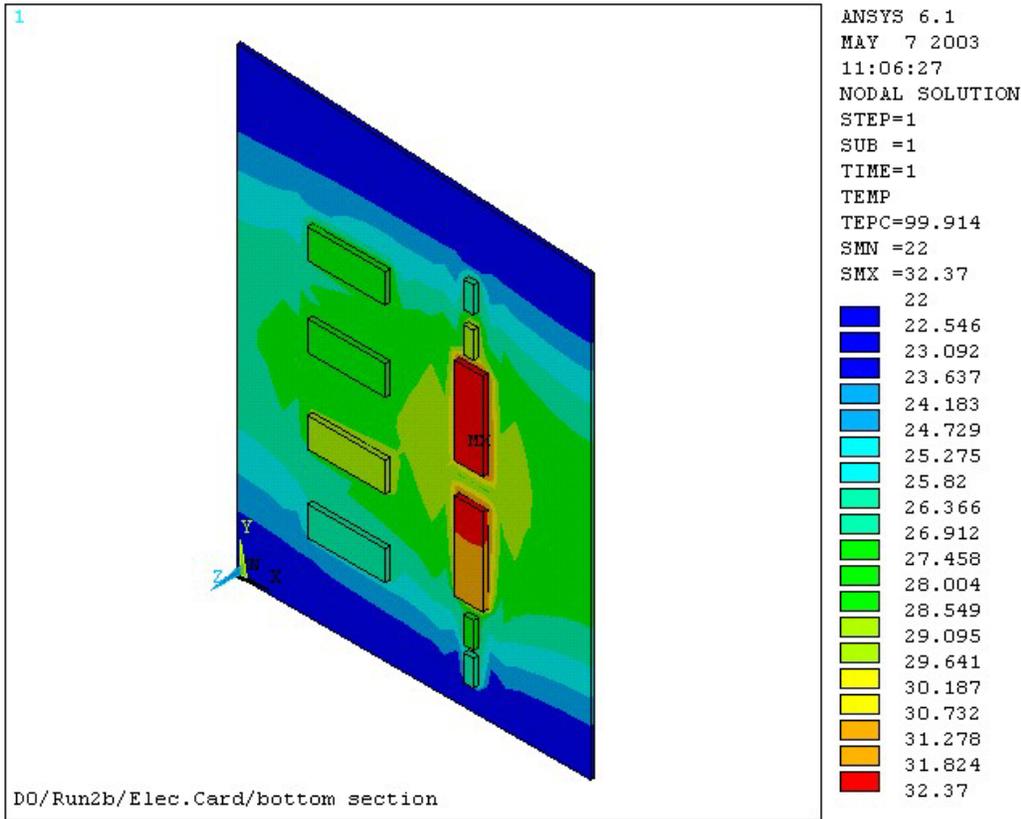
**Models**





## Results





The maximum temperature achieved in the model is 36 °C on the top side.

When testing the real complete card, the temperature reduction effect by convection and with the conduction through the additional layers present should be insignificant. However, lack of good thermal contact between the chips and the G-10 may significantly increase the maximum temperature reached.