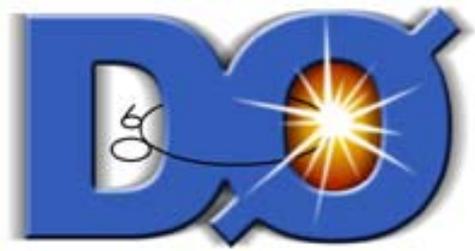


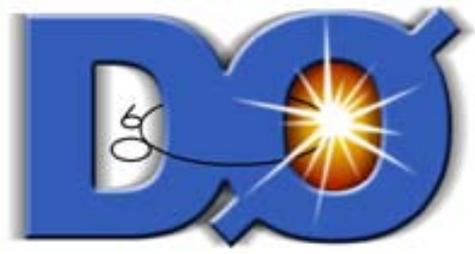
1% Teststand Status

S.Burdin (FNAL)



Recent problem

- ✓ Unstable readout during first ~50 events in 1553 and SCL modes (396)
- ✓ Reason: no clock when PRD2 is high
- ✓ Mike's fix for firmware helped a lot



✓ Readout was tested for the following modes:

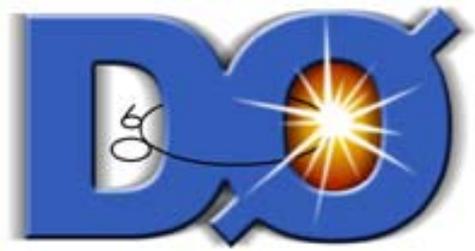
➤ VRBC

- Regular trigger: 132 & 396
- Cal. Inject: 132

➤ 1553

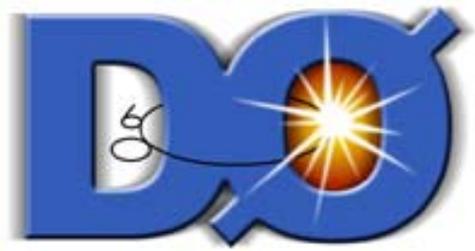
- Regular trigger: 132 & 396
- Cal. Inject: 132

➤ SCL

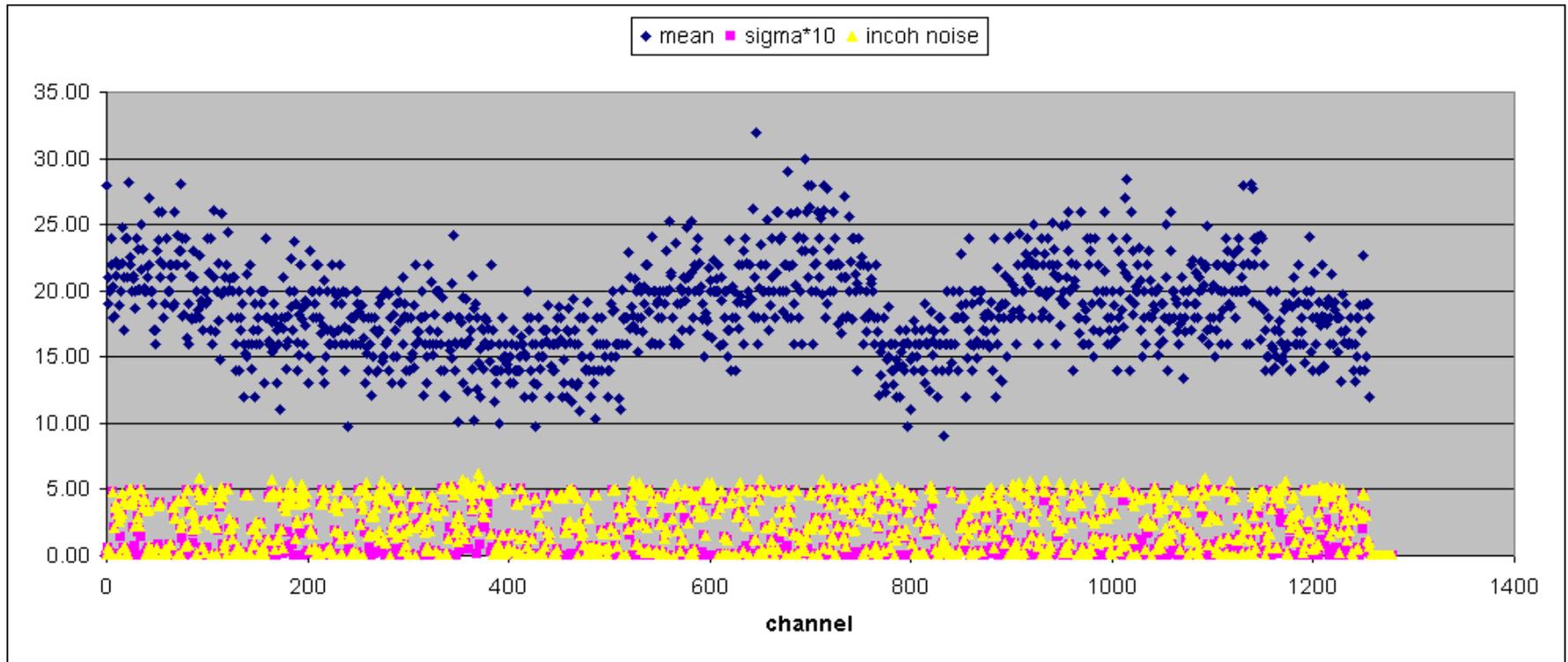


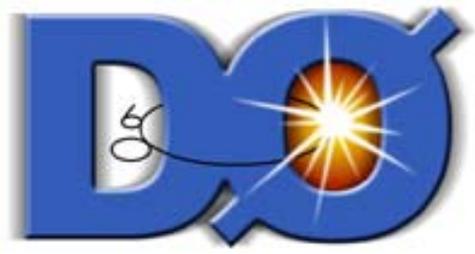
Tests with high statistics

- ✓ Rate ~30Hz
- ✓ VRBC Regular trigger (396): ~850k, no errors
- ✓ 1553 Regular trigger (396): ~850k, no errors
- ✓ SCL mode:
 - Total: 1M events
 - Repeated events: 4
 - Wrong word length: 8



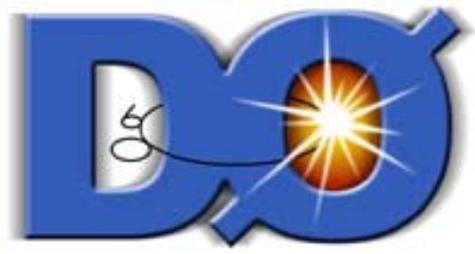
Output in SCL mode





Convert SBC output to L3 format

- ✓ Program to decode the SBC output under Linux is ready
- ✓ Packing into the RDC is underway:
 - L3base (G.Watts) package can be used



Plans

- ✓ Try to increase the rate at least in SCL mode
- ✓ Check the readout in Cal. Inject (396) mode
- ✓ Prepare the data file in L3 format