

Commissioning the L1CalTrack Trigger System

This document describes items which must be completed in order to commission the L1CalTrack Trigger system. The document is divided into three sections: Hardware, Infrastructure, and Software. Presently the document is more a note to us in order to search for tasks that are overlooked.

I. Hardware

- a. JTAG boundary scan test MTFB's and MTCxx's.
- b. All production MTCM, MTCxx, and MTFB cards are tested on test stands at Arizona and Fermilab using the MTT. The MTT provides an excellent proving ground for the hardware. That is, we can test all inputs, timing, buffering, and L1, L2, L3 outputs. The new MTT is certified and we are using it in loop tests at Arizona. We plan to build four more MTT's to populate Arizona, Boston, and Fermilab.
- c. Our top goal for the summer is to produce BOT (beginning-of-turn) triggers and to readout both L1CalTrack crates. The L1CalTrack crates reside in M119. Note it may be necessary for Stu to eventually move some of his Ethernet hardware in that rack. Another issue is that the power supply for crate 0x19 in the 3rd floor MCH must be replaced in order to accommodate an additional MRC card in that crate.

Initially we will use spare L1MU MTCM's and MTCxx's and replaced them with production L1CalTrack cards once they pass test stand scrutiny. For inputs we will use spare L1MU inputs on cables FPD 4 and 5 that run from PE to MCH1. Right now one is connected to an A-layer PDT. One important test will be to produce BOT triggers that can be sent to the TF. Achieving a stable BOT rate of 47712 is an excellent indication that the trigger system is working.

Another important test is to readout the L1CalTrack crates into L3. Here we can check both the bunch crossing numbers and trigger results. Achieving this readout is an excellent indication that the trigger system is working. The testing can be done between stores.

Performing these tests with existing L1MU MTCM's and MTCxx's will ensure all connections are properly made. Next we will replace L1CalTrack hardware with L1MU hardware. This will ensure the L1CalTrack MTCM's and MTCxx's are functioning properly in the running experiment. Next we will commission the new L1CTT inputs when they become available. Finally we will commission the L1CAL inputs when they become available. These latter two steps are relatively

minor compared to the first two. We'll use resistance measurements and parity error checking to certify these cables.

Some other things to worry about are:

- d. Modifications must be made to PDT front-ends at some point. This is a big job. Perhaps we should try to schedule this work for the August 04 shutdown. If so, we must start work now.
- e. We must install the SLDB transmitters for the L1CTT on the new DFEA boards. Jamieson told me the plan here is to setup a system in parallel with the existing one. We could install the SLDB transmitters at that time. However at the moment we probably don't have enough transmitters to run two FULL systems in parallel.
- f. We must install new splitter cards in the collision hall. Or possibly another splitter crate. The current splitter map is at www-clued0.fnal.gov/~robmcc/thesis.html (appendix A). This is a small job. Rob has a plan here.

The plan is: Unplug the "a" cables at the CTT end. These are the normal cables. Unplug the overlap cables from splitters 10 and 11 and move them down into two new cards into the lower splitter crate (central and north scintillator splitters). The output of these two new splitters will go to CTT splitters 0, 9, 10, 11.

- g. There will not be enough free AND-OR terms to do testing. This has to be sorted out.
- h. We should complete a first pass of trigger logic for L1CalTrack. The terms should include BOT terms, L1CTT only terms, L1CAL only terms, L1CAL.and.L1CTT terms for electrons, L1CAL.and.L1CTT terms for taus, and L1CAL.and.L1CTT terms for jets (if any). Some of these (BOT and L1CAL.and.L1CTT taus) are already implemented.
- i. We also need to swipe several 68040 processors from Darien/Dennis who have hidden them away from us. We have to take the processors off the 280mm extender cards, put the front panels back on, and put them on our 400mm deep extender cards.

II. Infrastructure

For infrastructure, this is more a todo list than a plan.

- a. We have already run LMR-200 cables from the collision hall to the 1st floor MCH for L1CTT. We will have to run LMR-200 cables from L1CAL to the 1st floor MCH when we know where L1CAL will be located.
- b. We have also already run twist-n-flat cables from the 3rd floor MCH to the 1st floor MCH for readout. We will also take advantage of an existing 24-wide ASTRO cable between the 3rd floor MCH and the 1st floor MCH. We will need to run two (including spare) 8-wide ASTRO cables to connect to this main trunk on the 3rd floor MCH and three (including spare) 4-wides to connect to this main trunk on the 1st floor MCH.
- c. We have to terminate all LMR-200 cables. We have to terminate all MTCXX LMR-100 cables. We have to terminate all DFEA-backplane LMR-100 cables. We have to terminate all backplane-pigtail LMR-100 cables. Jamieson needs to come up with a plan for the latter.
- d. We need to load-test our Wiener supplies and then install them in the 1st floor MCH. We need to produce a safety document and pass the safety review.
- e. We need to install RMI's, RM's, heat-exchangers, and blower-fan in rack M119. We will need to get these items from the D0 support group which may be problematic. I also have to check on the 220V connections in the 1st floor MCH. John Anderson said we could use a breakout box like we use on PE. Need to get our hands on this.
- f. We'll need to run 1553 cables to our MTCM's and perform 1553 tests. Shou Moua and Vladimir Sirotenko are the guys we need to bug.
- g. We also need Ethernet connections to the processors in our crates. Follow the FPD TM back to see if there are free spigots. Otherwise must talk to Stu.

III. Software

Again this is more just a todo list.

- a. Modify existing VxWorks to work with L1CalTrack.
- b. Add L1CalTrack startup to cold-start GUI.
- c. Modify COOR download to include L1CalTrack.
- d. Add L1CalTrack to parity-check GUI.

- e.** Add L1CalTrack to mtm-term GUI.
- f.** Add monitoring histograms to L3 Examine.
- g.** Add L1CalTrack to online simulator-hardware comparison code.
- h.** Add L1CalTrack to online efficiency code.
- i.** Develop code to readout L1CalTrack data from RDC.
- j.** Develop code to write L1CalTrack results to TMB.
- k.** Complete L1CalTrack simulator in tsim_11muo.