Progress on the L1 Calorimeter Trigger (WBS 1.2.1)

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for the L1Cal group

Outline

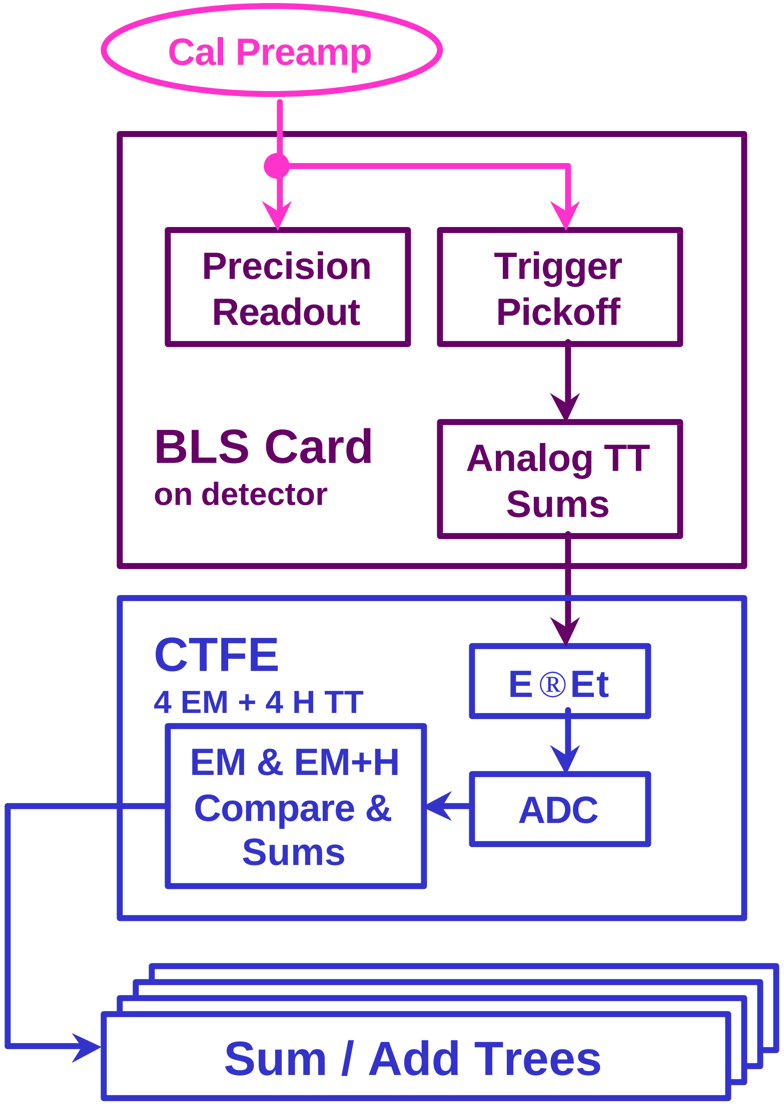
- Simulation Update
  - choice of baseline algorithms

- Baseline Design
  - ADC-Digital-Filter Board
  - Trigger Algorithm Board

L1 Cal in Run IIa

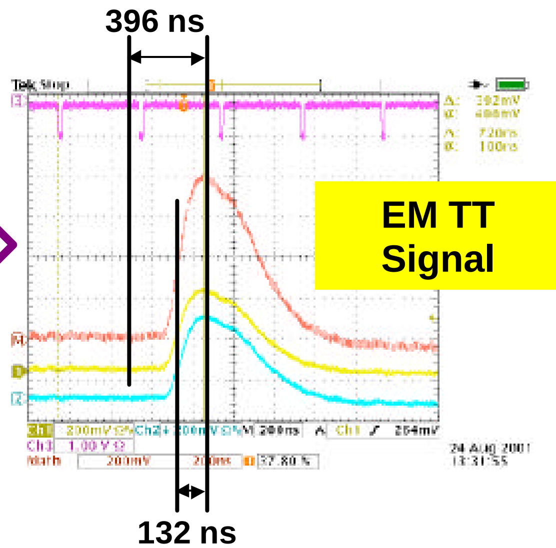
- DØ U-LAr Calorimeter
  - Hermetic: |h| < 4.2
  - Energy Resolution
    - EM: ~14%/ÖE Å <1%
    - Jet: ~80%/ÖE
  - Cells: Dh´Df = 0.1´0.1
  - Sampling: 4 EM, 4-5 Had
- Level-1 Calorimeter Trigger
  - Using Run 1b System (1990)
  - Unit = Trigger Tower (TT)
    - Dh´Df = 0.2´0.2 Þ 40´32

  Þ 1280 EM + 1280 Had
- Outputs
  - # EM & EM+H TTs > 4 Thr
    - also avail. by quadrant
  - Global E_T Sum & Missing E_T

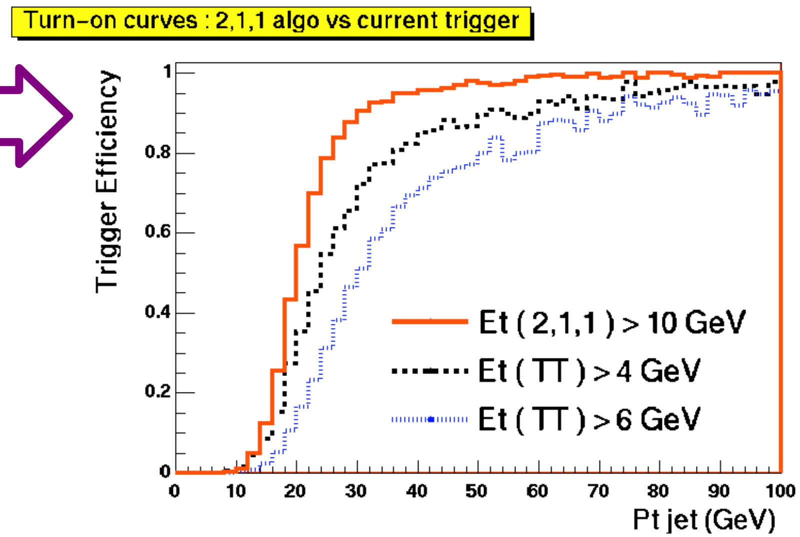


Summary of Problems

- **Signal rise > 132 ns**
  - can cross threshold before peak
    Þ trigger on wrong x'ing
  - affects high-Et events



- **Poor Et-resolution**
  - jet size > TT size
  - EM Et on TT boundaries
  - ICR Et not included
  - Þ slow turn-on curves



Trigger	Phys. Chan	Rate (kHz)
EM Trigger 1 TT > 10 GeV	W ® ev	9
Jet Trigger 2 TT > 4 GeV	ZH ® vvbb	2 (L = 5e32)

L1 Cal Simulation

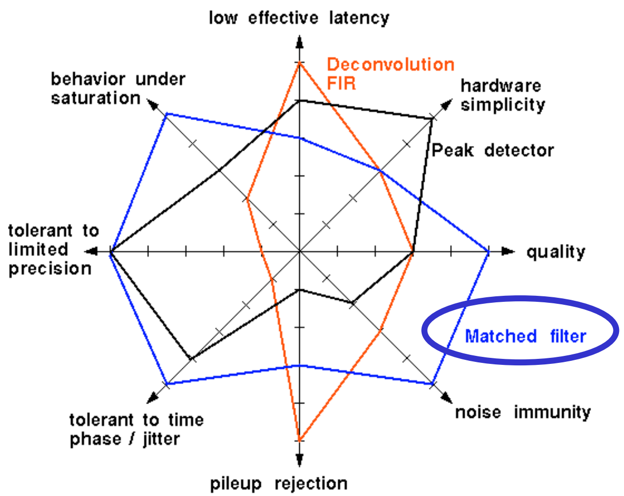
- Progress in Simulation
  - Run 2b L1Cal simulation integrated into DØ code
- New simulation results Þ Baseline Algo's

Item	Baseline
Digital Filter	Matched Filter + Peak Detector
Jet Algorithm	Sliding Windows parameters chosen • 2x2 RoI, 5x5 Decluster, 4x4 Cluster Et • Note: this drives the TAB hardware
EM Algorithm	Sliding Windows with hadronic and EM isolation • specific parameter set implemented
Tau Algorithm	"Narrow Jet" w/ Et(2x2)/Et(4x4) > cut
ICR	Include ICR energies in Global Sums and Clusters • modest gains indicated from simulation

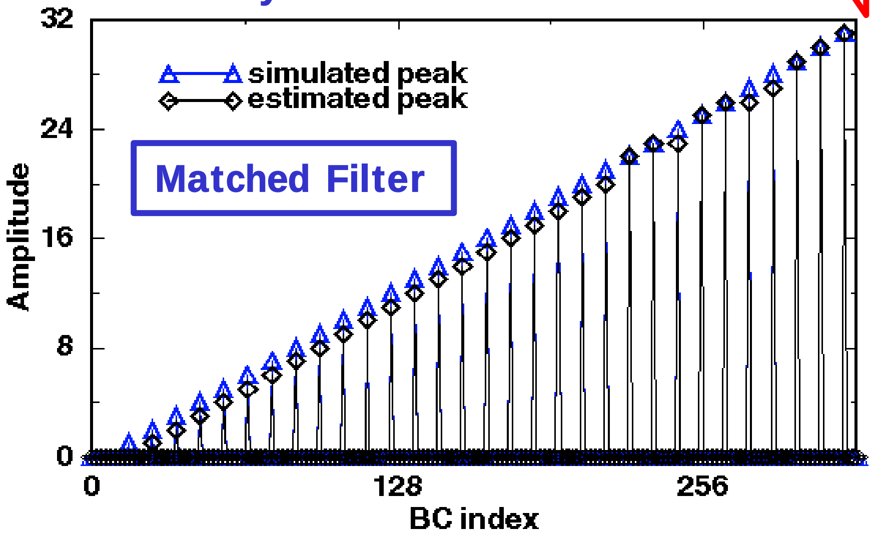
Digital Filter

- **Performance Criteria**
  - latency, #params, satur.
  - Et-res, BC mis-ID, Dt
  - noise, phase, jitter, shape
- **Algorithms Studied**
  - Deconvolution FIR
  - Peak Detector
  - Matched Filt + Peak Det

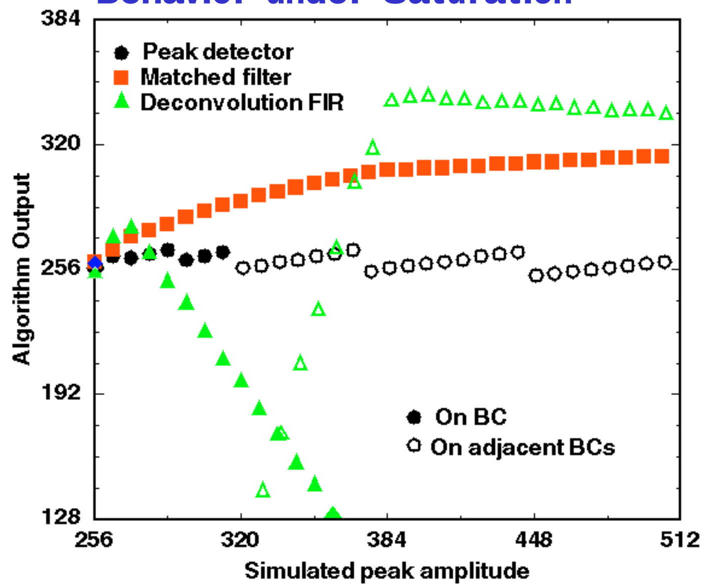
baseline



Linearity



Behavior under Saturation



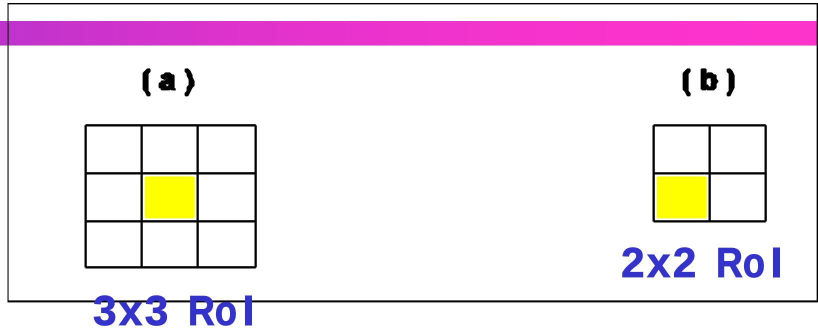
Digital Filter Algorithm

- **Matched Filter + Peak Detector**
  - Impulse filter Þ Et
  - 3-Point Peak Detector Þ Find peak
  - Strengths
    - linearity
    - robust against signal phase shift [-32ns – +32ns]
    - stable under modest saturation
  - Relative Weaknesses
    - latency can be large
    - does not resolve signals very close in time (few BC)
- **Testing the Algorithm**
  - currently: a few digital scope traces of signals
  - designing a “Splitter Board” to allow signals to be recorded while taking data with old system

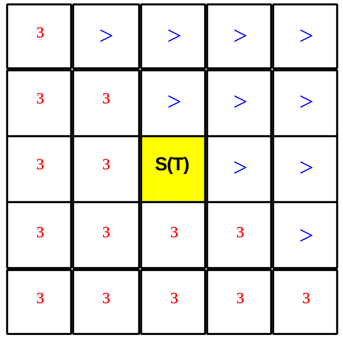
Jet Algorithm

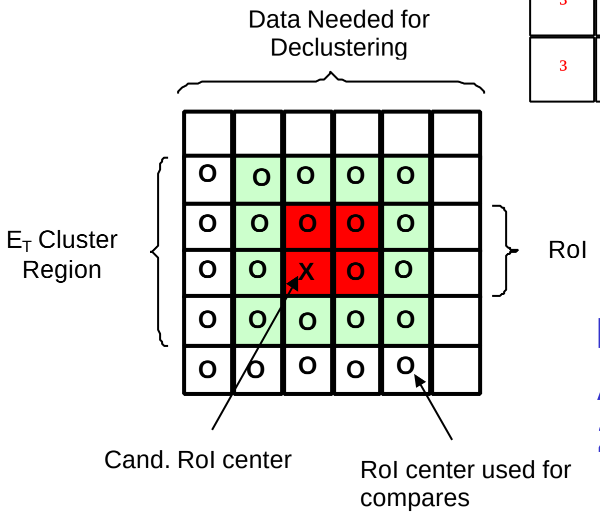
- **Algorithm parameters**
  - RoI Size
  - Declustering Region Size comp's to find Local Max
  - Et Cluster Region
- **Algorithms studied**

Algo	RoI (TTs)	Declust (RoIs)	Et-Clst (TTs)
2,1,1	2x2	5x5	4x4
2,0,1	2x2	3x3	4x4
3,0,1	3x3	5x5	5x5
3,-1,1	3x3	3x3	5x5



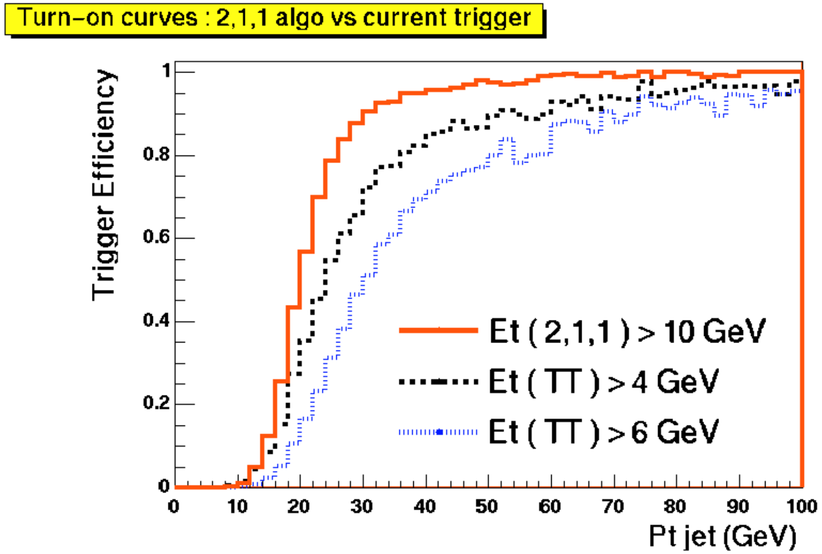
5x5 RoI declustering region

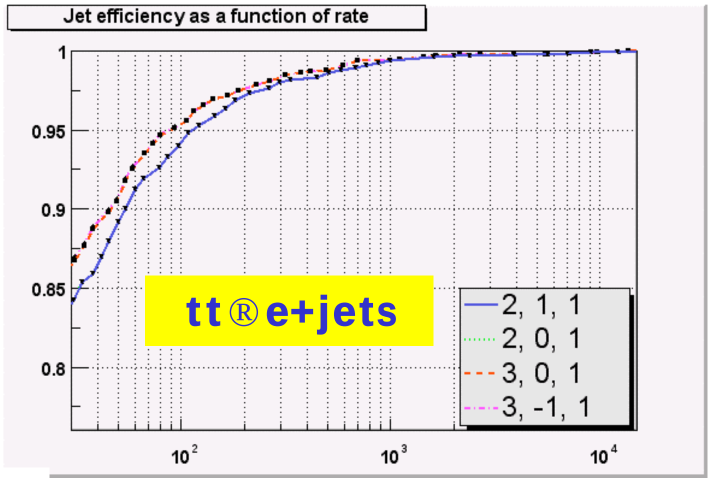




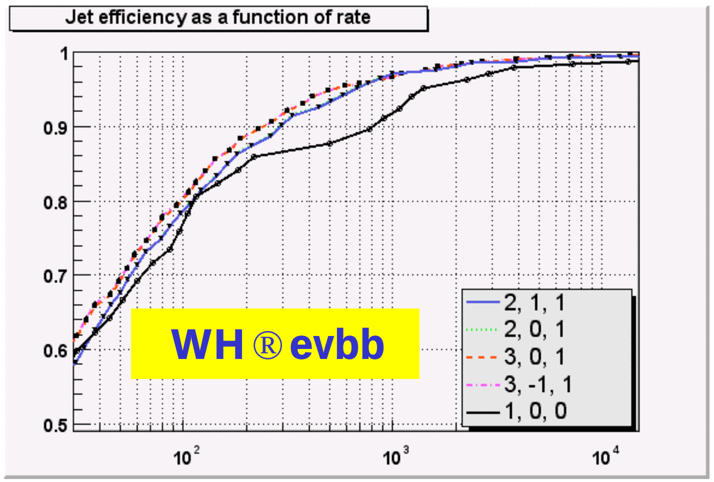
Baseline Jet Algorithm 2,1,1

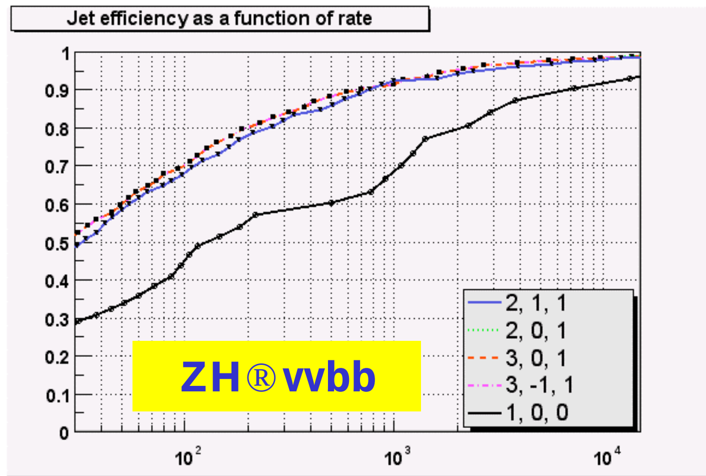
Jet Algo Comparisons



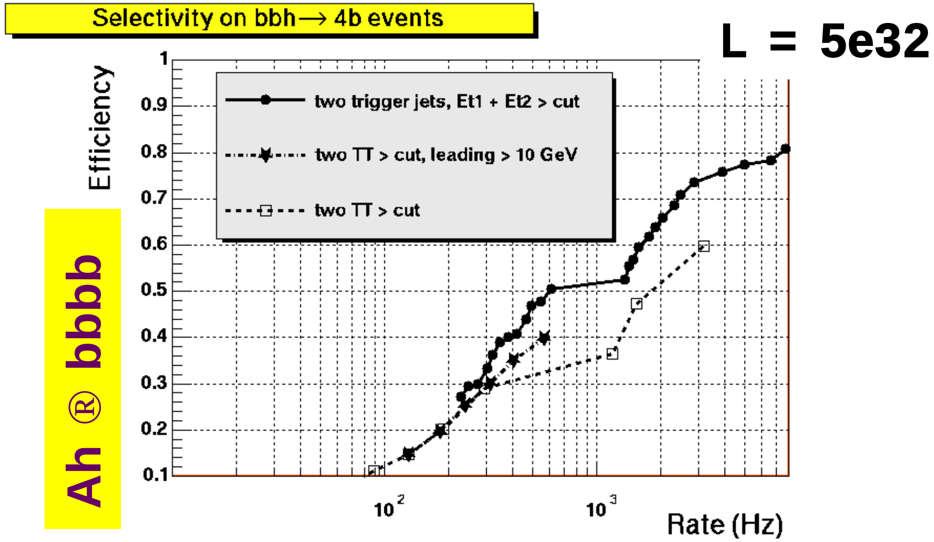


L = 5e32





Jet Eff vs Rate



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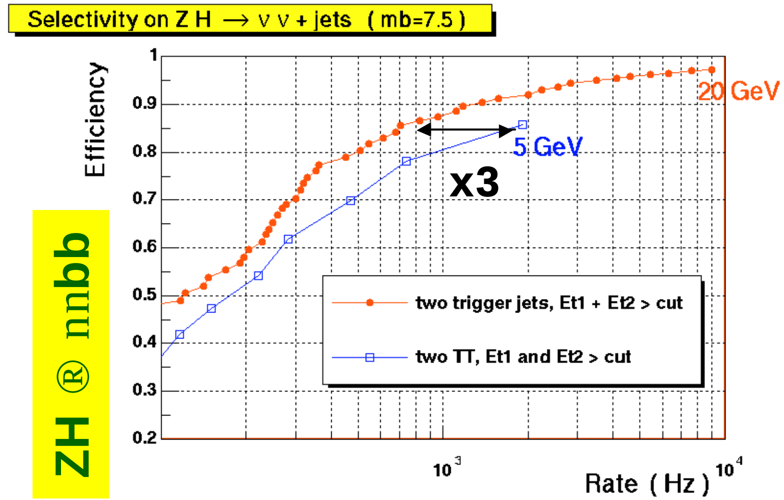
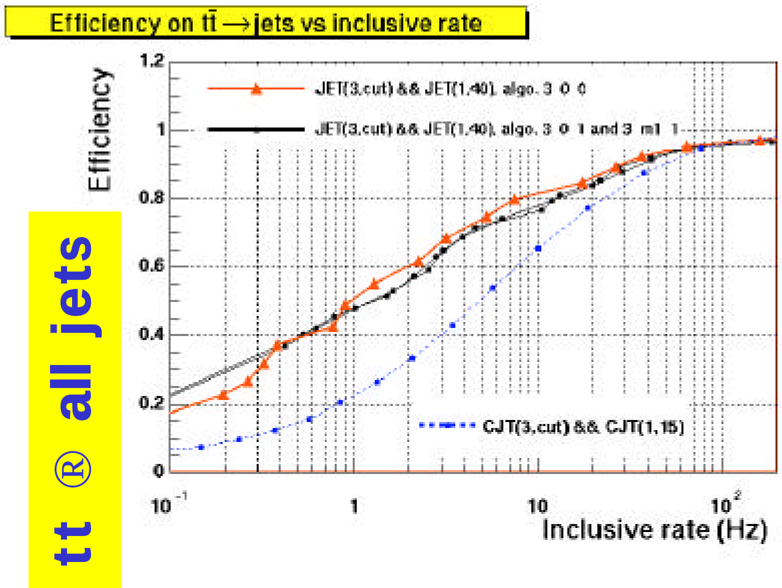
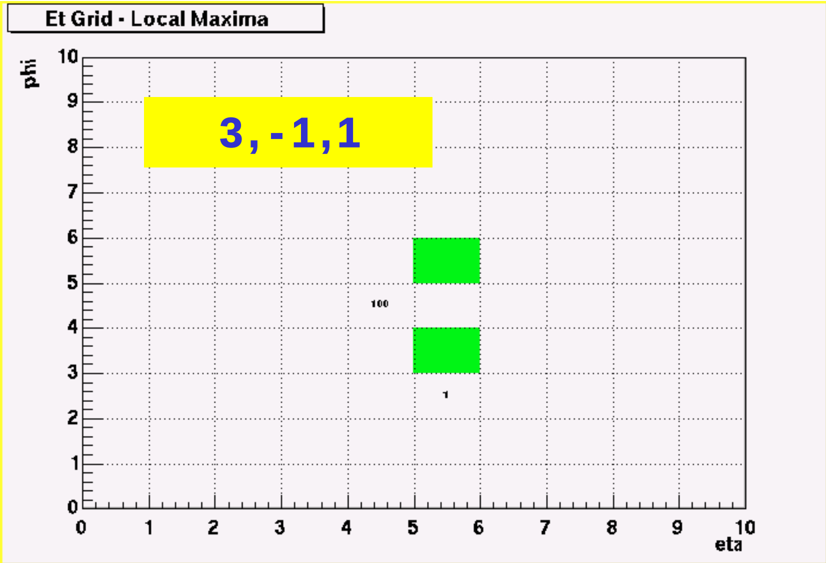


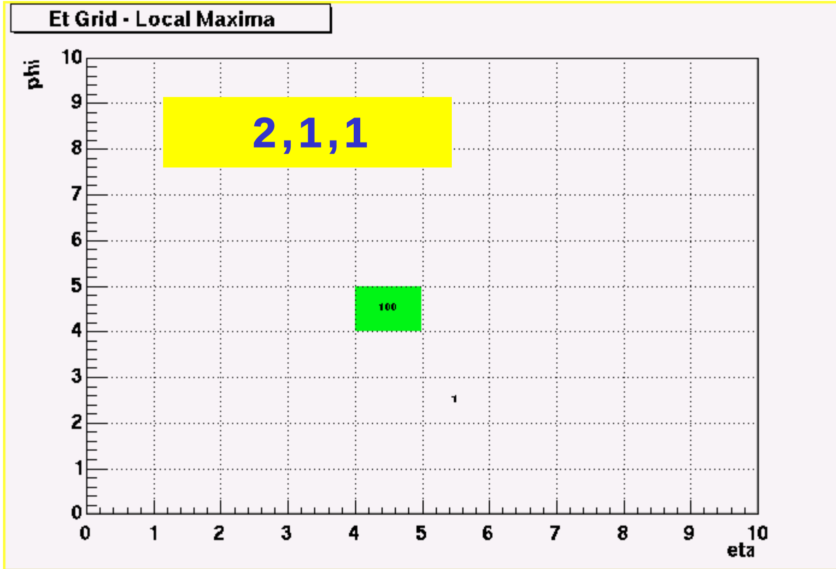


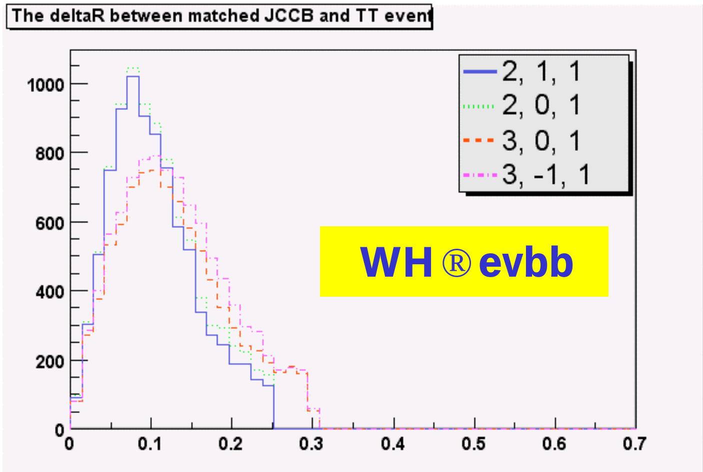
L = 5e32		Rates (kHz)	
Trigger	Phys. Chan	no upgr	w/ upgr
EM Trigger 1 TT > 10 GeV	W®eν	9	0.5
Jet Trigger 2 TT > 4 GeV	ZH®ννbb	2	0.5

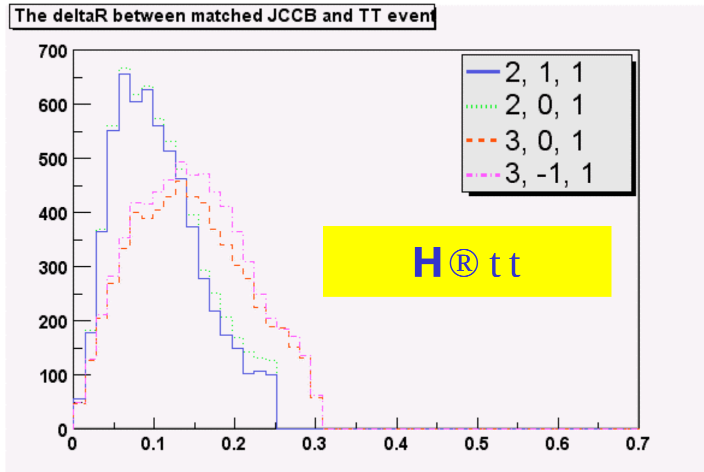
L1 Rate Limit: 5 kHz

Position Matching to Jets

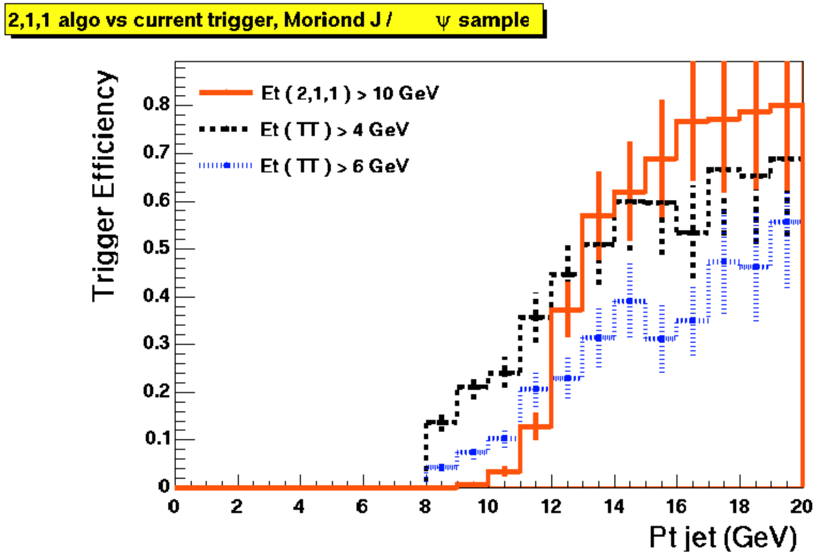




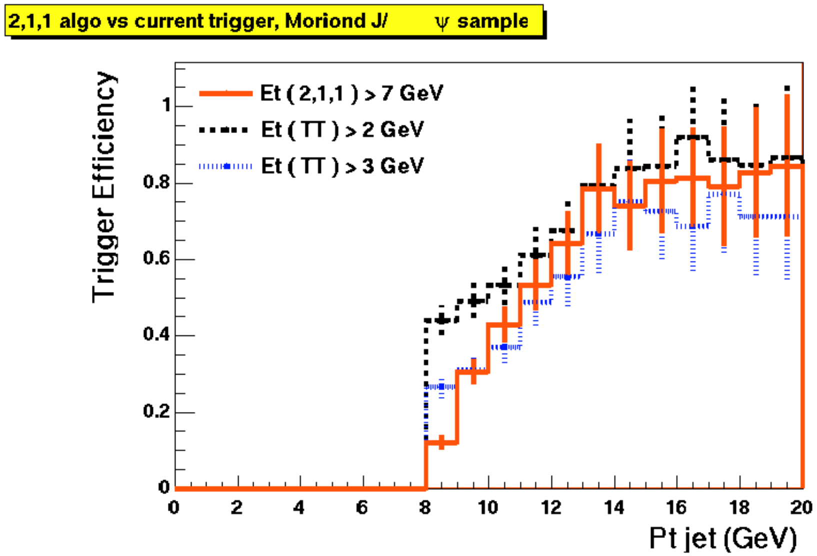




1st Look at Data !!!

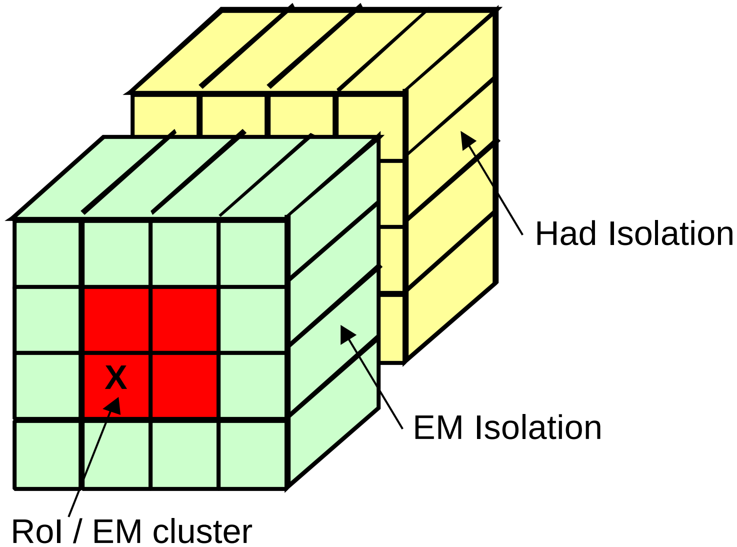


$J/\psi \rightarrow \mu\mu$
Data Sample

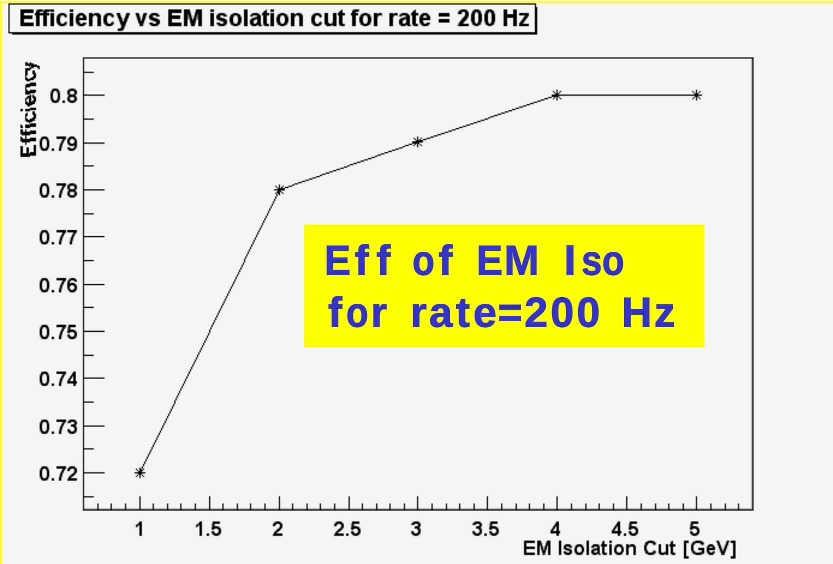


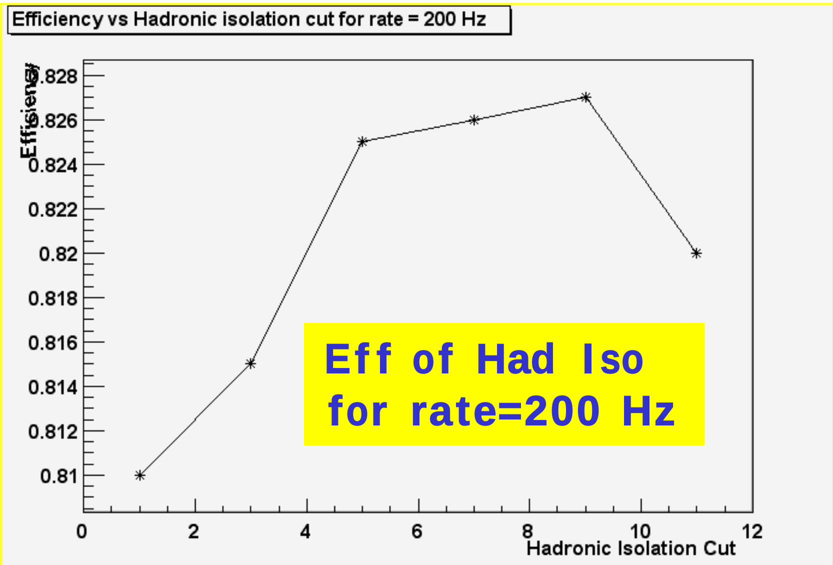
EM Algorithm

- Algorithm parameters
  - RoI size
  - Decluster Region size
  - Et Cluster = RoI
  - EM Isolation
  - Hadronic Isolation
- Eff. vs Rate studies still under way
  - have chosen a conservative algorithm as baseline



EM Algorithm Studies

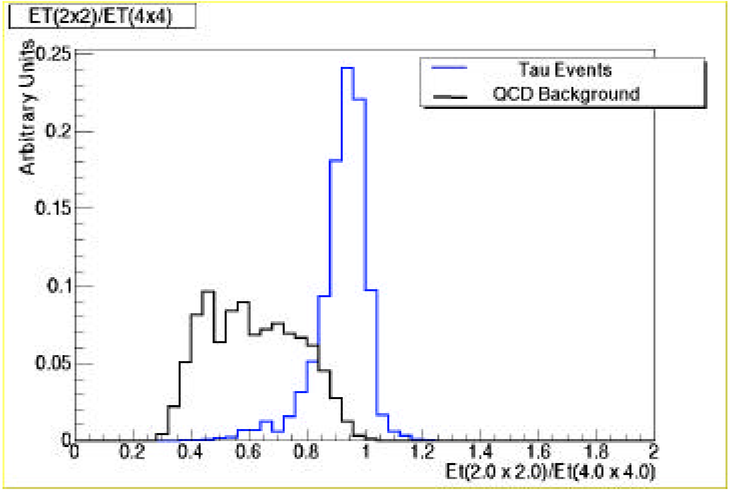




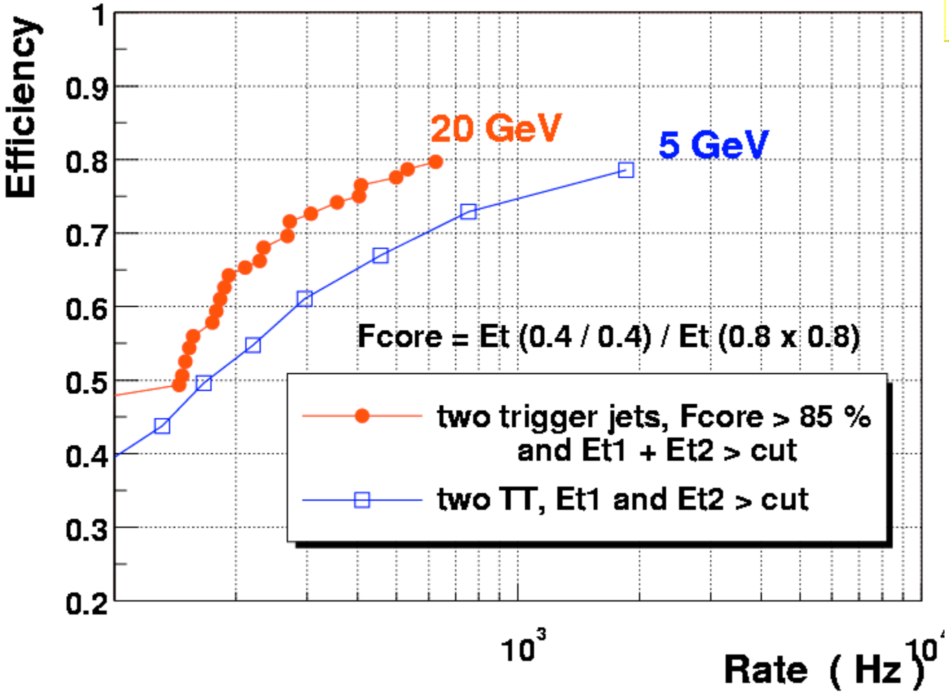
- Important to understand effects of isolation requirements on EM algorithm
- EM Isolation Requirement
  - Et(EM-ring) < *X*
- Had Isolation Requirement
  - Et(EM-RoI)/Et(Had) > *f*
- Plots
  - for a several iso. cuts
  - vary EM-RoI thresh to prod eff. vs. rate curves
  - plot eff. at a given rate for each iso. cut

Tau Algorithm

- Tau's = Narrow Jets
  - Et(2x2) / Et(4x4)
- Simple Algo for base.
  - uses results of Jet Algo

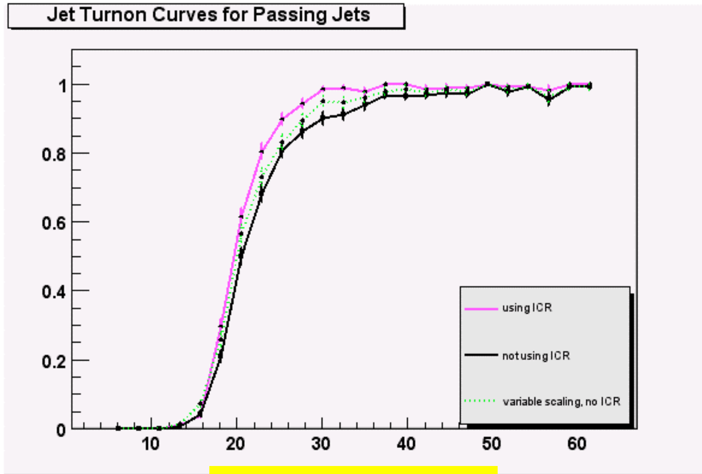


Selectivity on H → ττ → dijets (mb=7.5)

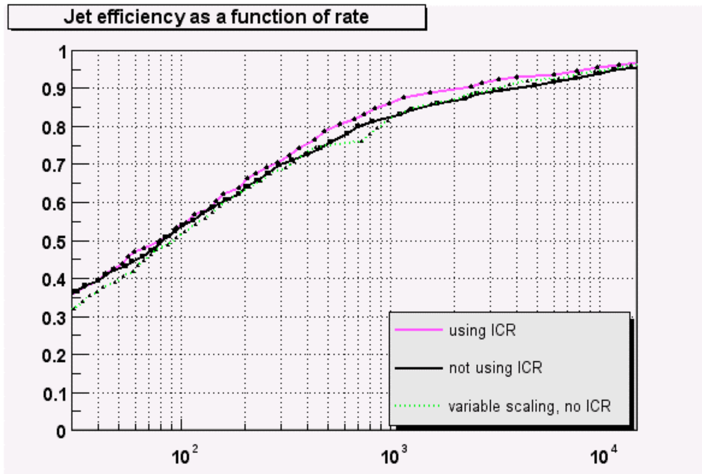


Inter-Cryostat Region

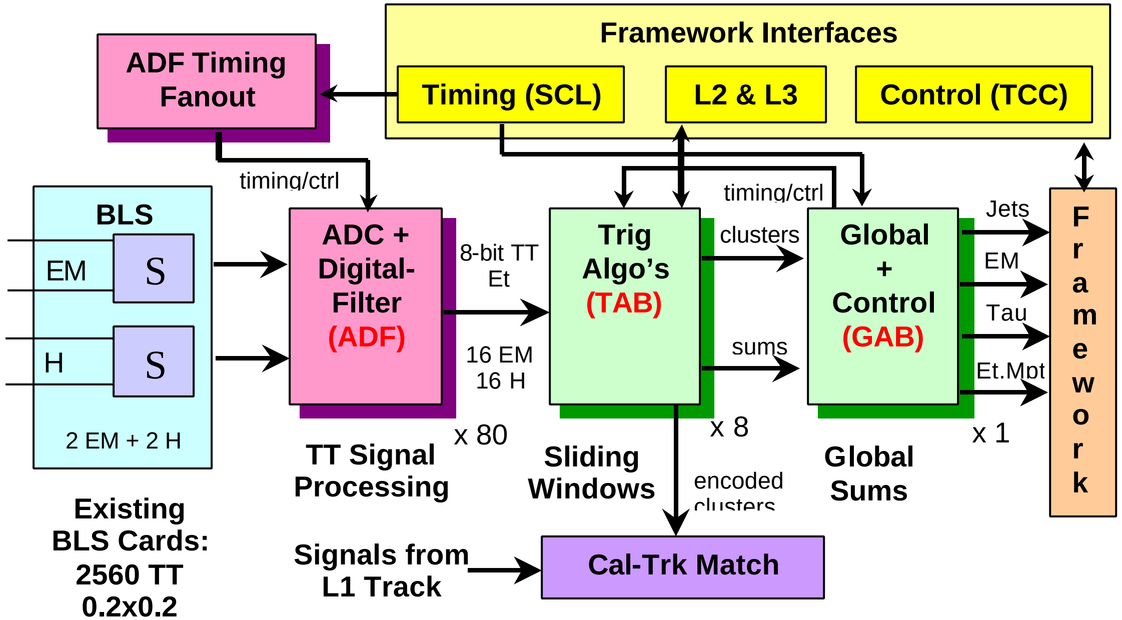
- Extra detectors added in area where endcap and barrel cryostats meet
  - (ICR = 0.8<|h|<1.5)
- These now available for L1 trigger
  - data sent physically as TTs at extreme +/-h
- Issues:
  - add ICR to Global Sums
  - add ICR to clusters
  - the 1^{st} is fairly easy the 2^{nd} more difficult in hardware terms



ZH®vvbb



L1Cal Hardware Overview



Board	No	Input (h´f)	Output (h´f)	Purpose	Status
ACD/Dig. Filt.	80	4x4	4x4	digitize, filter, E-Et	in design
ADF Timing F'out	1	all	all	control of ADF	concep des.
Trig Algo Brd	8	40x9	31x4	algo's, Cal-Trk, sums	start layout
Global Algo Brd	1	all	all	TAB ctrl, sums, trig's	concep des.

Who's Who in L1Cal

Saclay — **ADFs/ADF Timing/Splitters**

- Physicists: J.Bystricky, P.LeDu*, E.Perez
- Engineers: D.Calvet, I.Mandjavidze, M.Mur

Columbia/Nevis — **TABs/GABs**

- Physicists: H.Evans*, J.Parsons, M.Tuts
- Engineers: J.Ban, B.Sippach

Michigan State — **Framework/Integration**

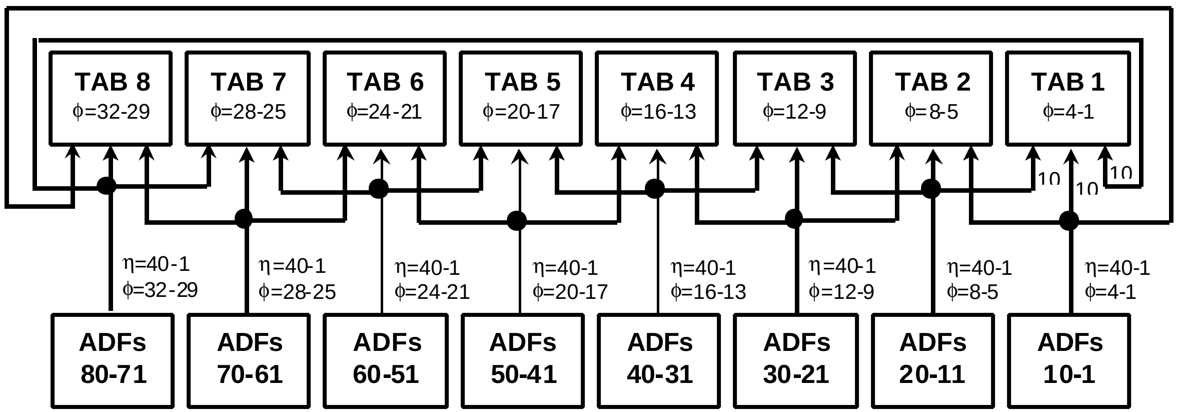
- Physicists: M.Abolins*, C.Brock, H.Weerts
- Engineers: D.Edmunds, P.Laurens

\+ Postdocs and Students

* L1Cal Project Leaders

Data Routing

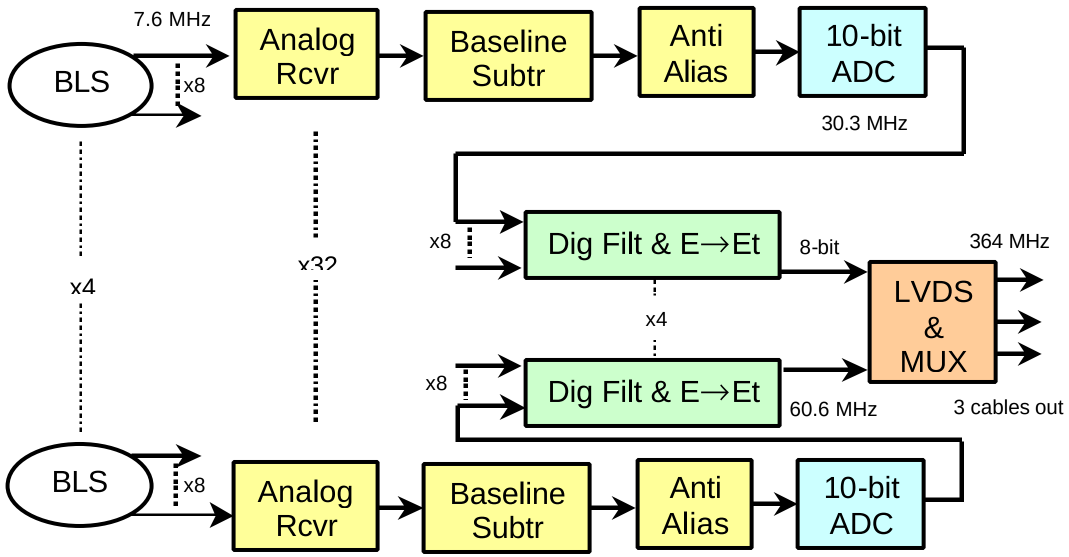
- System design driven by data sharing requirements of sliding windows algorithm
  - 2,1,1 Algo: data from 6x6 region to find one Local Max
    - Þ lots of data sharing
  - ICR included in jets: each TAB must get all data in h
  - Simple design: ADFs send out 3 identical copies of their data
    - Þ each TAB: inputs 40x9 – outputs 31x4 (edge effects)
- Serial Data transmission w/ MUXing
  - 2560x3 = 7680 separate signals
  - baseline = LVDS using National Channel-Link (de)serializers



ADC-Digital-Filter Design

ADF Function	Cand. Comp / Comments
Analog Receiver	Analog Devices AD8138
Baseline Subtr/Offset	Maxim octal 12-bit serial DAC
Anti-Aliasing Filter	Passive RC comp's
10-bit Analog-to-Digital	Analog AD9218 (40 Mbps)
Digital Filter	Xilinx Vertex 2 – 500K gates
10-bit E ® 8-bit E_T	0.25 GeV LSB
LVDS serializer	Channel Link DS90CR483 (48-8)

- 80 ADF boards
  - 6U VME
- 5 VME crates
  - Wiener 6023
  - custom b'plane
    - inputs, timing
  - VME interconnect



ADF to TAB Transfer

Transfer Data from ADFs to TABs Serially

- LVDS links
- (16 EM + 16 Had)×8-bits / 132ns = 242 Mbytes/s

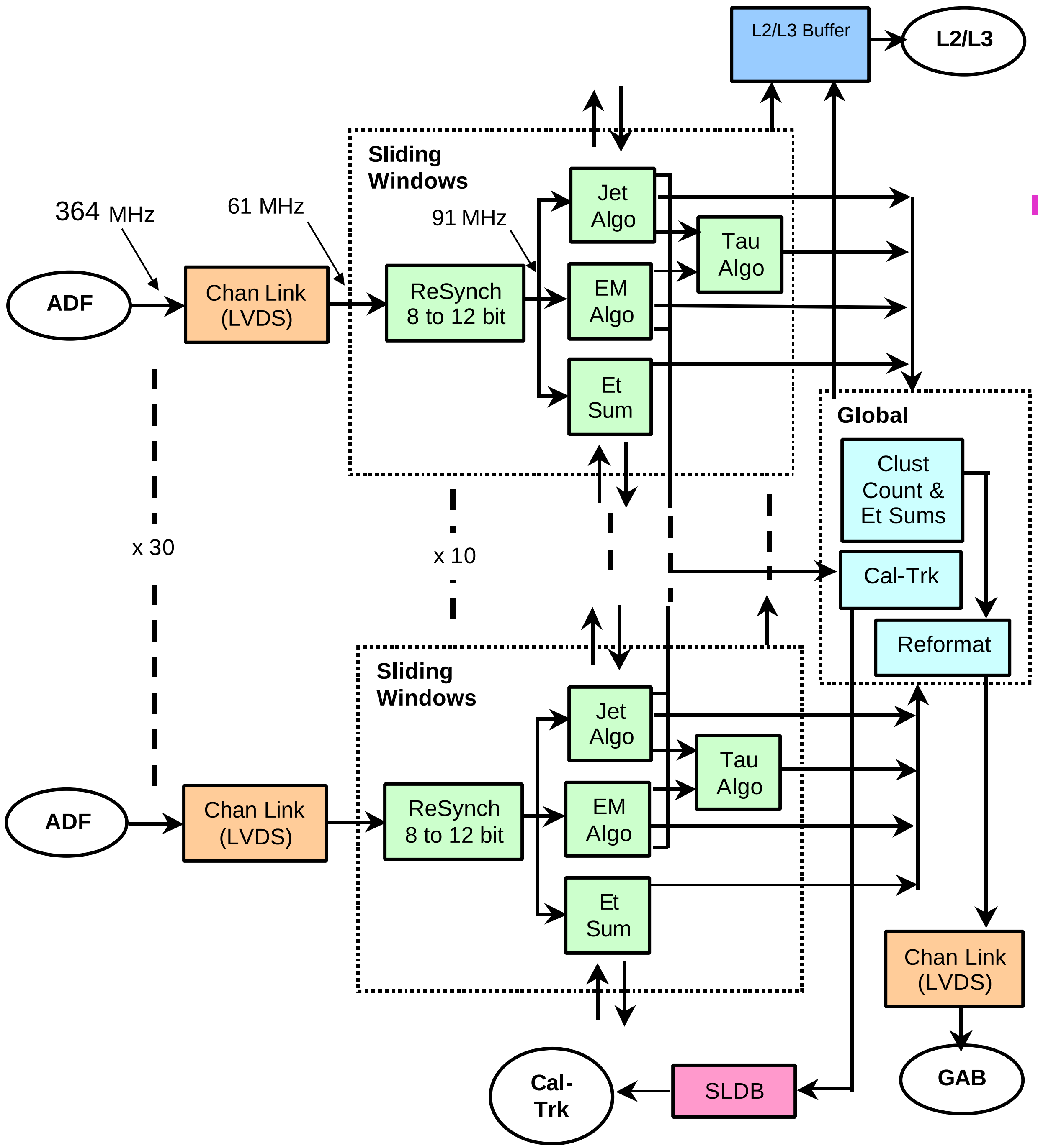
2 Solutions Considered

- LVDS on FPGA
  - + elegance, flexibility
  - + lower comp. count
  - - constrains design
- Use custom LVDS chipsets
  - + simple, factorizable
  - - use existing mux's
- Must match solution to available cables

Baseline = Custom LVDS chips

- Drivers/Receivers
  - 48:8 / 8:48 National Channel-Link chipset
    - use only 32:6
  - Data Input: 60.6 MHz
  - Data Output: 364 Mbit/s
  - Chips rated to 672 MHz
    - Atlas demo 480 MHz over 20 m cables
  - Unit Cost: $11
- Cables/Connectors
  - 6 data-pairs, Clk, Frame, Parity, data select
  - AMP w/ 2 mm hard-metric connectors
  - Unit Cost: ~$75

Algorithm Board Design

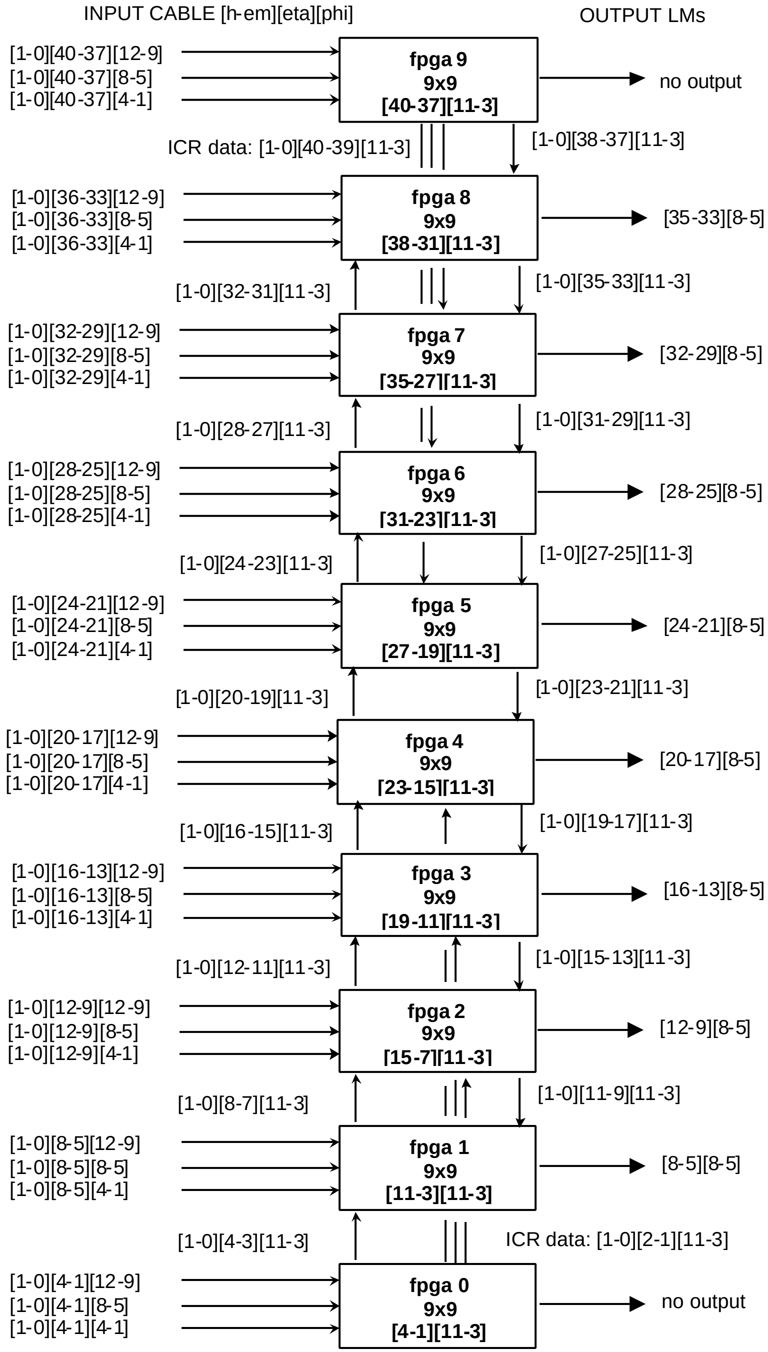


- 8 TABs
  - dbl-wide - 9U VME
- 1 Crate
  - VME CPU
  - GAB

Algorithm Board Comp's

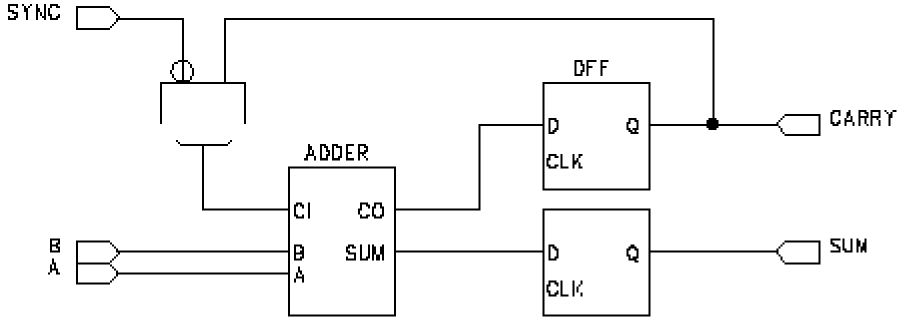
TAB Function	Component
LVDS Inputs from ADF	Channel Link - DS90CR484 (8-48)
Sliding Windows • resynch 8 to 12-bit • EM, Jet, Tau, Algo • generate Cal-Trk output • L2/L3 Buffering	Altera Stratix - EP1s10F780C6
Global • Cluster counts & sums • output to Cal-Trk	Altera Stratix - EP1s10F780C6
LVDS Output to GAB	Channel Link
G-Link Fiber Output to L2/L3	G-Link Transmitter
Serial Link DB Output to Cal-Trk	existing DB from U Arizona

Intra-TAB Data Routing

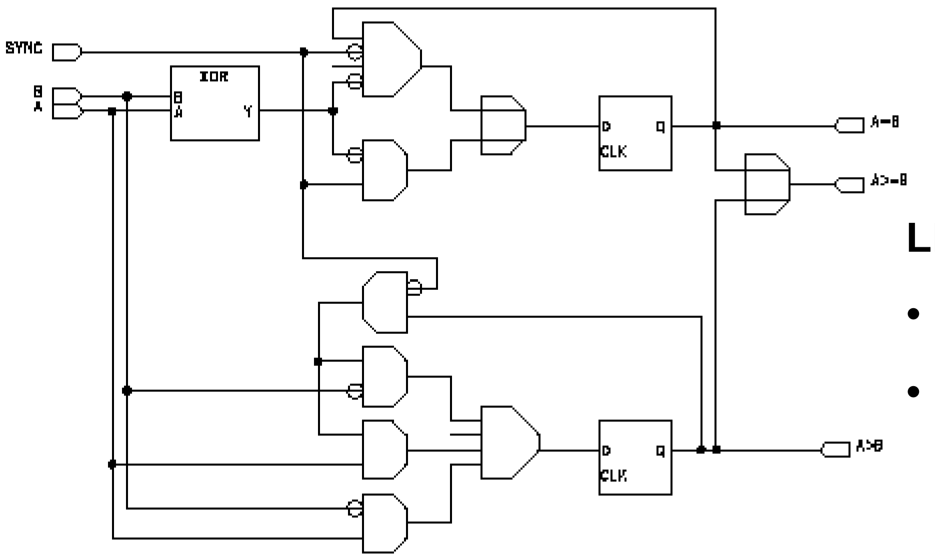


Serial Architecture

Serial Adder



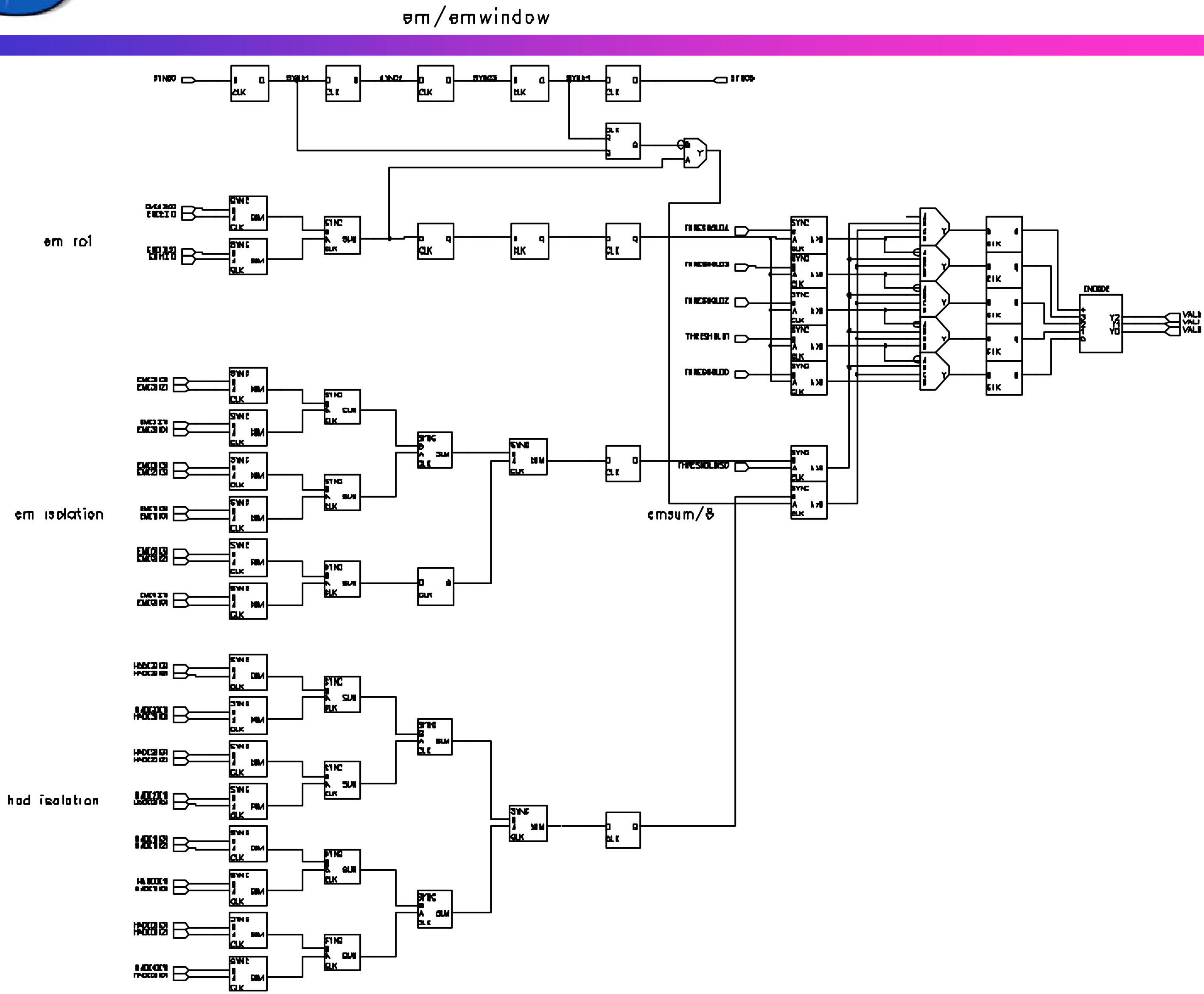
Serial Compare



LM finding needs

- **A>B**
- **A>=B**

Serial EM Algorithm



Other Electronics

- ADF Timing Distribution
  - fans out subset of f'wrk timing & control signals to ADFs
    - uses existing SCL rcvr
  - conceptual design w/ signals needed specified
  - still under discussion – where to put this card
- Splitters
  - needed to get high-stat's Cal signals for digital filter studies
  - must be an active splitter
  - design done – layout started
  - will be installed in next long shutdown
- Global Algorithm Board
  - Final summing of partial sums from TABs
  - Forms trigger terms from sums and cluster counts
  - Transmits trigger terms to Framework
  - Sends timing & control signals to TABs
    - uses existing SCL rcvr
  - Conceptual design started
    - signal set specified
    - needs final TAB design
  - Main Issue
    - how to perform signal fanout
    - cables?, backplane?

Integration

Stage	Tasks
Proto/Pre-prod	Based on experience with other systems (STT) • Verify ADF-TAB-GAB communication • Integrate with DØ Framework / DAQ • Shakedown online software • Goal: demonstrate that L1Cal functions in DØ
Final Install	Detailed plan from D.Edmunds (Run IIa) • Remove old L1Cal • Install cables • Populate crates (largely outside of MCH) • "Physics" commissioning w/ beam
* all groups will participate in all integration tasks	

Conclusions

- L1 Cal System well under way
  - baseline algorithms chosen for all elements
  - design work started on all components
  - some in layout phase
- Simulations indicate that new L1Cal is crucial to achieve Run IIb Physics Goals

L = 5e32		Rates (kHz)	
Trigger	Phys. Chan	no upgrade	w/ upgrade
EM Trigger 1 TT > 10 GeV	W ® ev	9	0.5
Jet Trigger 2 TT > 4 GeV	ZH ® vvbb	2	0.5