



AFEII-t and TriP-t Status

Feb 10, 2005 PMG

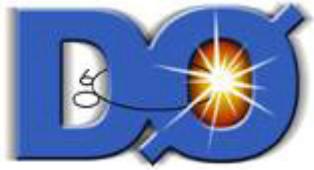
Paul Rubinov



AFEII-t and TriP-t Status

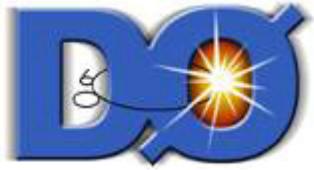
Long Story Made Short

- **TriP-t**
- **AFEII-t**
- **Schedule**



TriP-t testing

- **TriP-t testing is finally on a production footing.**
- **Needs:**
 - ◆ 5600 good chips (350 boards) = 62 trays = 12.5 boxes
 - ◆ Yield is around 80% so expect to test 16 boxes
 - ◆ Need to finish in 6 weeks so need to test ~3 boxes/week
 - ◆ Required yields are 72%
- **Not painless:**
 - ◆ Sockets getting dirty quickly
 - ◆ Alignment is delicate and needs attention when trays are changed
 - ◆ Will keep Leo off the streets for a while longer



TriP-t testing

- Philosophy: ok to mark good chips as marginal or bad, but only mark a chip good if SURE
- 1st box tested : 72% yield
 - ◆ 256 for the preproduction come from here
- 2nd box tested: 85% yield
 - ◆ Tweaked some TriP-t settings (made a big difference)
 - ◆ Tweaked some cuts (did not make a big difference)
- 3rd box partially tested.
 - ◆ Current rate ~0.5 box/day with only Leo checking the robot, swapping trays and sockets.



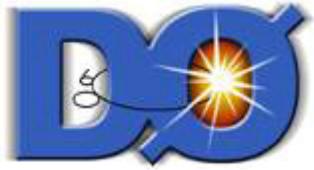
AFEII-t status

- **AFEII-t prototypes current status**
 - ◆ 9 of 10 boards working
 - ◆ 2.5 with production TriP-t (put on by hand)
 - ◆ Modified to look like pre-production boards
 - ◆ Many millions of events in test stands, Phase V, CTS, platform
- **The bottom line**
 - ◆ Bench testing of AFEII-t prototypes done
 - ◆ Next step testing pre-production boards
 - ◆ Platform testing / system integration ...



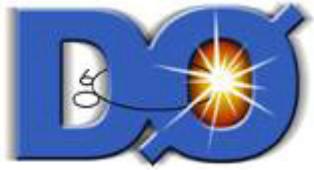
AFEII-t prototypes status

- Platform testing/system integration
 - ◆ “Platform test” plan endorsed by CFT operations:
CTS -> spare slot -> stereo slot -> axial slot
with each step required to proceed to next step
 - ◆ CTS test was ok
 - ◆ Spare slot test was ok
 - ◆ We got a unplanned “mini shutdown” of one week
 - Revealed readout errors on platform - we fixed these
 - Tested 6 slots with 5 boards - saw some issues in one slot after above fix but found work around
 - ◆ Stereo slot platform test attempted Feb 7th!



AFEII-t prototypes status

- Platform test Feb 7th
 - ◆ Not a success: 7% of events have readout errors
 - ◆ Otherwise AFEII-t looked fine
 - ◆ Serious problem because readout errors showed up only with beam
 - No errors during calibration run
 - No errors during LED run with or without zero suppression
 - No errors in any test stand with any seq or any cable tested so far
 - Looks like the same kind of cross talk we fixed during shutdown, but on a different bit



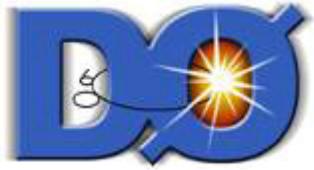
Schedule

- The big schedule slippage is **GONE** because TriP-t testing indicates
 - ◆ No need for second round of chip production
 - ◆ Currently ahead of the Nov PMG schedule
- Unfinished task
 - ◆ Finish testing of the TriP-t
 - ◆ Test and Certify pre-production boards
 - Current schedule calls for early March
 - ◆ Produce full set of 350 boards
 - Current schedule has finish mid May
 - ◆ Test boards
 - Current schedule has 11 weeks starting late April
 - ◆ Projected final milestone date 6/26/06



Schedule

- Unfinished tasks (continued)
 - ◆ 1.7.5.1.6 Pre-production Boards
 - About 1 week behind schedule
 - 1 week PCB delivery delay ... again
 - Platform Test
 - As promised in Nov, this is a multi-step test and is **REQUIRED** before full production
 - ◆ 1.7.5.2 Produce full board set
 - In schedule, 5 weeks plus 5 weeks, but expect rolling production with 3 week lag for PCB, 2 week lag for assembly.



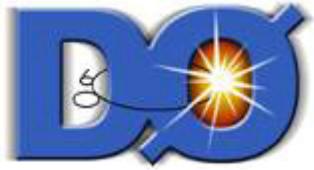
Schedule

- **Unfinished tasks (continued)**
 - ◆ **1.7.5.3 Board testing**
 - Required: produce 4 good boards per day
 - Goal: 6 to 8 boards tested per day
 - The time to implement any missed ECOs is key!
 - **3 Phase test:**
 - **Unpowered inspection and ECO phase (EED techs)**
 - 1 hour per board per person (assuming no significant ECOs!)
 - **Bench top tests EVERYTHING except cryo**
(highly automated, no special skills required: post docs, students)
 - 1 hour per board per test stand
 - **Phase V test stand for calibration and external injection test**
(some care required: techs, engineers...)
 - $\frac{1}{2}$ hour per board



Schedule

- **Concerns and issues**
 - ◆ Platform test is a tough milestone for Feb 27th
 - It is top priority above everything else!
 - Put off things that can be done during shutdown
 - ◆ Anticipate “certify for production” milestone by end of March.
 - ◆ Testing overlaps shutdown in May, tech availability of some concern. But backup available.
 - ◆ Management aware of this and planning jobs for key people accordingly (to maximize availability in May!)



Schedule

- **This box is from Nov PMG:**

- ◆ **Receiving & Final Assembly**

- Portions of effort of Curt Danner, Yolanda Echavarria
Paula Lippert, Lupe Rodriguez

- ◆ **Test Stands: Two-person Teams**

- ◆ **Bench-top Test Stands (3)**

- Tom Fitzpatrick & Bruce Merkel
- Kwame Bowie & Joshua Moua
- Victor Yakimchuk & Mikhail Kostin
- Alternate: Zonghan Shi

- ◆ **Combined Test Stand**

- Jadwiga Warchol & Dmitri Smirnov

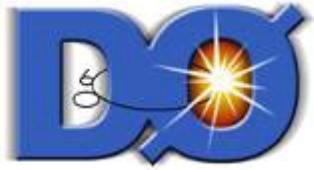
- **Backup plans: 3 students from Notre Dame**

- **Strong group from IIT (100% post doc, 100% tech, student)**



Conclusion

- Schedule looks ok
- TriP-t looks ok
- AFEII-t prototype boards look ok except...
- Bring on the AFEII-t preproduction!

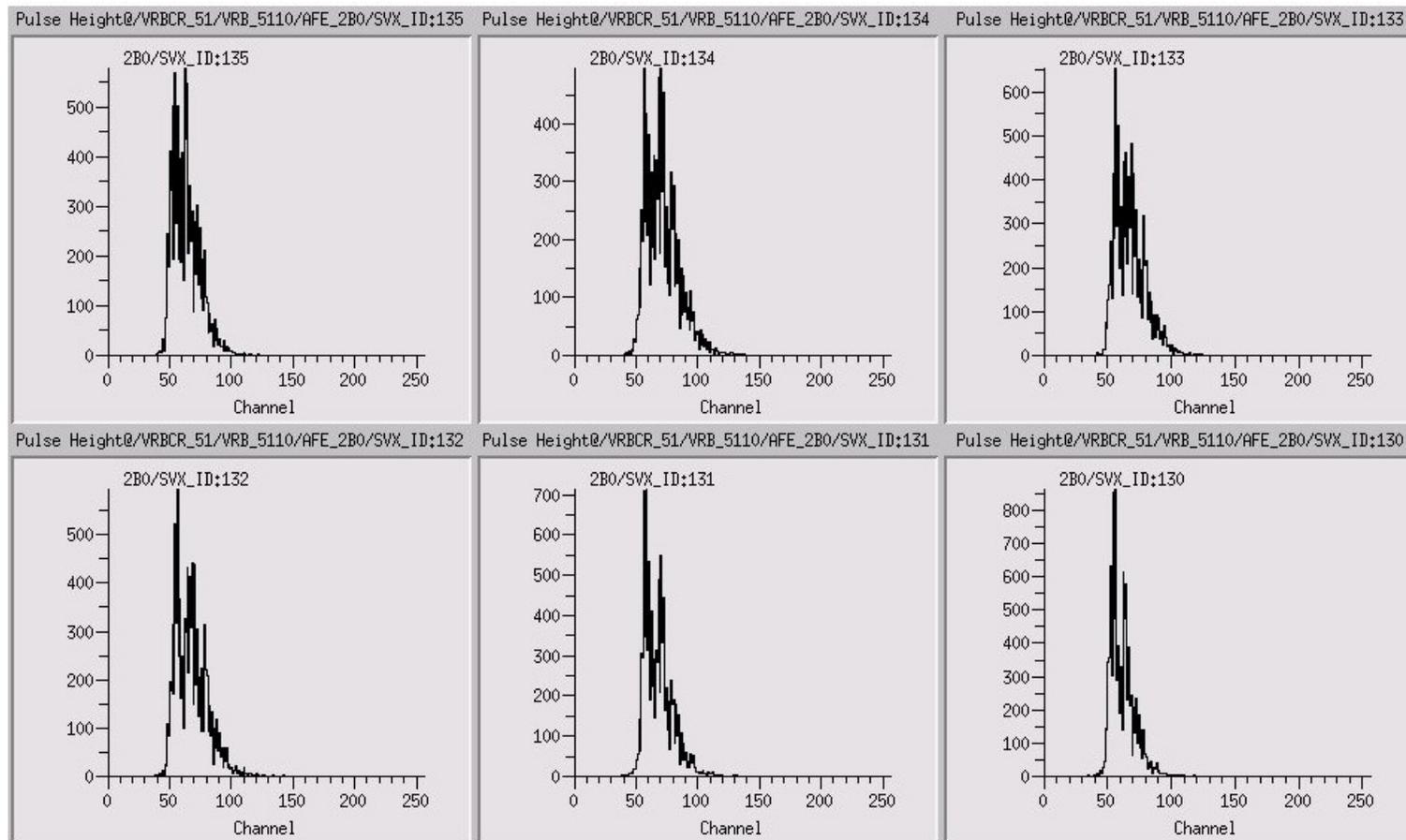


The following pages are
plots from the platform
test I do not have time
to show



AFEII-t

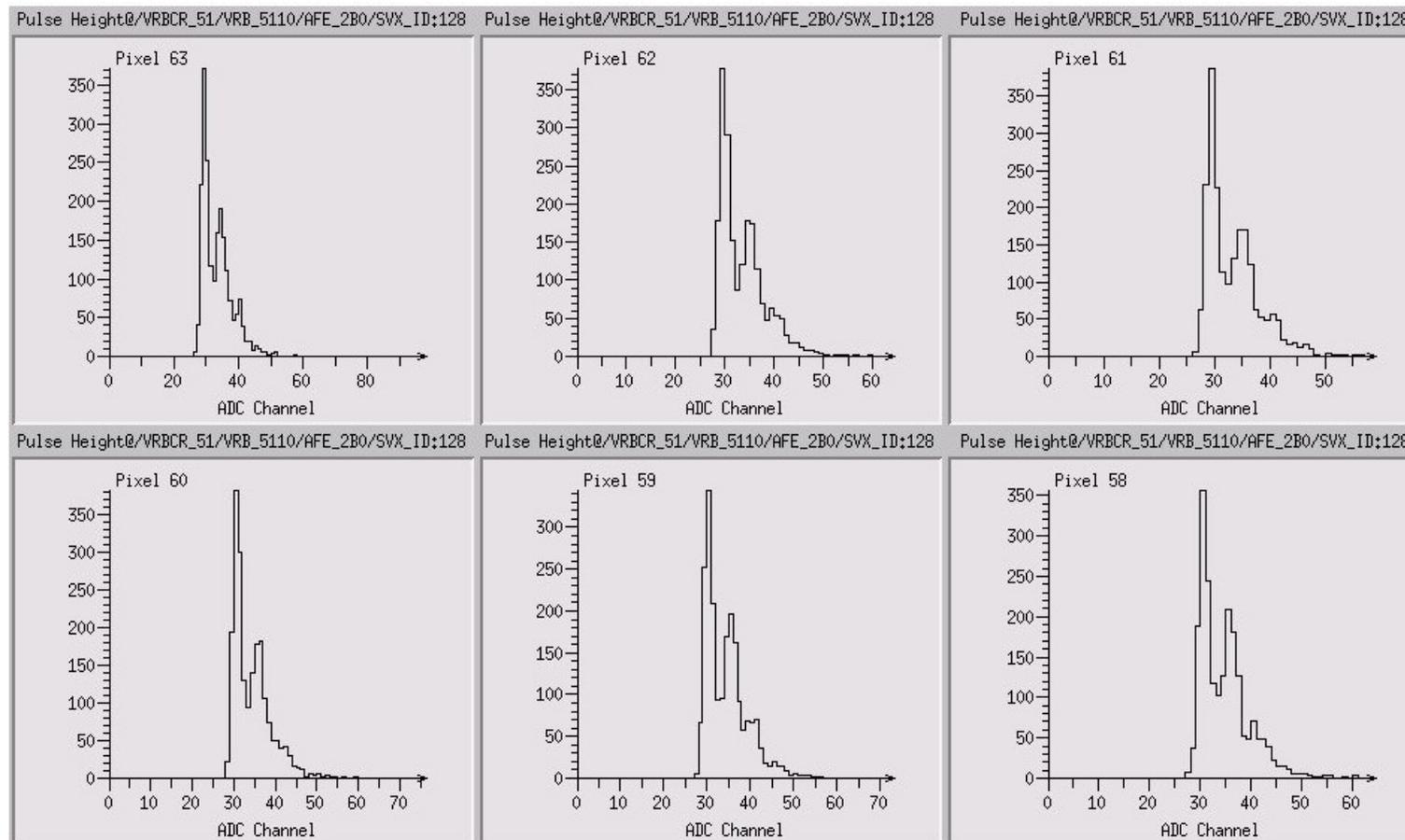
- Beam test results: AFE1





AFEII-t

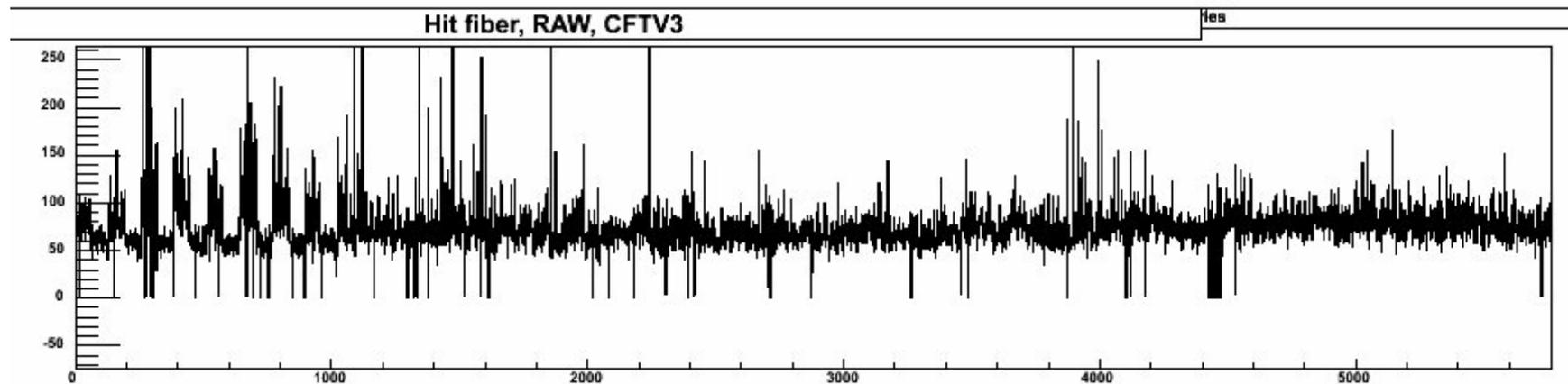
- Beam test results: AFEII





AFEII-t

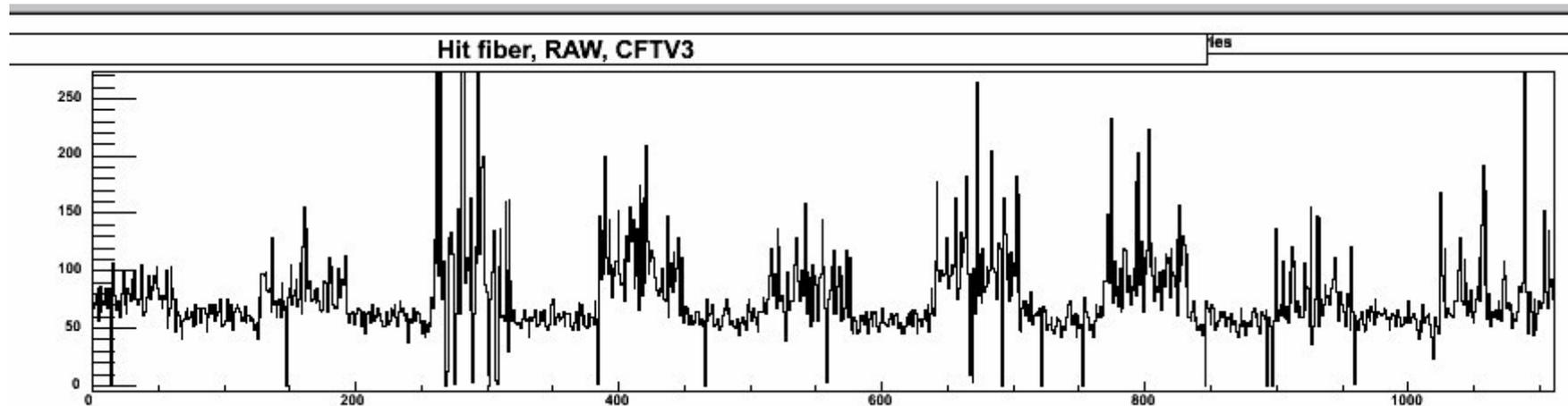
- Beam test results:
all fibers in one stereo layer.
Can you spot the AFEII fibers?





AFEII-t

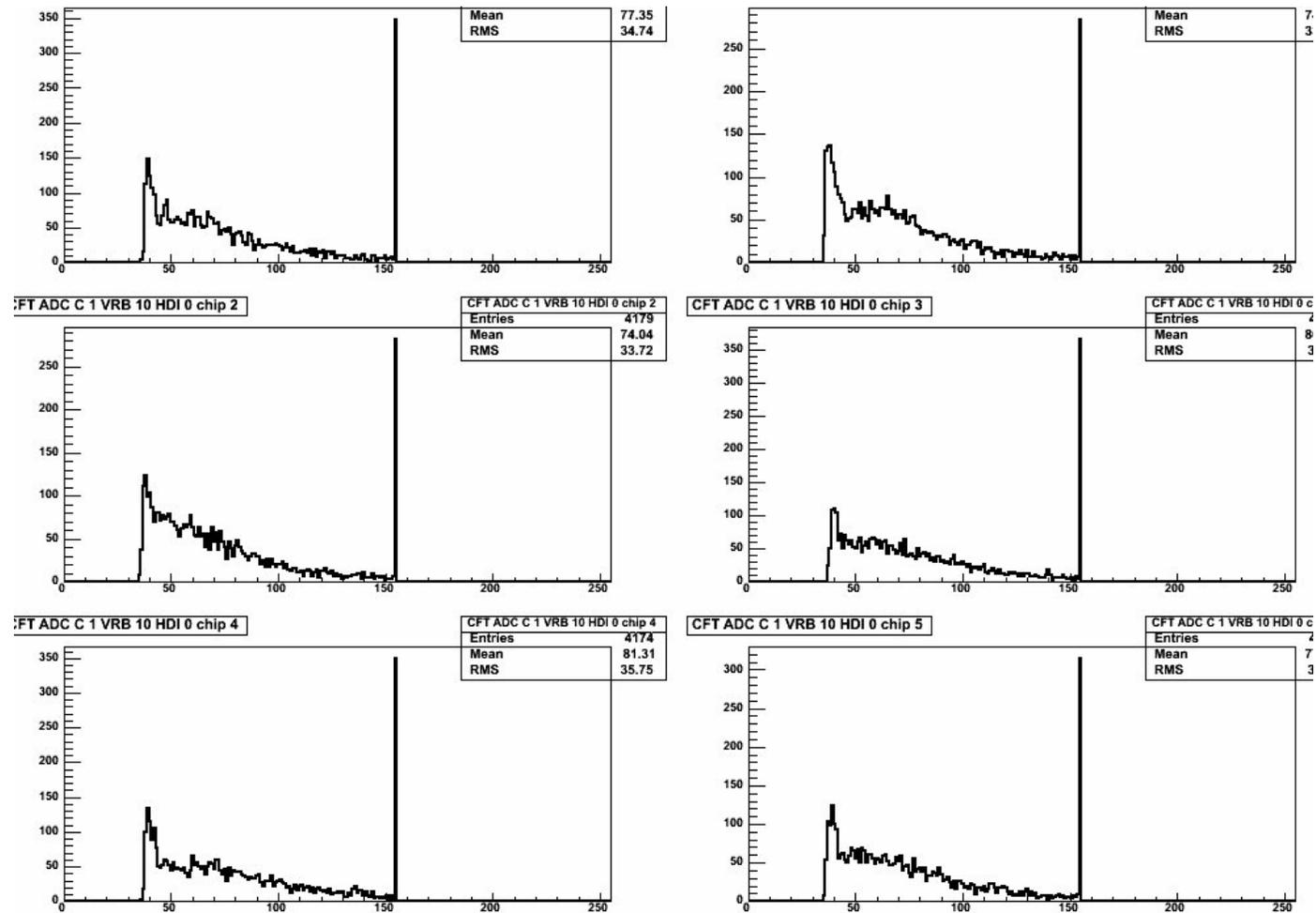
- Beam test results:

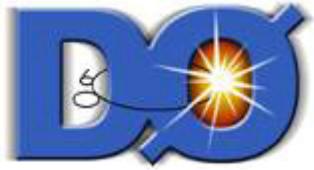




AFEII-t

- Beam test results:





AFEII-t

- Beam test results:

The rate of errors from the AFEII was approximately 2500 greater than all the AFE1 boards combined

