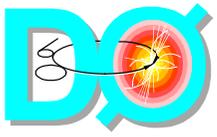


# The DØ Run 2b Trigger Upgrade

Darien Wood, Northeastern University,  
for the DØ collaboration

Fermilab PAC Meeting  
November 2, 2001



# Trigger Upgrades

## Prior to $L=5 \times 10^{32} \text{ cm}^{-1} \text{ s}^{-1}$

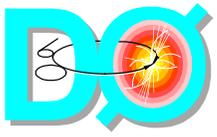
- ◆ SIFT replacement
- ◆ Level  $2\beta$
- ◆ Commercial DAQ system

## Preparation for $L=5 \times 10^{32} \text{ cm}^{-1} \text{ s}^{-1}$

- ◆ Level 1 Calorimeter Trigger upgrade ←
- ◆ Level 1 Track Trigger upgrade ←
- ◆ Level 1 Calorimeter-Track match ←
- ◆ Level 2 Silicon Track Trigger Upgrade
- ◆ Level  $2\beta$  Upgrade
- ◆ Online System

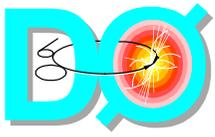
All described in Trigger CDR, but only underlined upgrades mentioned in this talk.





# Run 2b Trigger Upgrade Goals

- ◆ Critical need to upgrade trigger systems
  - » Increase trigger rejection to maintain existing rates with higher luminosity
  - » Ensure efficient triggering for full range of Higgs channels
- ◆ Biggest challenges at Level 1
  - » Input rate to Level 2 limited to 5 kHz (readout time)
  - » Need to get the events to level 2, where more handles are available (Silicon Track Trigger)
- ◆ Level 2 trigger rate limited to 1.8 kHz by calorimeter readout
- ◆ High  $p_T$  triggers expected to exceed these limits in Run 2b
- ◆ Need to increase trigger rejection, particularly at Level 1
  - » L1 Calorimeter trigger upgrade to sharpen thresholds
  - » L1 Tracking trigger upgrade to maintain rejection
  - » L2/L3 Processor upgrades

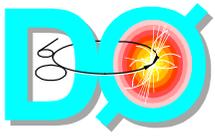


# Run 2b Trigger Task Force

- Run 2b Trigger Task Force in place Mon, 6/25/01:
  - Co-Chairs: M. Hildreth (Notre Dame), R. Partridge (Brown U)
- ◆ Calorimeter
  - » M. Abolins (MSU)
  - » D. Baden (UMaryland)
  - » B. Kehoe (MSU)
  - » P. Le Du (Saclay)
  - » E. Perez (Saclay)
  - » M. Tuts\* (Columbia)
  - » V. Zutshi (BNL)
- ◆ Technical/Hardware
  - » D. Edmunds (MSU)
  - » M. Johnson\* (Fermilab)
  - » J. Linnemann (MSU)
  - » D. Schamberger (Stony Brook)
- ◆ Tracking
  - » B. Abbott (UOklahoma)
  - » D. Alton (UMichigan)
  - » V. Bhatnagar (Orsay)
  - » F. Borcharding (Fermilab)
  - » S. Chopra (BNL)
  - » F. Filthaut (UNijmegen)
  - » Y. Gerstein (Brown U)
  - » G. Ginther\* (URochester)
  - » P. Petroff (Orsay)
- ◆ Muon
  - » J. Butler (Boston U)
  - » K. Johns\* (UArizona)

\* = Sub-Group Chair





# Trigger Task Force

(cont'd)

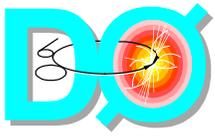
## ◆ Task Force Charge:

- » Develop plan for Run 2b trigger system that allows D0 to run at 132 nsec & lum 5E32 with output rates:
  - Level 1: 5 kHz
  - Level 2: 1 kHz
  - Level 3: 50 Hz
- » Installed in summer 2004
- » Reasonable cost, technical resources, development & production time, low impact on existing detector, infrastructure:
  - No tracker replacement, limited cable plant replacement, limit number additional crates in MCH, ...

## ◆ Conceptual Design Proposal submitted to Run 2b Project Mgr by Sep 17, 2001

- » Given tight time constraints (3 months):
  - Focus on high-pT physics program, Higgs search
  - Estimate rates, rejection for various options (simulation)
    - ◆ Level 1 calorimeter, track match, singlets/doublets, CFT stereo,...
  - Focus on Level 1
    - ◆ Feasibility arguments for Levels 2,3 may be sufficient





# DØ Trigger Architecture

## ◆ Level 1

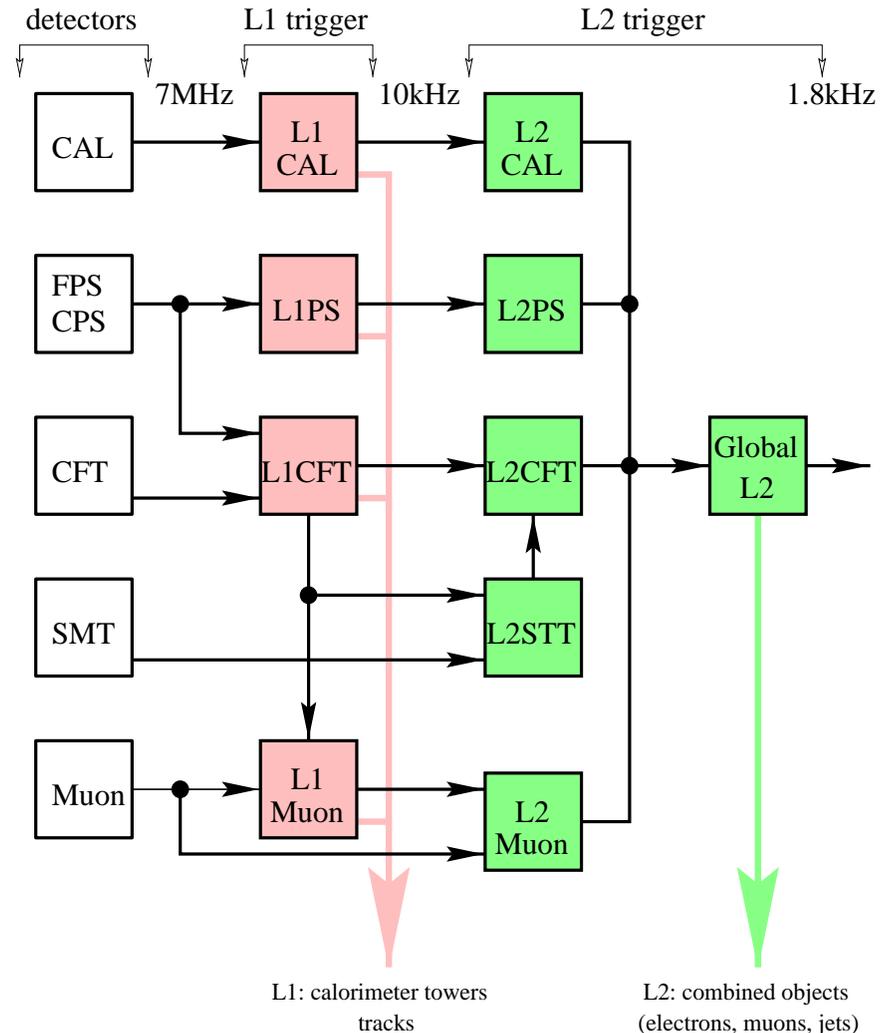
- » Calorimeter trigger
- » Fiber tracker trigger
- » Preshower (e/γ) trigger
- » Muon trigger

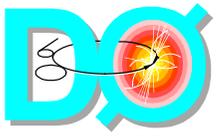
## ◆ Level 2

- » Silicon track trigger
- » Introduce Correlations, Refine Level 1 decision

## ◆ Level 3

- » Full event information available
- » Farm of high-performance computing nodes

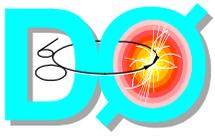




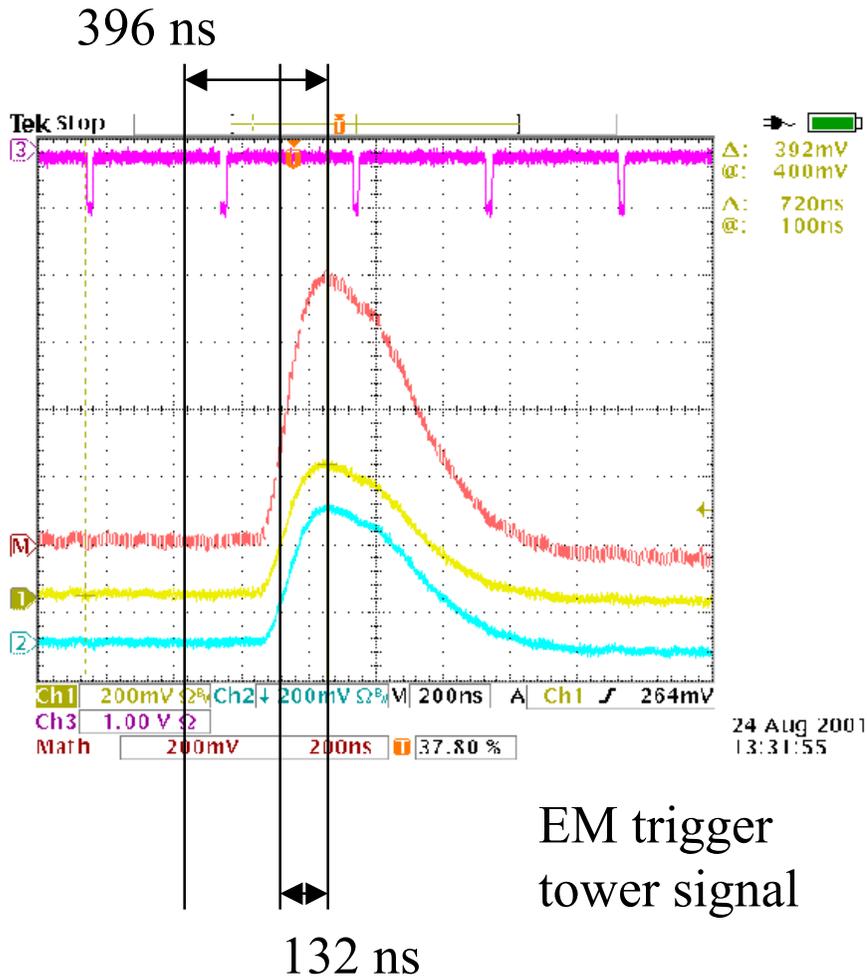
# Sample run 2b Trigger rates

- ◆  $5 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$ , assuming no trigger upgrades
- ◆ High  $p_T$  trigger menu exceeds available bandwidth

Trigger	Physics	Level 1 rate (kHz)
EM tower $> 10$ GeV	$W \rightarrow e \nu$	5
2 Tracks ( $> 10$ & $5$ GeV) + isolation + EM $> 2$ GeV	$H \rightarrow \tau^+ \tau^-$	10
2 Had+EM towers, sum $> 4$ GeV	$ZH \rightarrow \nu \bar{\nu} b \bar{b}$	2

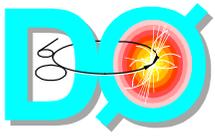


# Calorimeter Trigger Upgrade



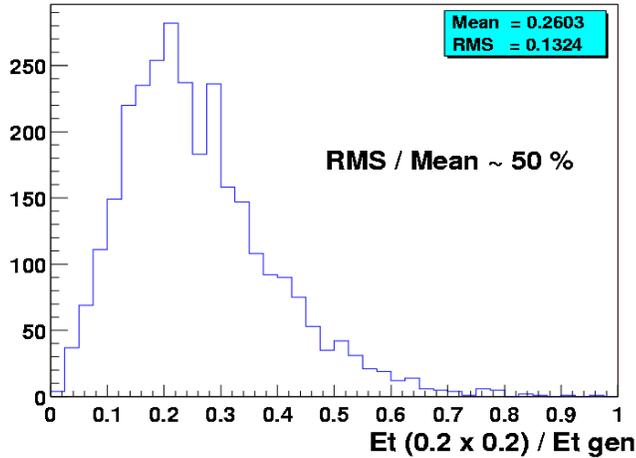
- ◆ Introduce digital filter on trigger tower signals
- ◆ Suppress pile-up effects
- ◆ Improve energy resolution
- ◆ Avoid triggering on wrong crossing (signal rise time  $> 132$  ns)
  - » Sample at peak to avoid timing variations
  - » Previous crossing will often be above threshold
  - » It would be the highest energy events (most interesting) which are mis-assigned



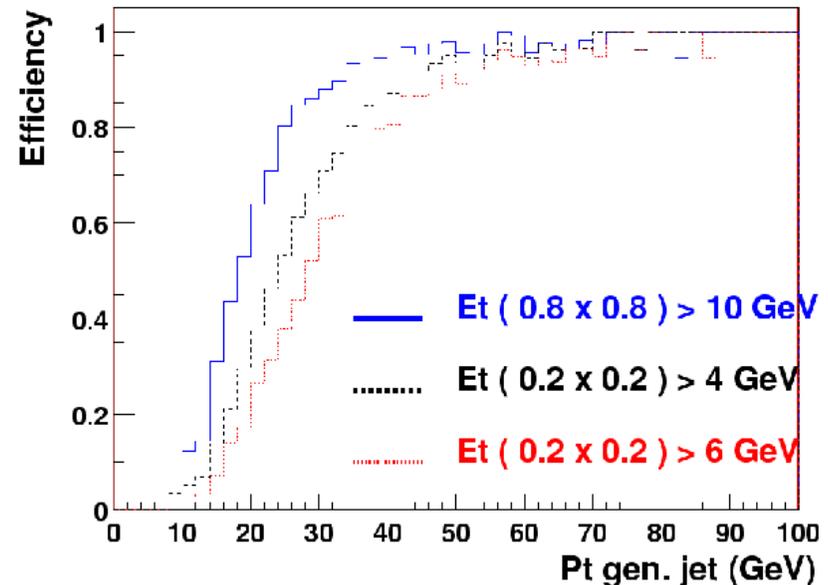
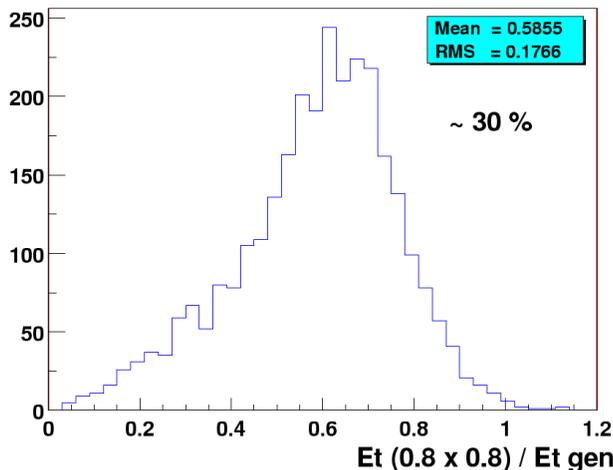


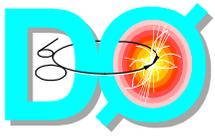
# Calorimeter Trigger Upgrade

- ◆ Sharpen thresholds by introducing EM, Jet clustering



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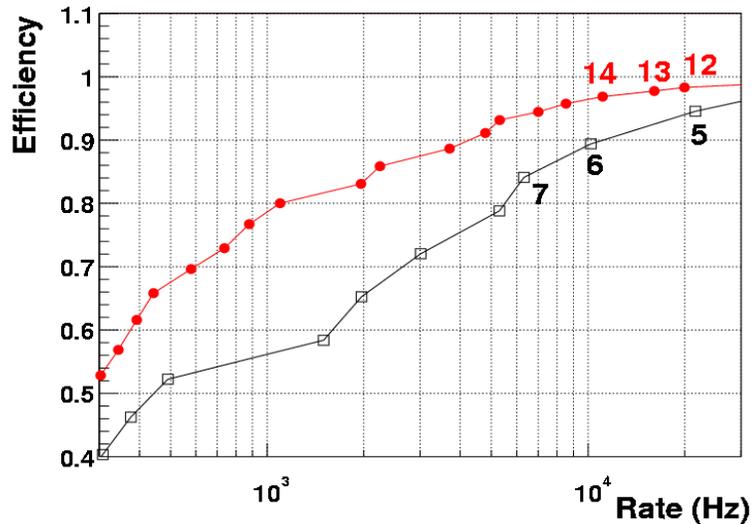




# Calorimeter Trigger Upgrade

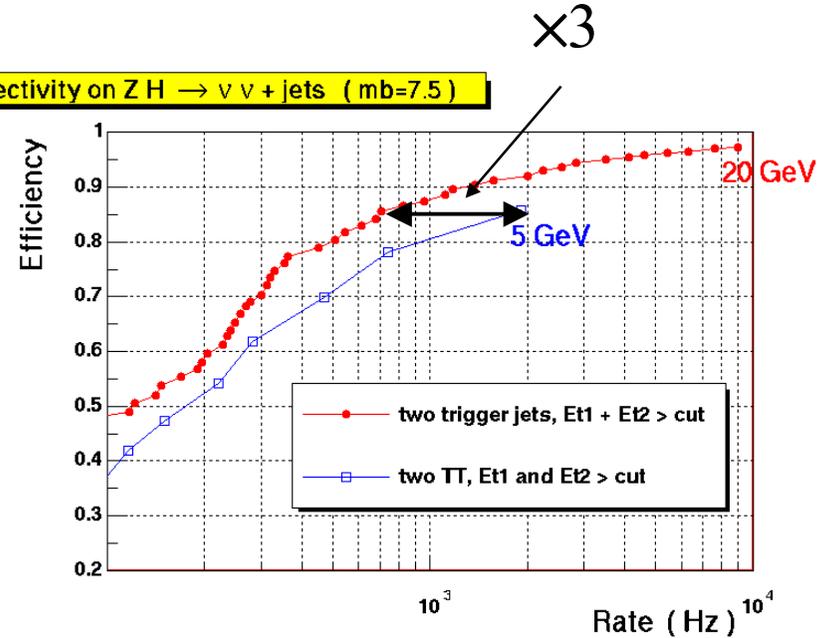
- ◆ Rate improvements from cluster thresholds vs. tower thresholds

Selectivity for  $P_{\text{that}} > 40 \text{ GeV}$ ,  $\text{mb} = 5$



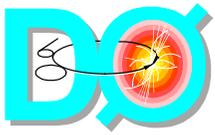
Single jet

Selectivity on  $ZH \rightarrow \nu\nu + \text{jets}$  ( $\text{mb}=7.5$ )



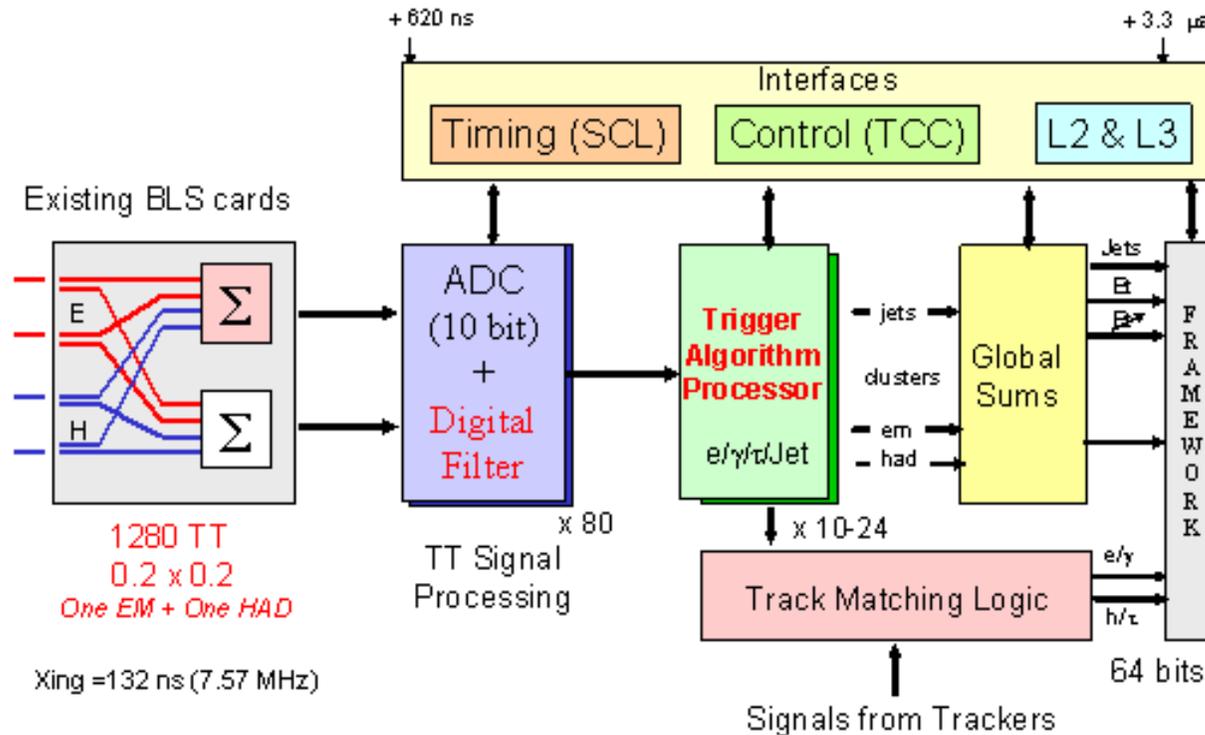
$ZH \rightarrow \nu\nu b\bar{b}$

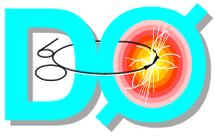




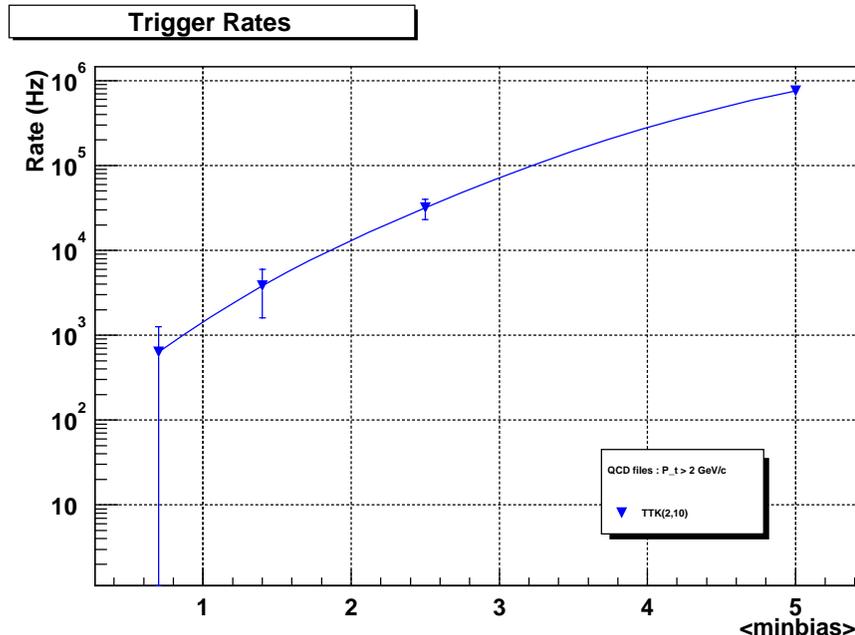
# Calorimeter Trigger Upgrade

- ◆ Clustering algorithm gets implemented in FPGA's
- ◆ Similar to ATLAS sliding-window algorithm



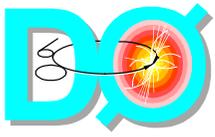


# Tracking Trigger Upgrades

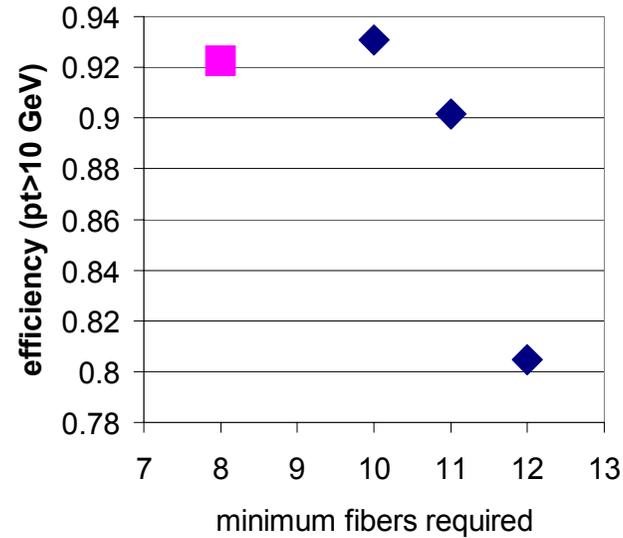
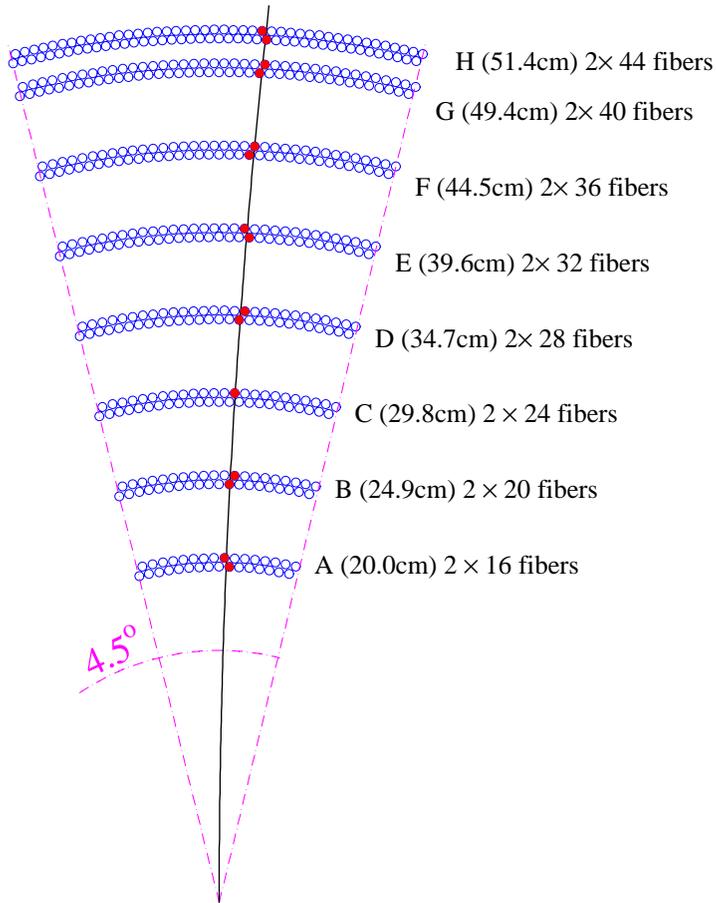


- ◆ Level 1 Central Track Trigger (CTT) essential for electrons, muons, taus (WH→lvjj)
- ◆ Tracking trigger rates sensitive to occupancy
- ◆ Upgrade proposal:
  - » Narrow tracker roads by using individual fiber hits (singlets) rather than pairing adjacent fibers (doublets)
  - » Cal-track matching

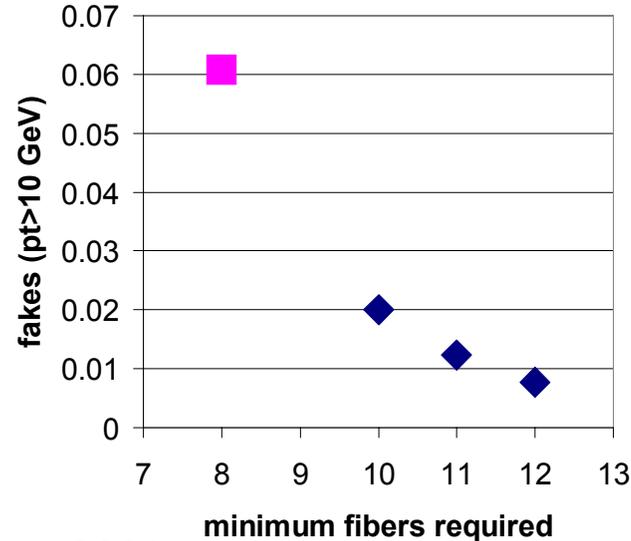


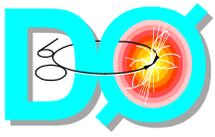


# Tracking Trigger Upgrades



5 min. bias events

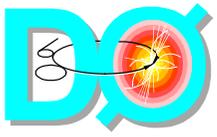




# Review of SIFT Replacement

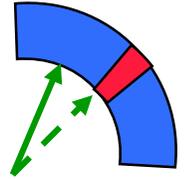
- ◆ Fiber Tracker Trigger Chip (SIFT) must be replaced for 132 nsec running
  - » Required 50-70 nsec charge collection times result in inefficiencies with current chip at 132 nsec
  - » Costly, some technical challenges
- ◆ Review of design, implementation: September 25, 2001
- ◆ Committee consisted of 2 D0 physicists, 3 non-D0 engineers:
  - » M. Bowden, V. Buescher, M. Larwill, R. Lipton (chair), V. Pavlicek
- ◆ Findings:
  - » Endorse overall design
    - With caveat that many details remain
  - » Performance should equal that of present chip at 396 nsec
  - » Recommend option that includes AFE board replacement
  - » If single ASIC submission, schedule reasonable for November '02 changeover to 132 nsec
  - » For dual submission, schedule tight, assuming changeover remains on above schedule
- ◆ Firm schedule for 132 nsec changeover not yet established

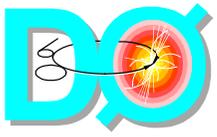




# Calorimeter Track matching

- ◆ Present calorimeter trigger allows calorimeter-track matching only by quadrant in azimuth
- ◆ Upgrade L1 Cal trigger would provide calorimeter matching information with 8 times finer granularity
- ◆ Additional factor of  $\sim 2$  in background rejection for electron triggers (confirming EM clusters with high- $p_T$  tracks)
- ◆ Additional factor of  $\sim 3$  in background rejection for tau's (confirming high- $p_T$  isolated tracks with EM+had energy)
- ◆ Modest extension to proposed calorimeter trigger upgrade
  - » Can use same hardware (Muon Trigger Cards) that presently does Level 1 muon-CTT match
  - » Can possibly just send CTT information to last stage of Level 1 calorimeter algorithm boards



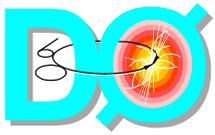


# Limited scope

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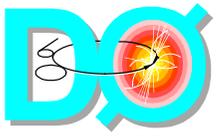
- ◆ Studied and eliminated several upgrade options in favor of lower schedule-risk and/or cost:
  - » Level 1 stereo tracking
  - » Preshower as 9<sup>th</sup> tracking layer
  - » Finer granularity of calorimeter towers (0.1x0.2)
- ◆ Studying use of existing hardware for new applications
  - » Muon Trigger Cards for calorimeter-track matching
  - » Tracker Digital Front Ends (DFE) for calorimeter cluster algorithms
  - » Existing DFE motherboards with daughter board replacement for tracking upgrade





## Additional features

- ◆ Muon triggers – No change needed to muon trigger system, but most muon triggers would gain rejection from upgrade of the CTT FPGA's.
- ◆ Global calorimeter sums – better missing  $E_T$  with incorporation of intercryostat detector and massless gaps
- ◆ EM shape and isolation – these cuts can be implemented in Level 1 after cluster finding, giving an additional factor of 2 rejection for electron & photon triggers
- ◆ Topology – flexibility to require acoplanar jets, etc.
- ◆ Flexibility: New clustering and tracking algorithms can be implemented with FPGA downloads

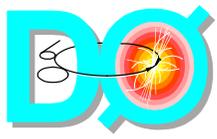


# Level 1 Trigger rates comparison

◆  $L = 5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$

Trigger	Physics	Level 1 rate, no upgrades (kHz)	Level 1 rate, w/ upgrades (kHz)
EM tower > 10 GeV	$W \rightarrow e \nu$	5	0.3 (track matching, 16-layer, EM fraction)
2 Tracks (>10 & 5 GeV) + isolation + EM > 2 GeV	$H \rightarrow \tau^+ \tau^-$	10	1 (calorimeter matching)
2 Had+EM towers, sum > 4 GeV	$ZH \rightarrow \nu \bar{\nu} b \bar{b}$	2	0.6 (calorimeter clustering)





# Costs

(Intend to submit trigger MRI this Winter)

## Level 1 calorimeter upgrade

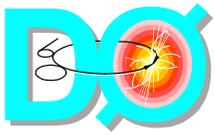
Item/process	Unit Cost (\$)	# Require	Total Cost (\$k)	Total Cost + 100% Contingency
<b>ADC/digital filter system</b>				
ADC/filter cards	3500	105	368	
Crates & power supplies	7100	8	57	
Controller cards	2000	8	16	
VME masters	2300	10	23	
<i>Subtotal</i>			<i>464</i>	<i>928</i>
<b>Digital Algorithm System</b>				
Trigger algorithm cards	7500	30	225	
Crates & power supplies	3000	3	9	
Controller cards	500	4	2	
<i>Subtotal</i>			<i>236</i>	<i>472</i>
LVDS cables	75	350	26	52
<i>TOTAL</i>			<i>\$726</i>	<i>\$1,452</i>

## Level 1 tracking upgrade

Item/process	Unit Cost (\$)	# Require	Total Cost (\$k)	Total Cost + 50% Contingency (\$k)
Fabricate Daughter Boards	500	88	44	66
Purchase new FPGA	900	350	315	473
<i>TOTAL</i>			<i>\$360</i>	<i>\$540</i>

Item/process	Unit Cost (\$)	# Require	Total Cost (\$k)	Total Cost + 50% Contingency (\$k)
Mu Trig Cards	3300	9	30	45
Serial Link Daughters	100	256	26	39
Crates, cables, etc.	44000	1	44	66
<i>TOTAL</i>			<i>\$100</i>	<i>\$150</i>





# Schedules & Manpower

## calorimeter

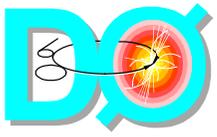
Milestone date	Task
03/02	Performance specification defined, major design choices made
08/02	Prototype design complete
12/02	Prototyping complete (ADC, TAP,...)
06/03	Prototype testing complete
09/03	Preproduction complete
12/03	Preproduction testing complete
06/04	Production complete, testing begins
07/04	Installation & commissioning starts
01/05	Commissioning complete

## tracking

Prototype algorithm coded and simulated using FPGA simulation tools	2/02
Target algorithm coded and simulated using FPGA simulation tools	6/02
Prototype boards delivered	1/03
Production boards delivered	10/03
Daughter boards tested and ready for installation	4/04

- Fully loaded schedule under preparation to estimate manpower
- Large project
- Many groups in the collaboration have expressed interest in participating, and have resources becoming available (engineering, technicians, physics):
  - Saclay, LAL Orsay, Paris VI, MSU, Columbia/Nevis, Arizona, Boston, Northeastern, Notre Dame, Manchester,...

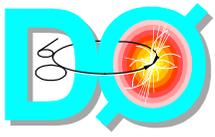




# Level 2 Trigger

- ◆ Silicon Track Trigger
  - » Vital for triggering on b-quarks
    - $ZH \rightarrow \nu\nu b\bar{b}$
    - $Z \rightarrow b\bar{b}$  (top mass jet energy scale)
  - » Upgrade needed to accommodate design of new silicon detector
  - » Most efficient to include additional modules in early '02 production
- ◆ Level 2  $\beta$  processors
  - » Replace unreliable alpha processors
  - » Add additional processing power for higher Run2b luminosity





# Conclusions

- ◆ Upgrades needed at level 1 to cope with:
  - » need for increased rejection at level 1
  - » Controlling rates even with multiple interactions
  - » Triggering on correct beam crossing at 132 ns
- ◆ Since last PAC meeting, extensive study of triggering options has been completed, resulting in a conceptual design for calorimeter and tracking upgrades
  - » Scope has been limited due to constraints in schedule, manpower, and costs
  - » Design offer considerable flexibility to deal with unanticipated physics requirements
  - » We are ready to begin the detailed design and assemble the project
- ◆ We request Stage 1 approval for the trigger upgrades

