



# ‘DØ Run 2b Silicon Tracker’

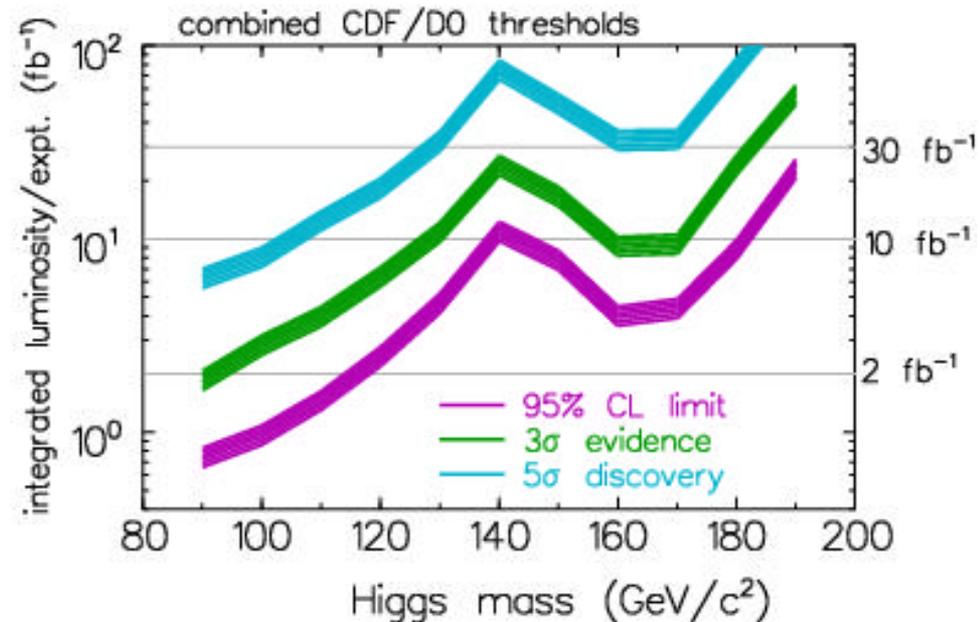
Fermilab PAC Meeting  
November 2-4, 2001

Marcel Demarteau  
Fermilab

For the Run 2b Silicon Group

# Run 2b

- ❑ Although we just built a major silicon detector and are still commissioning it (and the rest of the detector), a new silicon detector is planned; major undertaking.
- ❑ Current silicon detector designed for  $\sim 2 \text{ fb}^{-1}$ ; will most likely survive 4-5  $\text{fb}^{-1}$ 
  - The most appropriate rad-hard technology used at that time
- ❑ Laboratory:
  - Supports extended running to  $\sim 15 \text{ fb}^{-1} / \text{exp}$
  - Asked both collaborations to study replacement options
    - » Choice of exp's is full replacement
  - Suggested a time scale and budget
  - Asked for TDR's by Oct '01



- ❑ The Higgs search is the highest priority of the laboratory and perhaps of the field, and given the stringent time frame set by the turn-on of the LHC at CERN, a clear consensus regarding the scope of the project needs to be obtained now

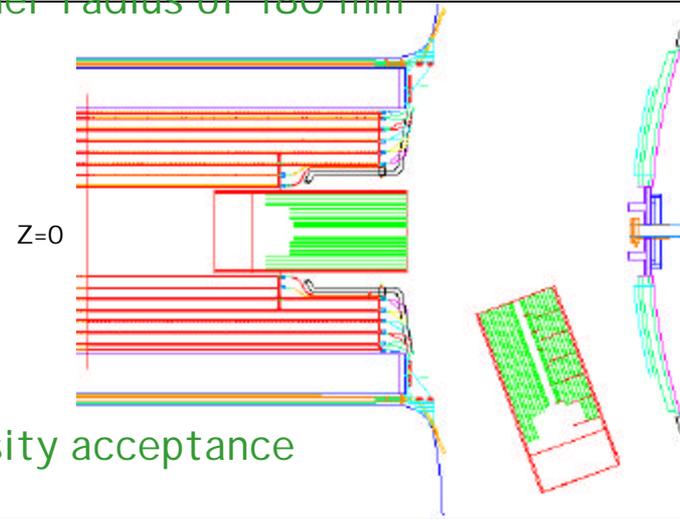
# Outline

- ❑ Overview of TDR design
  - Boundary Conditions for full replacement
    - » Space constraints
    - » Luminous region
    - » DAQ constraints
    - » Radiation damage
    - » Silicon Track Trigger
  - Design considerations
  - Design choices
    - » Layer 0, Layer 1
    - » Layer 2-5
    - » Hybrids and readout
- ❑ Organization
- ❑ Cost
- ❑ Resources
- ❑ Schedule

# Boundary Conditions

## □ Spatial

- Installation within existing fiber tracker, with inner radius of 180 mm
- Full tracking coverage
  - » Fiber tracker up to  $|\eta| < 1.6$
  - » Silicon stand-alone up to  $|\eta| < 2.0$
- Installation in collision hall
  - » Tracker will be built in two independent half-modules, split at  $z=0$



## □ Luminous Region

- Length of inner layer 96 cm, on plateau of luminosity acceptance

## □ Data Acquisition

- Retain readout system downstream of adapter card
- Current cable plant allows for ~912 readout modules
- Total number of readout modules cannot exceed 912

## □ Radiation Damage

- Limit  $V_{\text{depl}}$  to ~700V after  $15 \text{ fb}^{-1}$ , and minimize  $I_{\text{leak}}$  for innermost radii
- Requires silicon operating temperature of  $-10^\circ \text{ C}$ , off-board electronics for innermost layer

## □ Silicon Track Trigger

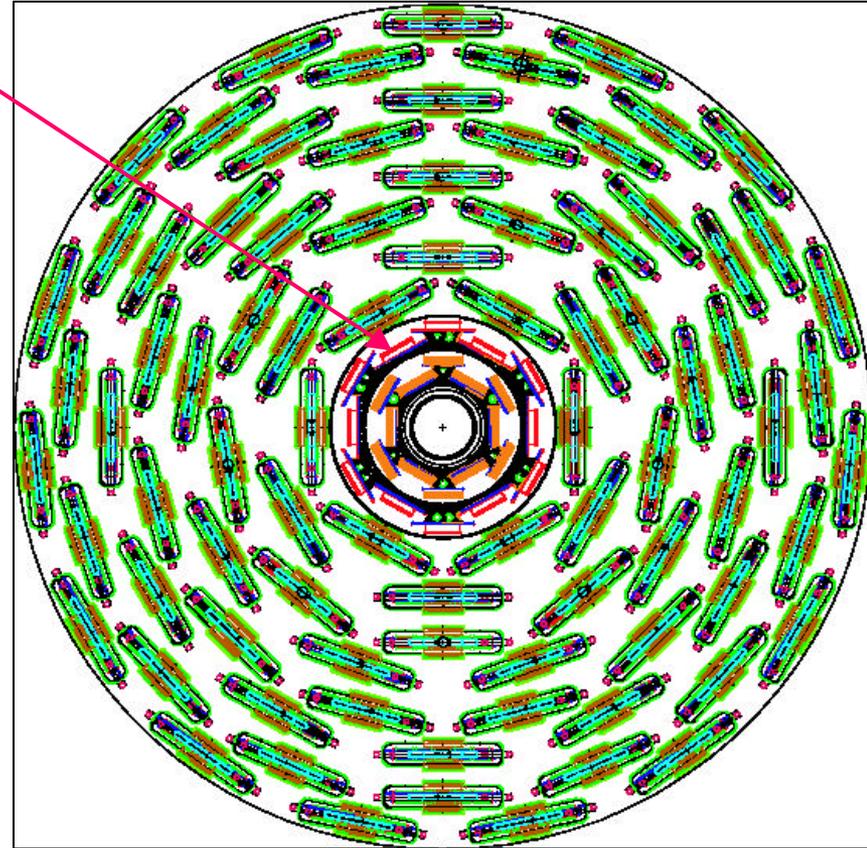
- Respect 6-fold symmetry

# Design Considerations

- ❑ Do not compromise on the performance of the Run2a silicon tracker
- ❑ Choose design adequate to achieve physics goals (no 90-degree stereo), but do not over-design
- ❑ Provide stand-alone tracking up to  $|\eta| < 2.0$
- ❑ Modular design, minimize the number of different elements
- ❑ Use established technologies
- ❑ Divide tracker in two radial groups:
  - Inner layers
    - » Design to withstand integrated luminosity of  $15 \text{ fb}^{-1}$ , with adequate margin
    - » Provide path for possible replacement of only innermost or both inner layers
  - Outer layers
    - » Design to last a long time

# Design Choices

- ❑ Six layer silicon tracker, divided in two radial groups
  - Inner layers: Layers 0 and 1
    - » Axial readout only
    - » Mounted on integrated support
    - » Assembled into one unit
    - » Designed for  $V_{\text{bias}}$  up to 1000 V
  - Outer layers: Layers 2-5
    - » Axial and stereo readout
    - » Stave support structure
    - » Designed for  $V_{\text{bias}}$  up to 300 V
- ❑ Employ single sided silicon only, 3 sensor types
  - 2-chip wide for Layer 0
  - 3-chip wide for Layer 1
  - 5-chip wide for Layers 2-5
- ❑ No element supported from the beampipe
- ❑ Drilled Be Beampipe with I D of 0.96", 500 $\mu\text{m}$  wall thickness



# Design Choices

## ❑ Sensor lengths

- Inner layers: 79.4 mm, 6 sensors per half-module
- Outer layers: 100 mm, 5 or 6 sensors per half-module

## ❑ Longitudinal segmentation

	Z=0																Z (mm)			
	0	40	80	120	160	200	240	280	320	360	400	440	480	520	560	600				
Layer 0			S		S		S		S		S		S							
Layer 1			1/2D	1/2D			1/2D	1/2D			1/2D	1/2D								
Layer 2				1/2D	1/2D				1/2D	1/2D										
Layer 3				1/2D	1/2D				1/2D	1/2D										
Layer 4				1/2D	1/2D						1/2D	1/2D								
Layer 5				1/2D	1/2D						1/2D	1/2D								

### ➤ Indicating readout by length of readout segment:

- » L0, L1: each sensor readout
- » L2, L3: 10-10-10-20 readout
- » L4, L5: 10-10-20-20 readout

### ➤ Governed by:

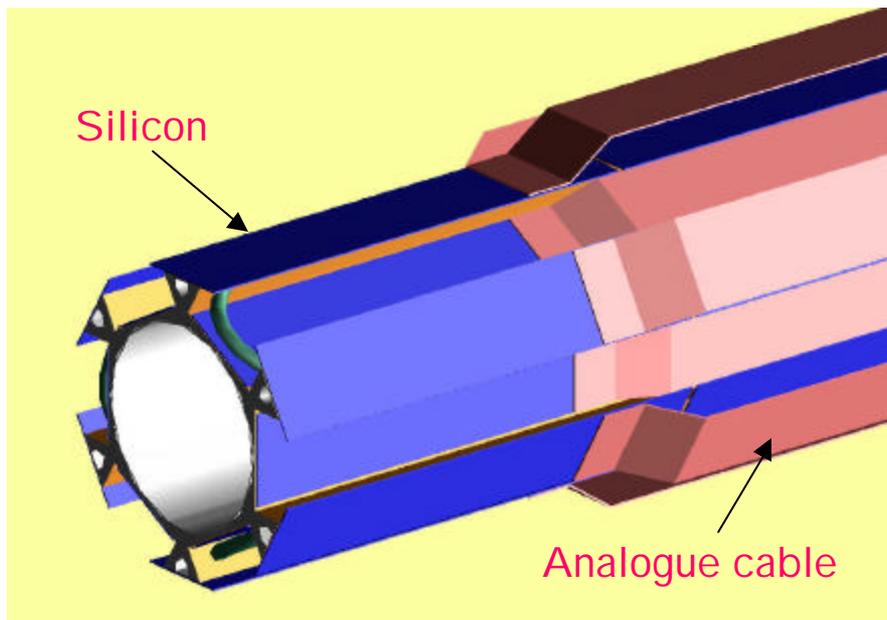
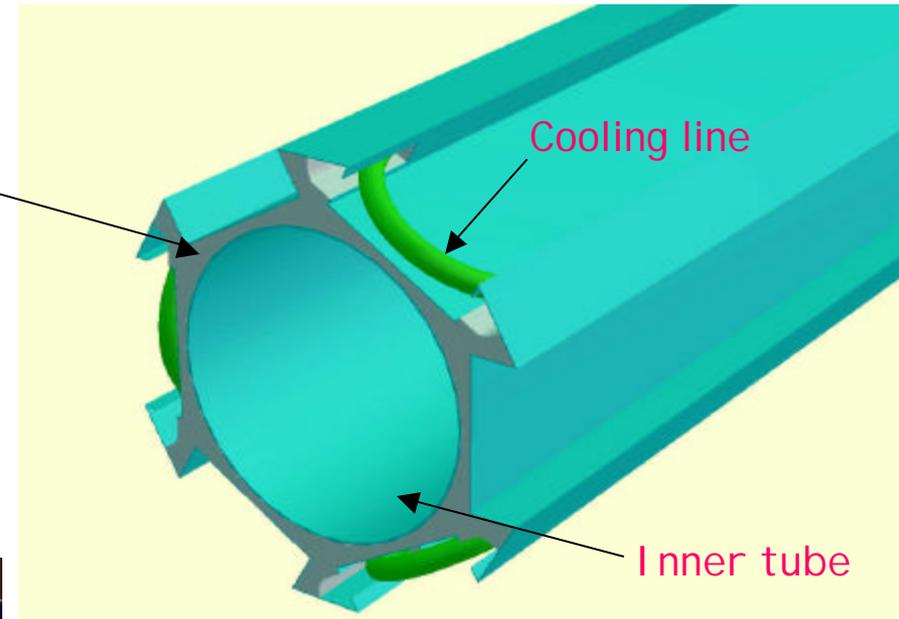
- » Number of allowed readout cables
- » Occupancy, cluster sharing

## ❑ Hybrids are double-ended, i.e service out two readout segments, indicated by the length of the respective readout segments: 10-10, 10-20, 20-20

# Layer 0

## Support Structure

- 12-fold crenellated geometry
- carbon fiber lined carbon foam
- Integrated cooling
- $R_{in} = 18.5 \text{ mm}$

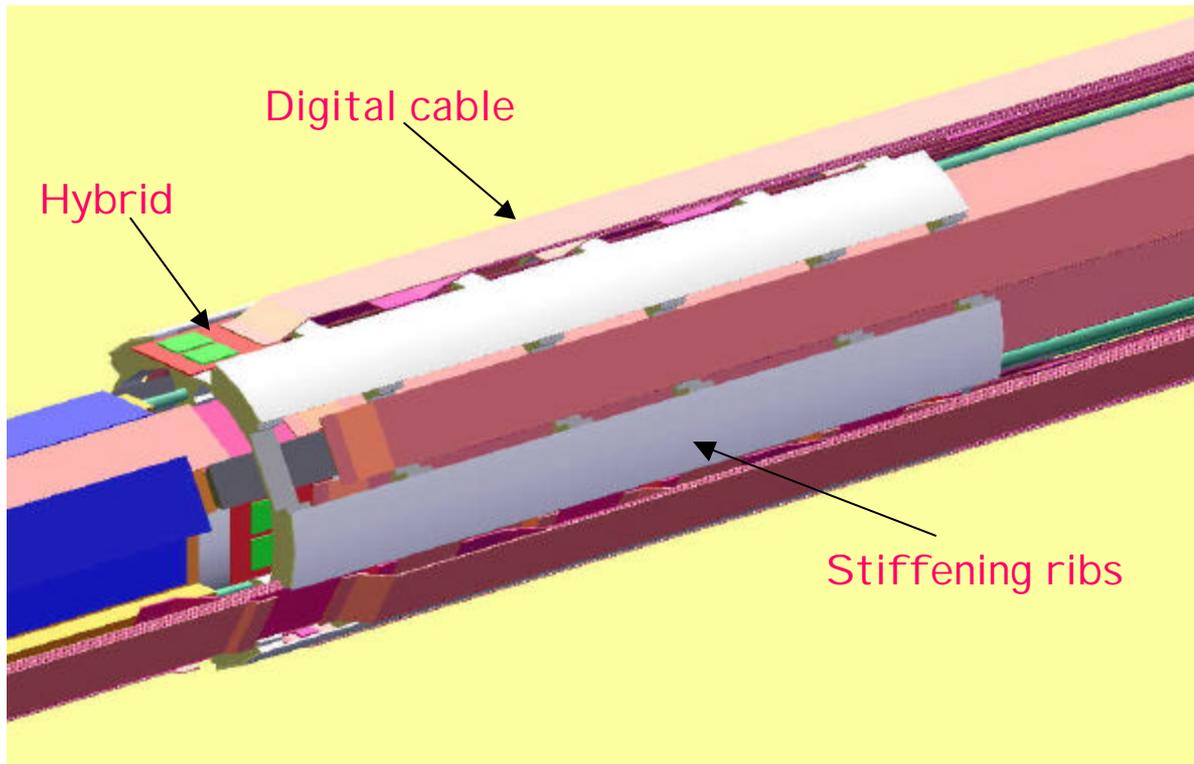


## Assembly

- 2-chip wide sensors
- $25 \mu\text{m}$  pitch,  $50 \mu\text{m}$  readout
- Analogue cables for readout
- Hybrids off-board

# Layer 0

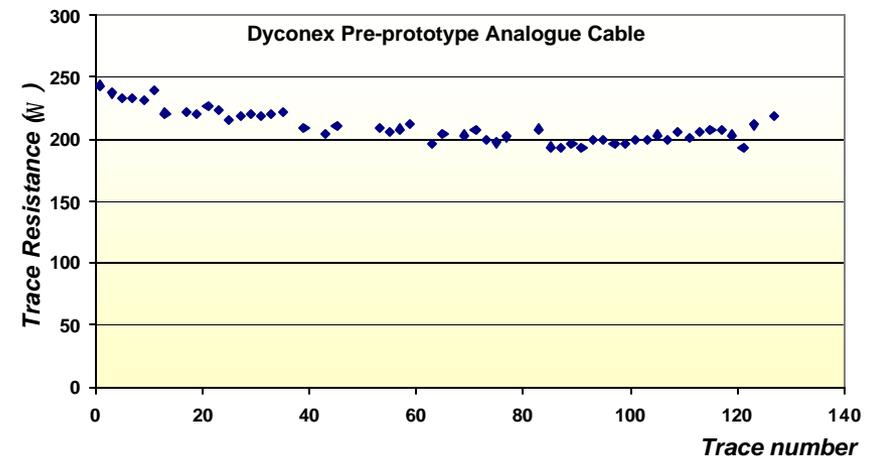
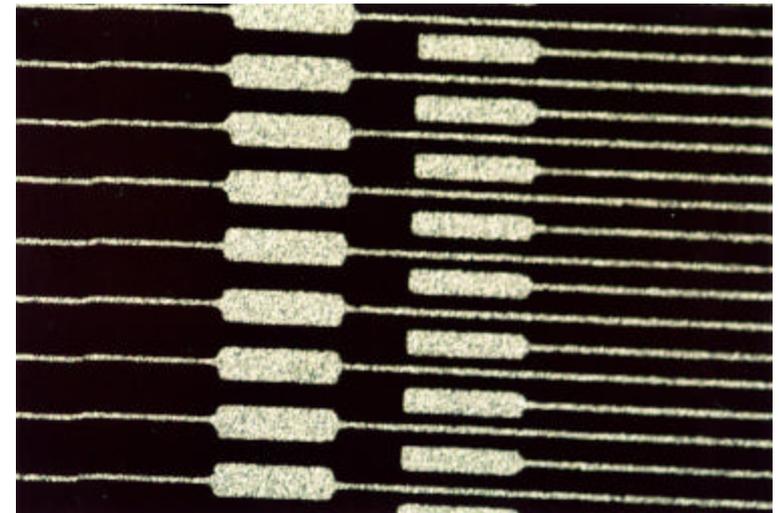
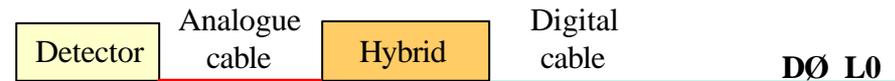
- ❑ Hybrids are off board
  - Analogue cables carry signals
  - 2-chip hybrids
  - Staggered in z for 6 readouts per end per phi-sector
- ❑ Space is extremely tight !



- ❑ Six support rings
  - Holds hybrids
  - Provides heat flow path
- ❑ Six stiffening ribs

# Analogue Flex Cables

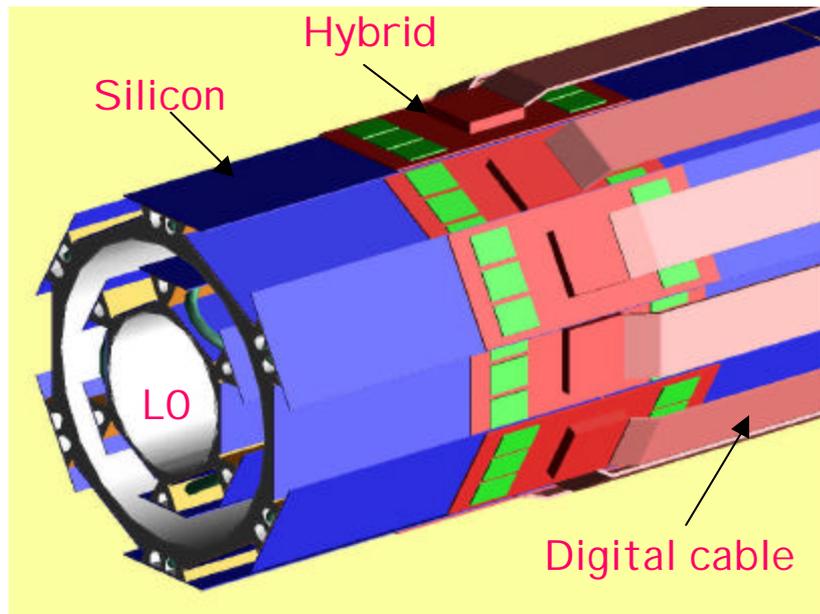
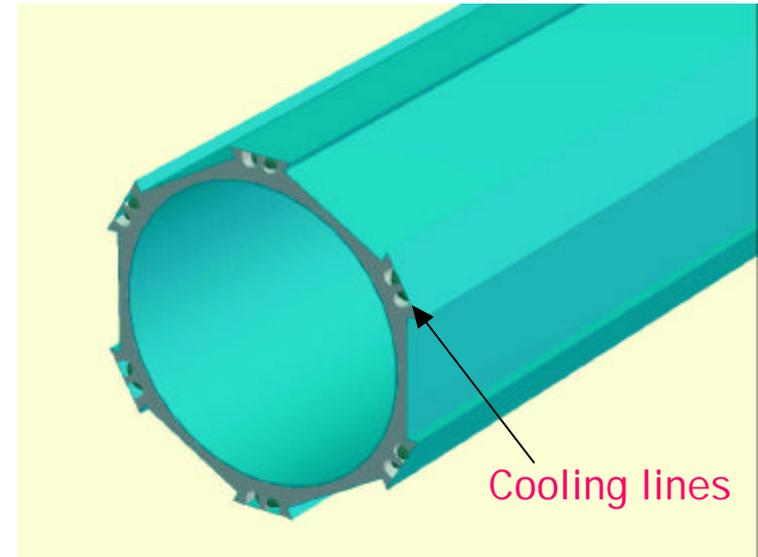
- ❑ Low mass, fine pitch cables to bring analogue signals outside of tracking volume
  - Technically challenging
    - » Feature size ~ 3-4  $\mu\text{m}$
    - »  $C \sim 0.4 \text{ pF/cm}$
- ❑ Dyconex (Switzerland)
  - Delivered 2 pre-prototype cables
    - » 128 channels, trace width 6-7  $\mu\text{m}$
    - » 13.7 mm of 50  $\mu\text{m}$  pitch traces
    - » 26.0 mm of 100  $\mu\text{m}$  pitch traces
    - » fan-in and fan-out region (1.7-2.9 mm)
    - » total trace length including fan-in/out between 41.4 - 42.6 mm
    - » 2 rows of bond pads on each side
    - » No gold plating yet
  - Results so far are very encouraging
    - » Only 3 opens, no shorts
    - » Uniform characteristics across cable



# Layer 1

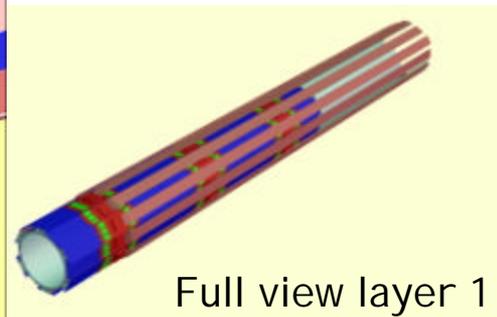
## Support Structure

- 12-fold crenellated geometry
- carbon fiber lined carbon foam
- Integrated cooling
- $R_{in} = 34.8 \text{ mm}$



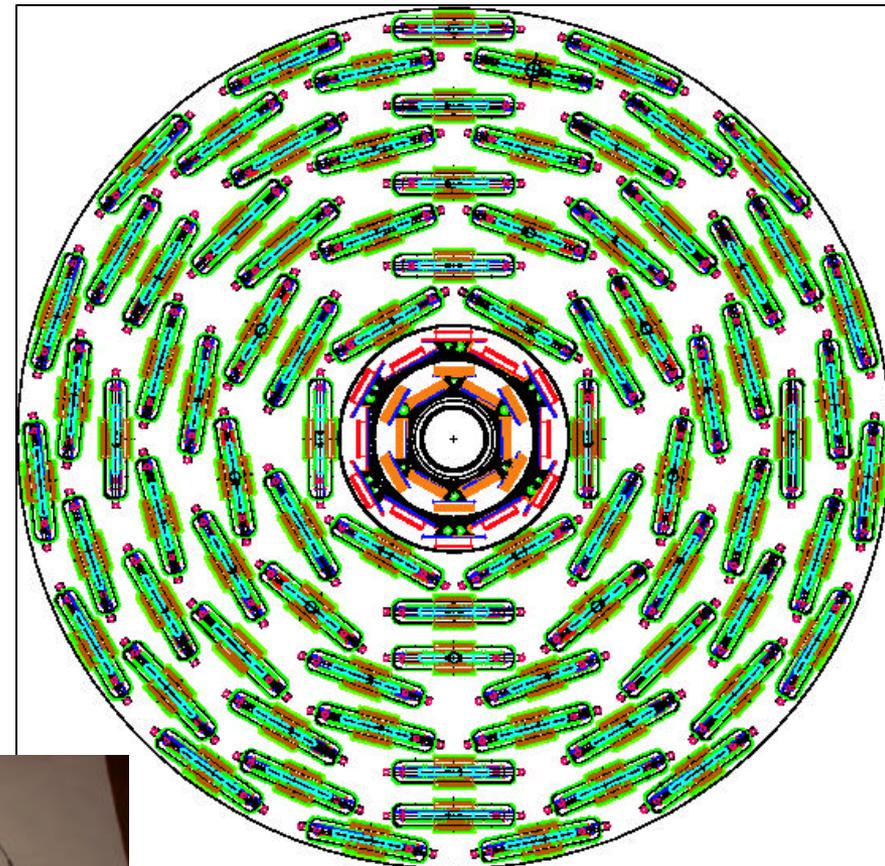
## Assembly

- 3-chip wide sensors, 58  $\mu\text{m}$  pitch, axial readout
- Hybrids on-board
- 6-chip double-ended hybrid readout



# Layers 2-5

- ❑ 12, 18, 24 and 30-fold geometry
- ❑ All layers:
  - 5-chip wide sensors, 30  $\mu\text{m}$  pitch, 60  $\mu\text{m}$  readout
  - Hybrids on-board
  - 10-chip hybrid readout
  - Stereo and axial readout
  - Stereo angle obtained by rotating sensor
- ❑ Support
  - Modules are assembled into staves
  - Staves are positioned with carbon-fiber bulkheads



# Outer Layer Modules

❑ Staves are assembled from readout modules

❑ Readout modules:

➤ 6 types

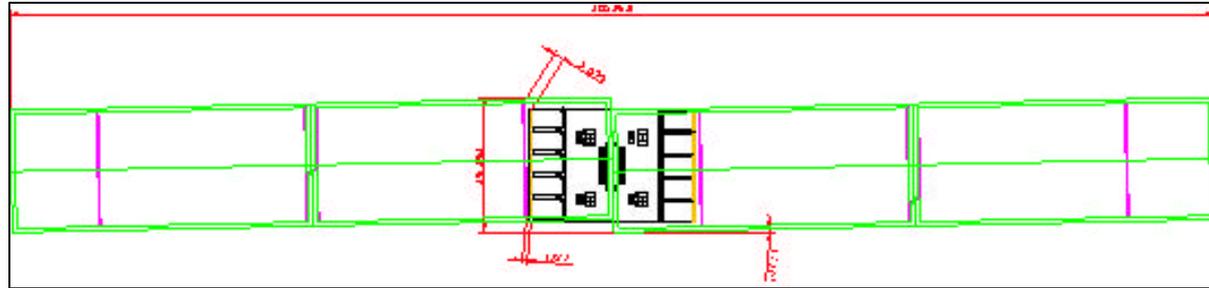
- » 10-10 (axial, stereo)
- » 10-20 (axial, stereo)
- » 20-20 (axial, stereo)

➤ Stereo angle determined by mechanical constraints

- » 10cm readout:  $\alpha = 2.5^\circ$
- » 20cm readout:  $\alpha = 1.25^\circ$
- » For 10-20 readout module, there will be a small gap at the transition

➤ Ganged sensors will have traces aligned

❑ Module configuration



Layer 4-5



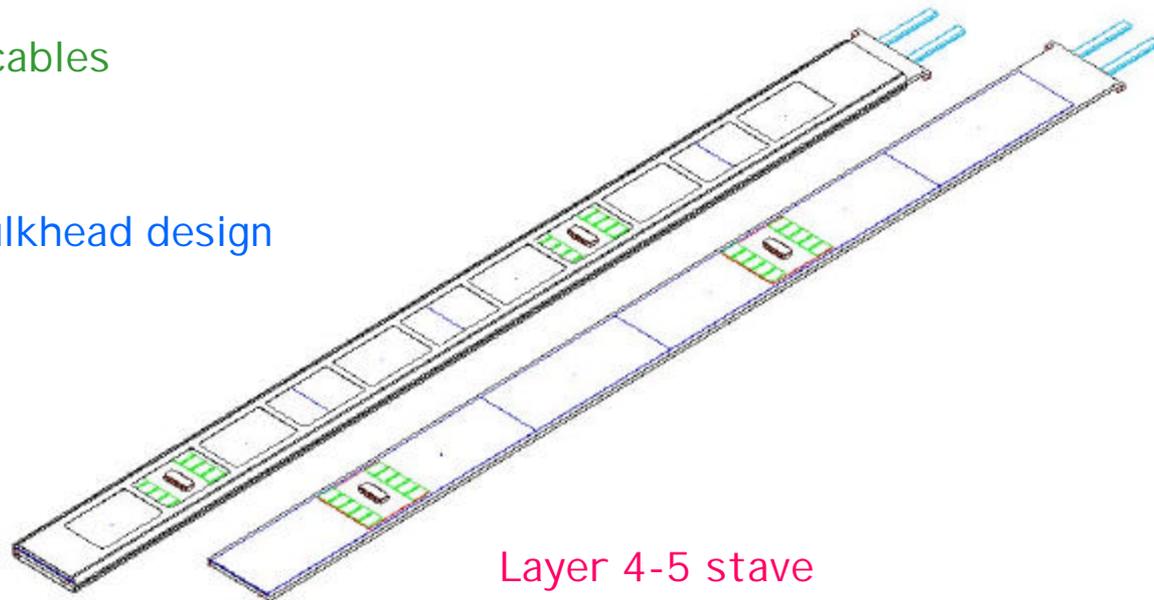
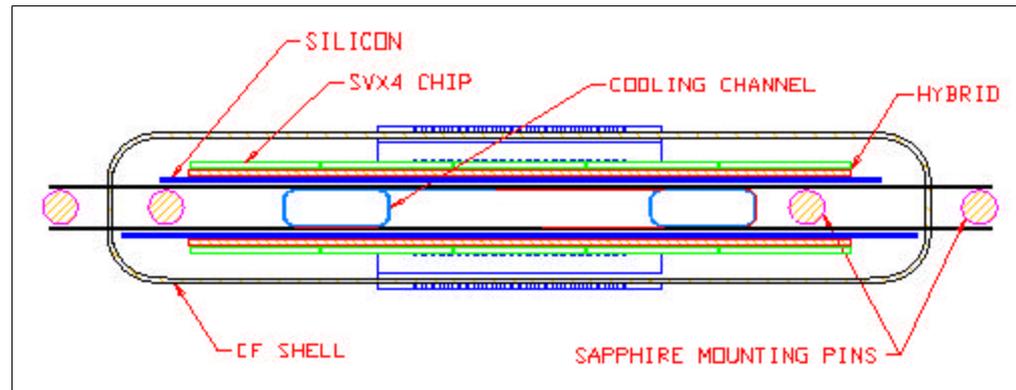
Layer 2-3

10-10

10-20

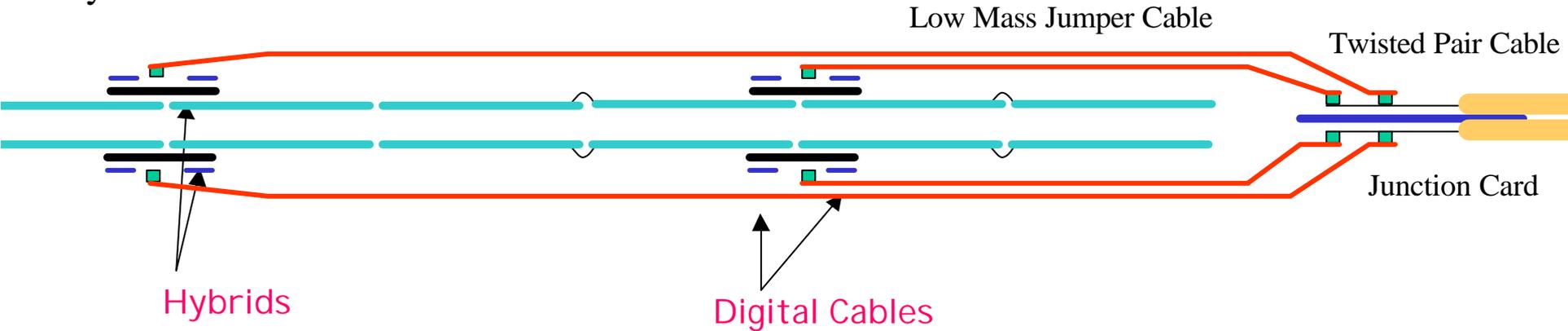
# Stave Structure

- ❑ Stave is doublet structure of four readout modules
  - Two layers of silicon
    - » Axial and stereo
    - » Two readout modules each
  - separated by PEEK cooling lines
  - Total of 168 staves
- ❑ Stave has carbon fiber cover
  - Protect wirebonds
  - Provide path for digital cables
- ❑ Staves are mounted in end carbon fiber bulkheads
- ❑ Cooling manifold similar to bulkhead design



# Stave Readout Schematic

Layer 4-5



## □ Hybrid

- Digitizes Si analogue signal, launches the digital signal on the ...

## □ Digital cable

- Flex circuit which brings signals to the ...

## □ Junction card

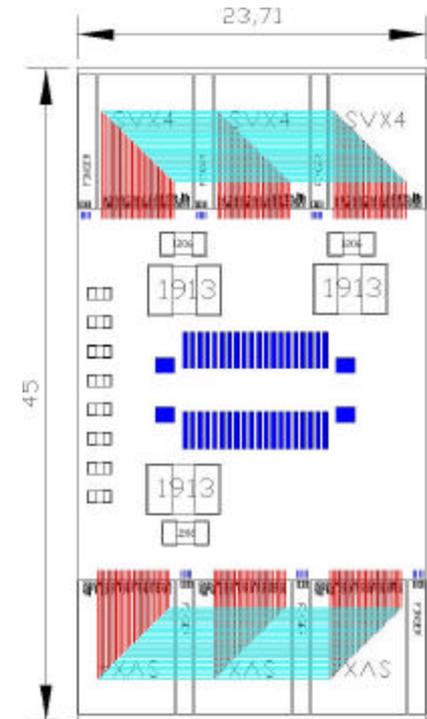
- Passive element which transfers signals to high quality twisted pair signal cable which brings the signal to the ...

## □ Adapter card

- Active element that provides the differential drive for the svx4 chip

# Hybrids

- ❑ Characteristics:
  - Layer 0
    - » 2-chip hybrids; each hybrid reads out one sensor
  - Layers 1-5
    - » Hybrids are double-ended
      - ✿ 6-chip hybrids for layer 1
      - ✿ 10-chip hybrids for layers 2-5
  - Design of Layer 1 hybrid complete
    - » Ceramic hybrid (BeO)
    - » 6 layers
    - » Connector pinout frozen
- ❑ Hybrids carry the bias voltage for layers 2-5 (300 V)
  - One HV feed / hybrid;
  - HV is split between up to 4 sensors
- ❑ Prototype hybrids for Layer 1 ready to be ordered

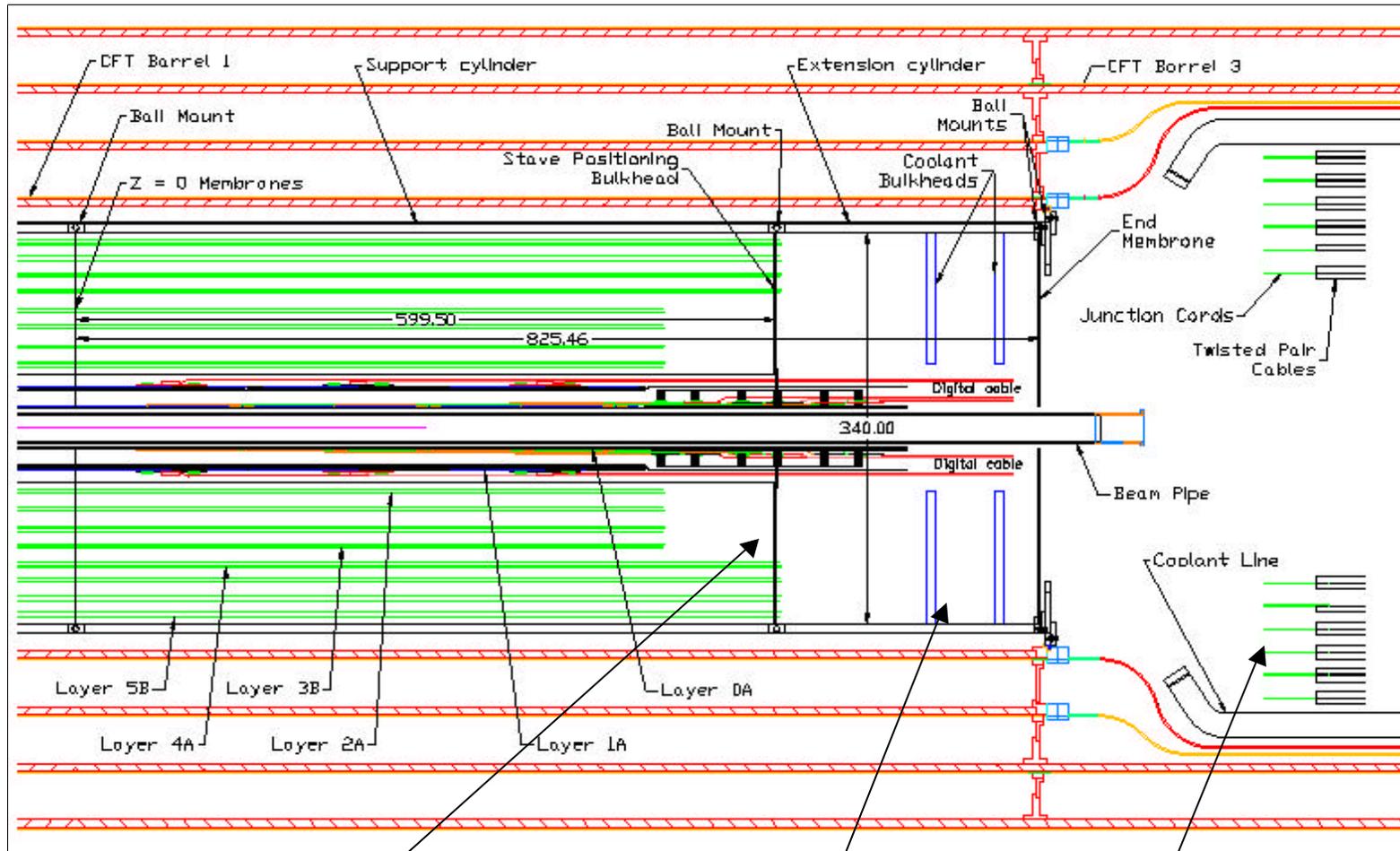


6-chip hybrid

# Digital Cables

- ❑ Digital signals are launched from the hybrid onto the digital flex cable and the twisted pair cable to take the signals out of the tracking volume
  
- ❑ Digital flex cable
  - Traces
    - » 11 differential
      - \* D0-D7, DV, PRI OUT, CLK
    - » 5 single ended
      - \* PRI IN, CHMOD, BEMOD, FEMOD, VCAL
    - » 4 power
      - \* AVDD, AGND, DVDD, DGND
  - 2-layer kapton-Cu cable
  
- ❑ Twisted pair digital cable
  - Twisted Pairs
    - » 10 differential
      - \* D0-D7, DV, PRI OUT
    - » 5 single ended
      - \* PRI IN, CHMOD, BEMOD, FEMOD, VCAL
    - » 2 twisted pairs for power
      - \* AVDD, AGND, DVDD, DGND
    - » 1 twisted pair for HV
    - » 2 coax cables for clocks
  
- ❑ Adapter Card translates signals from 5V to 2.5V. All elements downstream of adapter card should remain the same
- ❑ Adapter card being designed

# Overall Plan View



Positioning bulkhead

Cooling bulkheads

Junction cards

# Parameters

				# Sensors in z	# Sensors Total	Sensor Width (mm)	Readout Pitch ( $\mu\text{m}$ )	# Readout in z	# Chips per Readout	Total Chips	# Hybrids Total
Layer	Nphi	R (mm) Axial	R (mm) Stereo								
0A	12	17.80	---	12	72	15.50	50	12	2	144	72
0B	12	24.65	---	12	72	15.50	50	12	2	144	72
1A	12	34.80	---	12	72	24.97	58	12	3	216	36
1B	12	38.85	---	12	72	24.97	58	12	3	216	36
2A	12	53.57	50.45	10	120	41.10	60	8	5	480	48
2B	12	69.93	66.81	10	120	41.10	60	8	5	480	48
3A	18	88.10	84.98	10	180	41.10	60	8	5	720	72
3B	18	102.30	99.18	10	180	41.10	60	8	5	720	72
4A	24	119.69	116.57	12	288	41.10	60	8	5	960	96
4B	24	133.19	130.07	12	288	41.10	60	8	5	960	96
5A	30	150.36	147.25	12	360	41.10	60	8	5	1200	120
5B	30	163.59	160.47	12	360	41.10	60	8	5	1200	120
<b>Total</b>					<b>2184</b>					<b>7440</b>	<b>888</b>

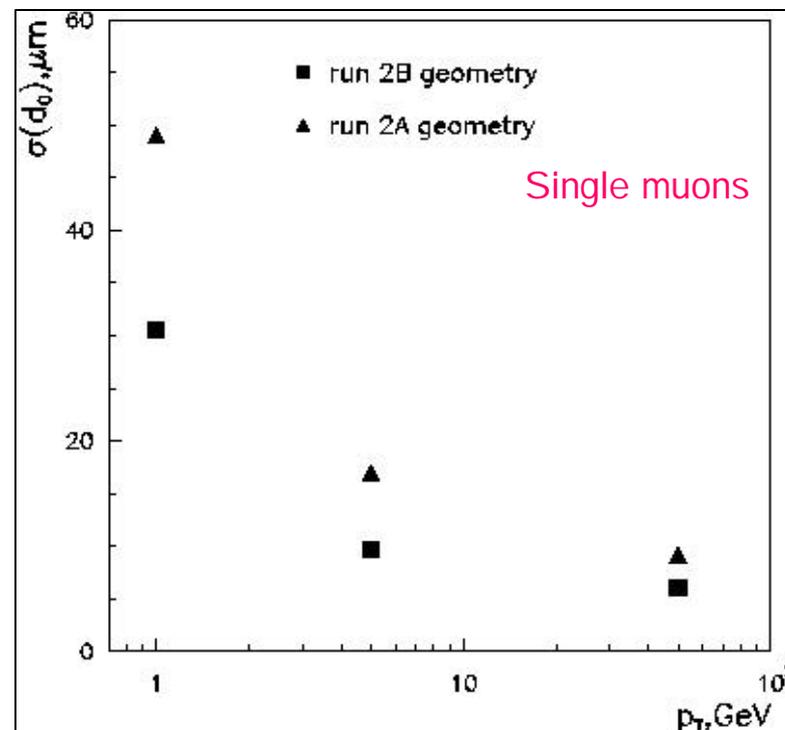
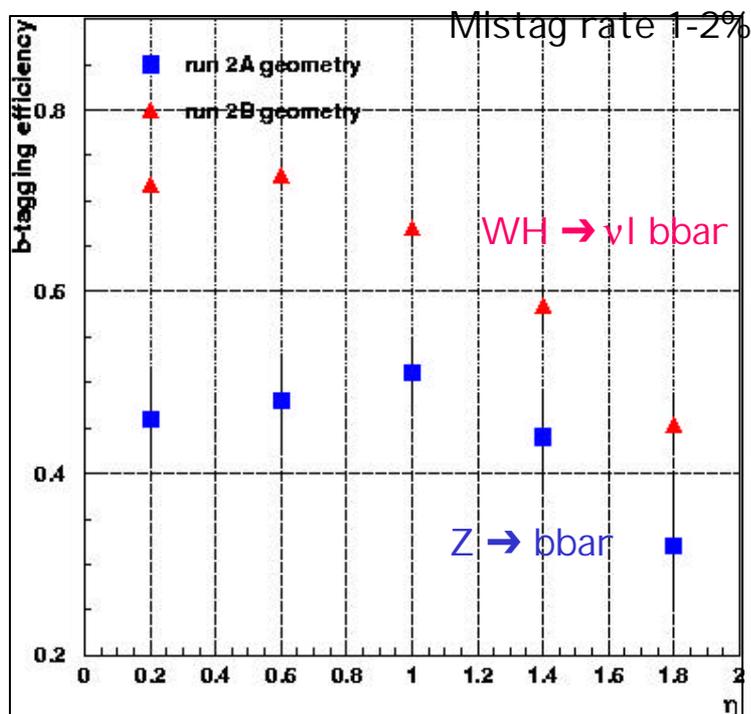
❑ Comparing channel count:

- 2a: 792576 channels
- 2b: 952320 channels

❑ Cable plant is slightly smaller than in Run2a

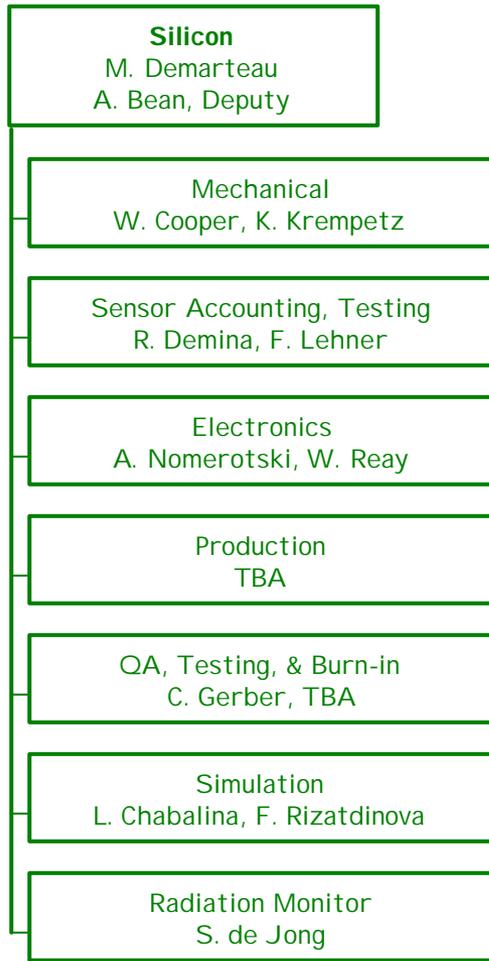
# Performance

- Expected performance of new tracker compared with 2a tracker



	Run2b	Run2a
$P(n_b \geq 1)$	80%	68%
$P(n_b \geq 2)$	35%	21%

# Organization



- ❑ Major commitments from various groups
  - Mechanical
    - » University of Washington: Layer 0, 1
  - Sensor Testing
    - » Kansas State University
    - » Stony Brook
    - » Cinvestav
  - Electronics
    - » Kansas State University
      - ✿ Digital cables, Adapter card
    - » Kansas University
      - ✿ Hybrid testing
  - QA
    - » UIC
  - Radiation Monitoring
    - » NIKHEF, Amsterdam
- ❑ Discussing with other groups
- ❑ Trying to strengthen group
  - Will tap from pool of people when commissioning Run2a detector completed

WBS 1.1 SILICON TRACKER								
WBS 1.1	ITEM SILICON TRACKER	MATERIALS & SERVICES (M&S)				CONTINGENCY		TOTAL Cost
		Unit	#	Unit Cost	M&S TOTAL	%	Cost	
1.1.1	<i>Silicon Sensors</i>				2,244,400	31	703,320	2,947,720
1.1.2	<i>Readout System</i>				3,637,520	47	1,692,004	5,329,524
1.1.3	<i>Mechanical Design and Fabrication</i>				1,649,700	50	830,445	2,480,145
1.1.4	<i>Detector Assembly and Testing</i>				429,000	32	138,050	567,050
1.1.5	<i>Installation</i>				90,000	47	42,500	132,500
1.1.6	<i>Software</i>				51,000	22	11,400	62,400
1.1	SILICON TRACKER				8,101,620	42	3,417,719	11,519,339

- ❑ Total M&S Project cost of \$8.1 M, without contingency
  - Cost estimate carried out down to WBS level 5
  - Estimate has changed very little since first estimate
    - » \$6.8M (\$10.0M) April '01
  - Cost drivers
    - » Silicon sensors
    - » Cables, analogue, digital and twisted pair in near equal amounts
    - » Hybrids

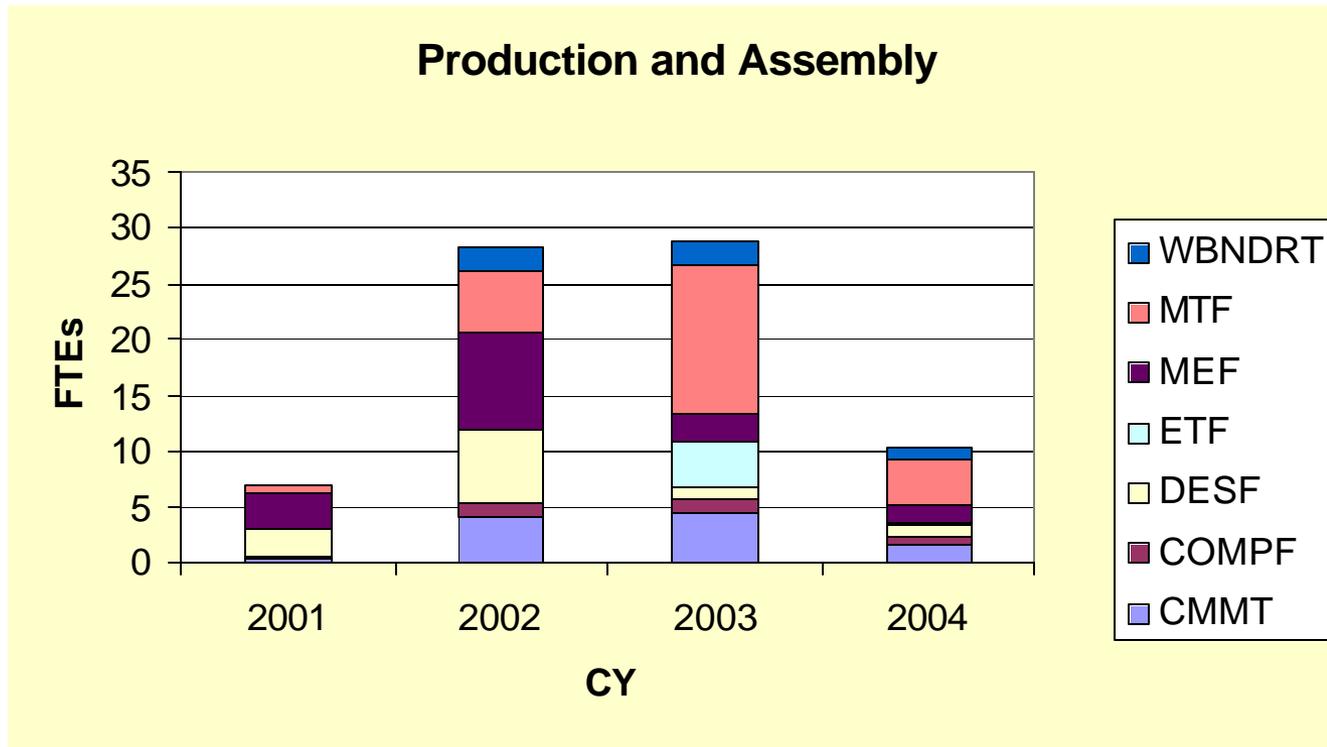
# FY02 Needs

WBS SILICON TRACKER							
WBS	ITEM		R&D		total FY 2002	no contingency	
1.0		#	Unit Cost	R&D TOTAL	#	Unit cost	TOTAL
1.1	<i>Silicon Sensors</i>			192,000			1,342,000
1.2	<i>Readout System</i>			516,200			1,770,700
1.3	<i>Mechanical Design and Fabrication</i>			213,000			968,000
1.4	<i>Detector Assembly and Testing</i>			62,000			158,000
1.0	SILICON TRACKER			983,200			4,238,700

- ❑ Submitted request to laboratory for FY02 in the amount of \$4.2M
- ❑ In order to maintain the schedule, procurement has to start immediately
  - Project needs to be front loaded; otherwise may not recover from delay
- ❑ Needs the full support from the laboratory to maximize return
  - Most efficient way to handle MRI funds if requisitions go through Fermilab (no G&A)
    - » \$0.8M from MRI funds in FY02
  - Phased obligations if purchase order written

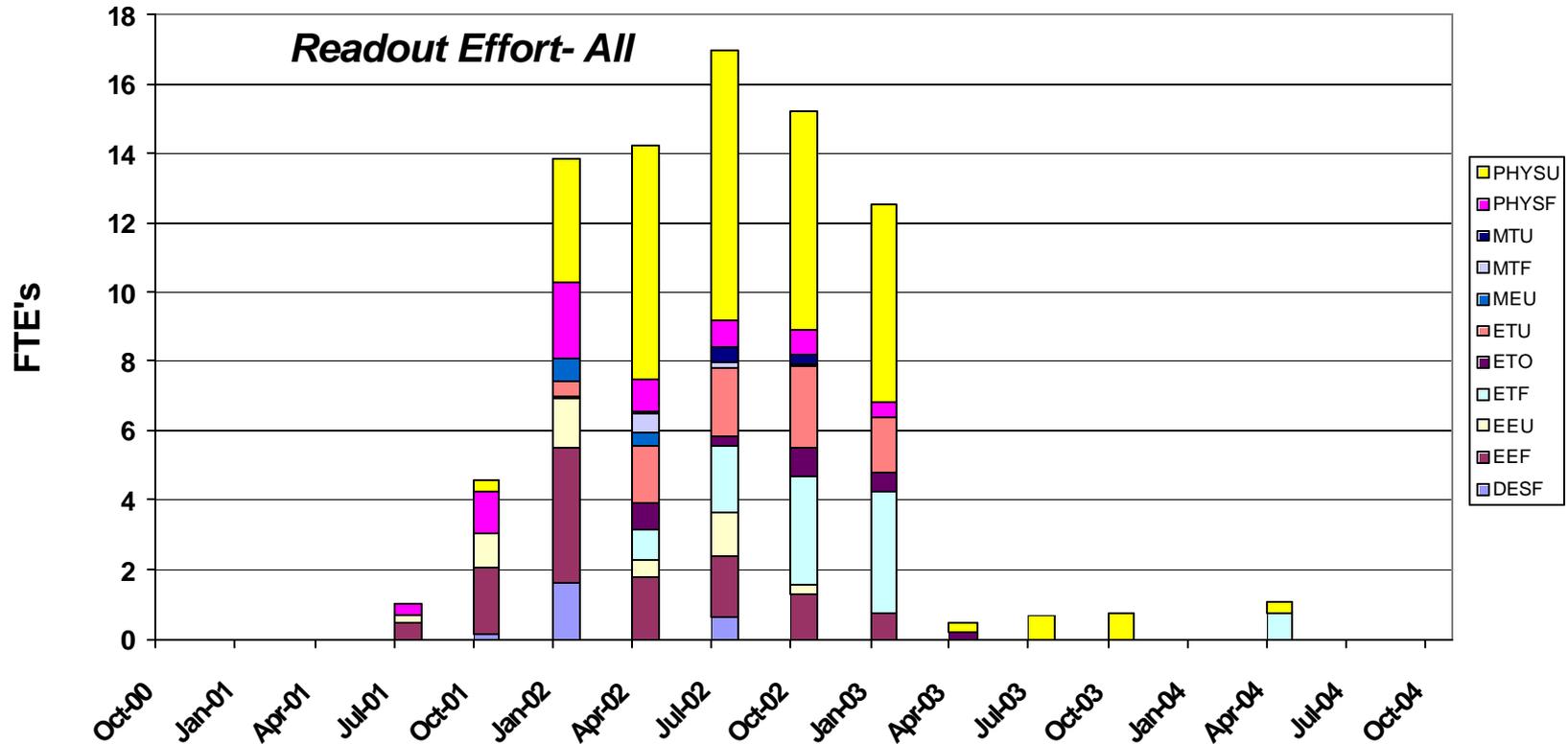
# Resources

- Fermilab resources needed for production only



- At peak:
  - 9 mechanical technicians, 2.5 wirebonders, 4 CMM operators/programmers, 5 electrical technicians

# Resources



## □ At peak:

- 4 electrical engineers, 8 physicists
- Recall, a large part of the electronics is done at universities

# Near Term Start Dates

- ❑ Complete resource loaded schedule being prepared
- ❑ Some near term start dates / milestones

Selected near-term start dates	Start Dates
Produce L0 sensor prototypes	9/11/01
Procure L1 hybrid prototypes	11/29/01
Prepare adapter card prototypes	11/29/01
Prototype support cylinder	11/29/01
Order L1 preproduction sensors	12/12/01
Order L2-L5 preproduction sensors	12/12/01
Beam Tube Order Placed	12/19/01
Perform L0 sensor irradiation testing	1/14/02
Fabricate prototype stave cores	1/16/02
Prepare digital jumper cable prototypes	1/21/02
Produce L2-L5 preproduction sensors	1/25/02
Produce pre-production analog cables	3/27/02

← Submitted to ELMA  
← Ready for submission

# Fallback

- ❑ The design adequately addresses the physics goals of Run2b
  - Emphasis on impact parameter measurement at small radii
  - Minimum of four stereo measurements needed for efficient pattern recognition
- ❑ The design is a conservative, not overextended design
- ❑ As such, any descoping would adversely affect physics performance
- ❑ We believe we can build this device within the time frame proposed, given adequate support
- ❑ Considered 'what if' scenarios
  - Modularity
    - » Inner and outer barrel, north and south tracker built as independent units
  - Branch points
    - » Assess viability of various design choices
    - » Assess impact of delivery schedule for various components
  - Branch points will have to be developed in the near future

# Summary and Conclusions

---

- ❑ The design of the Run2b silicon detector is solid
    - Adequately addresses the physics issues
    - Design not overextended
  - ❑ Schedule is aggressive, but achievable we believe
  
  - ❑ We are in a position to start ordering prototypes for various elements
  - ❑ Delay in procurement will result in linear delay of project
  - ❑ The collaboration is committed to building the new detector; if the project is endorsed, we are looking for a similar commitment from the laboratory
-