

Run 2b Trigger Conceptual Design Report

The DØ Collaboration

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1 Introduction

1.1 Overview

We present in this report a description of the trigger and related upgrades DØ is proposing to mount in order to adequately address the Run 2b physics program. An initial draft of a Technical Design Report for the Run 2b silicon detector is presented to the Committee under separate cover; we include herein a discussion of all the other – “non-silicon” - upgrades we are proposing. These include upgrades to the three trigger levels, as well as the online system. The motivation for these improvements, supported by Monte Carlo studies, is described, as are the technical descriptions of each of the proposed projects. Preliminary outlines of the cost and schedule for each of the upgrades are included as well.

The primary feature driving the design of the Run 2b trigger elements is the higher rates associated with the approximately factor of 2.5 increase in instantaneous luminosity that will be delivered to the experiments. The concomitant increase in the integrated exposure motivates the silicon upgrade, and is less of a concern for the readout elements described here. Nevertheless, with the Run 2 program now expected to extend to 6 or more years of data taking, the long-term hardware needs and maintenance have become more of an issue. This extension of the run has motivated a somewhat modified approach to the development of the Run 2 detector and the associated organization with which we oversee it: we consider the distinction between Run 2a and 2b now as being for the most part artificial, and increasingly treat the Run 2 experiment as a continually evolving, integrated enterprise, with the goal of optimizing the physics reach over the entire run in as efficient and cost-effective a manner as possible. Accordingly, we include in this report brief status reports and plans for the Fiber Tracker Trigger (SIFT) chip replacement for 132 nsec running, the Level 2 β trigger system, and the data acquisition system - all of which are needed for near-term physics running - in addition to those upgrades specifically targeted at addressing the increase in luminosity in 2004. The latter subject, however, is the primary focus of this report. A description of the overall management of the Run 2b project for DØ, including the trigger sub-projects discussed in this report, can be found in the silicon Technical Design Report submitted to this Committee under separate cover.

Finally, we note that the bulk of the information contained here – and particularly that portion of the report focusing on the increase in luminosity, along with the associated simulation studies – reflects the considerable efforts of the DØ Run 2b Upgrade Trigger Task Force. The 29-member Task Force was appointed on June 25, 2001 by the DØ Technical Manager (J. Kotcher); the charge and personnel are given in Appendix A. We take this opportunity to thank the Task Force for its dedication and perseverance in providing the experiment with the basis on which these trigger upgrades can be defined and pursued.

1.2 Trigger Upgrade Motivation

A powerful and flexible trigger is the cornerstone of a modern hadron collider experiment. It dictates what physics processes can be studied properly and what is ultimately left unexplored. The trigger must offer sufficient flexibility to respond to changing physics goals and new ideas. It should allow the pursuit of complementary approaches to a particular event topology in order to maximize trigger efficiency and allow measurement of trigger turn-on curves. Adequate bandwidth for calibration, monitoring, and background samples must be provided in order to calibrate the detector and control systematic errors. If the trigger is not able to achieve sufficient selectivity to meet these requirements, the capabilities of the experiment will be seriously compromised.

As described in the charge to the DØ Run 2b Upgrade Trigger Task Force in Appendix A, a number of ground rules were established for our studies. These reflect the expected Run 2b environment: we anticipate operating at a peak luminosity of $\sim 5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ in Run 2b, which is a factor of 2.5 higher than the Run 2a design luminosity. The higher luminosity leads to increased rates for all physics processes, both signal and backgrounds. Assuming ~ 100 bunches with 132 ns bunch spacing, we expect an average of ~ 5 non-diffractive “minbias” interactions superimposed on each hard scattering. The increased luminosity also increases occupancies in the detector, leading to a substantial loss in trigger rejection for some systems. Thus, triggers sensitive to pileup or combinatorial effects have rates that grow more rapidly than the growth in luminosity.

We will retain the present trigger architecture with three trigger levels. The Level 1 (L1) trigger employs fast, deterministic algorithms, generating an accept/reject decision every 132 ns. The Level 2 (L2) trigger utilizes Digital Signal Processors (DSPs) and high performance processors with variable processing time, but must issue its accept/reject decisions sequentially. The Level 3 (L3) trigger is based on high-performance processors and is completely asynchronous. The L1 and L2 trigger rely on dedicated trigger data paths, while the L3 trigger utilizes the DAQ readout to collect all event data in a L3 processing node.

We cannot accommodate the higher luminosity by simply increasing trigger rates. The L1 trigger rate is limited to a peak rate of ~ 5 kHz by readout deadtime. The L2 trigger rate is limited to a peak rate of ~ 1 kHz by the calorimeter digitization time. Finally, we have set a goal of ~ 50 Hz for the L3 trigger rate to limit the strain on (and cost of) data storage and offline computing.

The above L1 and L2 rate limits remain essentially the same in Run 2b as in Run 2a. Thus, we must accommodate the higher luminosity in Run 2b by increasing the L1 trigger rejection by a factor of 2.5 and maintaining the current L2 rejection factor of 5. Since Run 2b will focus primarily on high- p_T physics processes, we expect some bandwidth will be freed by reducing the trigger rate devoted to low- p_T processes. However, this reduction is not sufficient to meet our rate limitations, nor does it address the difficulties in triggering efficiently on some important high- p_T processes. Only by upgrading the trigger will we have a

reasonable level of confidence in our ability to acquire the data samples needed to carry out the Run 2b physics program.

Potential Run 2b trigger upgrades are further limited by the relatively short time available. Any such upgrade must be completed by the start of high-luminosity running following the installation of the Run 2b silicon tracker, currently scheduled for mid-2004. This goal is made all the more challenging by the need to simultaneously complete and commission the Run 2a detector, acquire physics data, and exploit the resulting physics opportunities. Thus, it is essential that the number and scope of the proposed Run 2b trigger upgrades not exceed the resources of the collaboration.

In the sections below, we describe the results of Task Force studies for these upgrades. We first consider various options for improving the L1 track trigger, since the tracks found by this trigger are potentially useful to the other triggers. We then examine replacement of the L1 calorimeter trigger, which is one of the few remaining pieces of Run 1 electronics in DØ, with entirely new electronics. This upgrade will employ digital filtering to better associate energy with the correct beam crossing and provide the capability of clustering energy from multiple trigger towers. It will also allow improved $e/\gamma/\tau$ triggers that make use of energy flow (HAD/EM, cluster shape/size, isolation) and tracking information. These improvements significantly reduce the rate for multijet background by sharpening trigger thresholds and improving particle identification. The sections that follow describe possible upgrades to the L1 muon trigger, processor and Silicon Track Trigger (STT) upgrades of the L2 trigger, processor upgrades for the L3 trigger, and plans for improvements to the online system. As mentioned above, we also intersperse status reports of the outstanding Run 2a trigger projects – SIFT, L2 β , and L3 - in the relevant sections. The last section summarizes the results and conclusions of the report.

2 Triggers, Trigger Terms, and Trigger Rates

At 2 TeV, the inelastic proton-antiproton cross section is very large, about 50 mb. At Run 2 luminosities, this results in interaction rates of ~ 25 MHz, with multiple interactions occurring in most beam crossings. Virtually all of these events are without interest to the physics program. In contrast, at these luminosities W bosons are produced at a few Hz and a few top quark pairs are produced per hour. It is evident that sophisticated triggers are necessary to separate out the rare events of physics interest from the overwhelming backgrounds. Rejection factors of nearly 10^6 must be achieved in decision times of a few milliseconds.

The salient features of interesting physics events naturally break down into specific signatures which can be sought after in a programmable trigger. The appearance in an event of a high p_T lepton, for example, can signal the presence of a W or a Z . Combined with jets containing b quark tags, the same lepton signature could now be indicative of top quark pair production or the Higgs. Leptons combined instead with missing energy is a classic SUSY discovery topology, etc. The physics “menu” of Run 2 is built on the menu of signatures and topologies available to the trigger. In order for the physics program to succeed, these fundamental objects must remain un-compromised at the highest luminosities. The following paragraphs give a brief overview of the trigger system and a sampling of the physics impact of the various combinations of trigger objects.

2.1 Overview of the DØ Run 2a Trigger System

The DØ trigger system for Run 2 is divided into three levels of increasing complexity and capability. The Level 1 (L1) trigger is entirely implemented in hardware (see Figure 1). It looks for patterns of hits or energy deposition consistent with the passage of high energy particles through the detector. The calorimeter trigger tests for energy in calorimeter towers above pre-programmed thresholds. Hit patterns in the muon system and the Central Fiber Tracker (CFT) are examined to see if they are consistent with charged tracks above various transverse momentum thresholds. These tests take up to $3.5 \mu\text{s}$ to complete, the equivalent of 27 beam crossings. Since $\sim 10 \mu\text{s}$ of deadtime for readout is incurred following a L1 trigger, we have set a maximum L1 trigger rate of 5 kHz.

Each L1 system prepares a set of terms representing specific conditions that are satisfied (e.g. 2 or more CFT tracks with p_T above 3 GeV). These hardware terms are sent to the L1 Trigger Framework, where specific triggers are formed from combinations of terms (e.g. 2 or more CFT tracks with p_T above 3 GeV AND 2 or more EM calorimeter clusters with energy above 10 GeV). Using firmware, the trigger framework can also form more complex combinations of terms involving ORs of hardware terms (e.g. a match of preshower and calorimeter clusters in any of 4 azimuthal quadrants). The Trigger Framework has capacity for 256 hardware terms and about 40 firmware terms.

The Level 2 trigger (L2) takes advantage of the spatial correlations and more precise detector information to further reduce the trigger rate. The L2 system consists of dedicated preprocessors, each of which reduces the data from one detector subsystem (calorimeter, muon, CFT, preshowers, and SMT). A global L2 processor takes the individual elements and assembles them into physics "objects" such as muons, electrons, or jets. The Silicon Track Trigger (STT) introduces the precise track information from the SMT to look for large impact parameter tracks from b quark decays. Some pipelining is necessary at L2 to meet the constraints of the 100 μ s decision time. L2 can accept events and pass them on to Level 3 at a rate of up to 1 kHz.

The Level 3 (L3) trigger consists of a farm of fast, high-level computers (PCs) which perform a simplified reconstruction of the entire event. Even within the tight time budget of 25 ms, this event reconstruction will allow the application of algorithms in the trigger with sophistication very close to that of the offline analyses. Events that satisfy desired characteristics will then be written out to a permanent storage medium. The maximum L3 output for Run 2a is 50 Hz and is largely dictated by downstream computing limits.

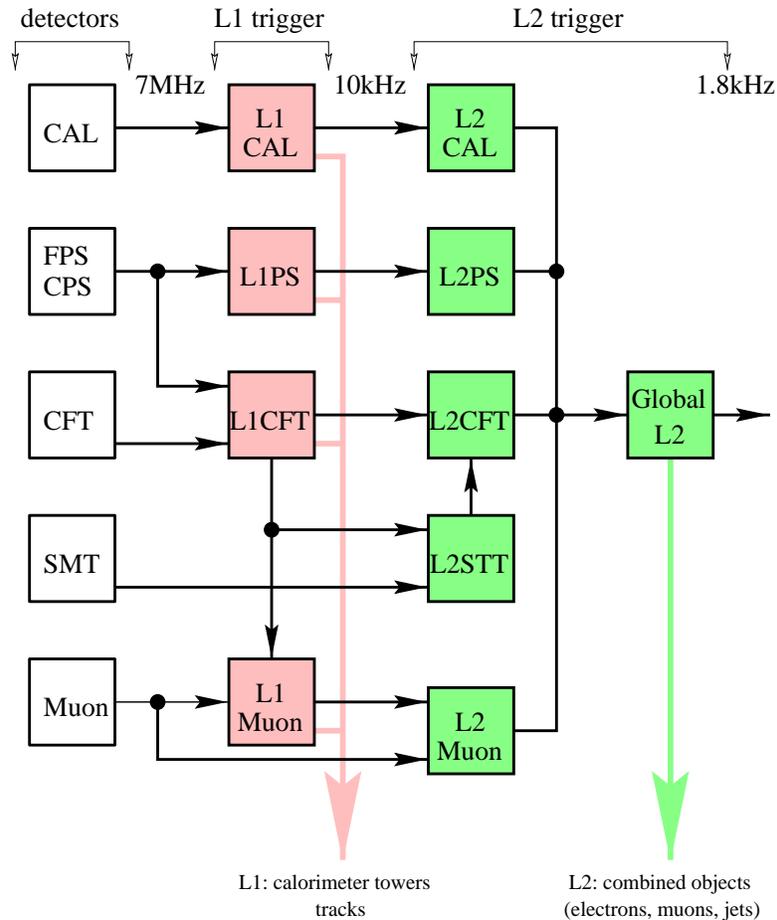


Figure 1. Block diagram of Level 1 and Level 2 triggers, indicating the individual trigger processors that comprise each level.

2.2 Leptonic Triggers

Leptons provide the primary means of selecting events containing W and Z bosons. They can also tag b quarks through their semileptonic decays, complementing the more efficient (but only available at Level 2 through the STT) lifetime selection. The impact of the purely leptonic tag is seen most strongly in the measurements of the W mass, the W and Z production cross sections, and the W width, since the events containing W and Z bosons are selected solely by requiring energetic leptons. The increased statistics provided by Run 2b should allow for a significant improvement in the precision of these measurements, complementing the direct searches in placing more stringent constraints on the Standard Model.

In addition to their inherent physics interest, leptonic signals will play an increasingly important role in the calibration of the energy and momentum scales of the detectors, which is crucial for the top quark and W mass measurements. This will be accomplished using $Z \rightarrow e^+e^-$, $Y \rightarrow e^+e^-$, and $J/\Psi \rightarrow e^+e^-$ for the electromagnetic calorimeter energy scale and the corresponding muon decays for the momentum scale. Since the trigger bandwidth available for acquiring calibration samples must be non-zero, another set of constraints is imposed on the overall allocation of trigger resources.

2.3 Leptons plus Jets

During Run I, lepton-tagged decays of the W bosons and b quarks played an essential role in the discovery of the top quark and were exploited in the measurements of the top mass and production cross section. The new capability provided by the STT to tag b quark decays on-line will allow the collection of many thousands of $t\bar{t}$ pairs in the channel $t\bar{t} \rightarrow \ell\nu + \text{jets}$ with one b -tagged jet. This will be sufficient to allow the study of top production dynamics as well as the measurement of the top decay branching fractions. The precision in measuring the top quark mass will ultimately be limited by our ability to control systematic errors, and the increase in statistics for Run 2b will allow the reduction of several key systematic errors for this channel as well as for the channel $t\bar{t} \rightarrow \ell\nu\ell'\nu + \text{jets}$. One of these, the uncertainty in the jet energy scale, can be reduced by understanding the systematics of the direct reconstruction of W or Z boson decays into jets. The most promising channel in this case is the decay $Z \rightarrow b\bar{b}$, in which secondary vertex triggers can provide the needed rejection against the dominant two-jet background.

2.4 Leptons/Jets plus Missing E_T

Events containing multiple leptons and missing energy are often referred to as the “gold-plated” SUSY discovery mode. These signatures, such as three leptons plus missing energy, were explored in Run I to yield some of the most stringent limits on physics beyond the Standard Model. These investigations will be an integral part of the search for new physics in Run 2. Missing energy is characteristic of any physics process where an invisible particle, such as an energetic neutrino or a massive stable neutral particle, carries away a large

fraction of the available energy. Missing energy combined with leptons/photons or jets can be a manifestation of the presence of large extra dimensions, different SUSY configurations, or other new physics beyond the Standard Model.

2.5 Triggers for Higgs Searches

One of the primary goals of the Run 2b physics program will be to exploit the delivered luminosity as fully as possible in search of the Higgs boson up to the highest accessible Higgs mass¹. Since even a delivered luminosity of 15fb^{-1} per experiment may not lead to a statistically significant discovery, the emphasis will be on the combination of as many decay channels and production mechanisms as possible. For the trigger, this implies that flexibility, ease of monitoring, and selectivity will be critical issues.

Coverage of the potential window of discovery is provided by the decay channel $H \rightarrow b\bar{b}$ at low masses, and by $H \rightarrow W^{(*)}W$ at higher masses. In the first case, the production mechanism with the highest sensitivity will probably be in the mode $p\bar{p} \rightarrow WH$. For leptonic W decays, the leptons can be used to tag the events directly. If the W decays hadronically, however, the four jets from the $q\bar{q}b\bar{b}$ final state will have to be pulled out from the large QCD backgrounds. Tagging b jets on-line will provide a means to select these events and ensure that they are recorded. Of course, three or four jets with sufficient transverse energy are also required. Another decay mode with good sensitivity is $p\bar{p} \rightarrow ZH$, where the Z decays to leptons, neutrinos, or hadrons. From a trigger perspective, the case where the Z decays hadronically is identical to the WH all-hadronic final state. The final state $ZH \rightarrow \nu\bar{\nu}b\bar{b}$, however, provides a stringent test for the jet and missing E_T triggers, since the final state is only characterized by two modest b jets and missing energy.

Recently, the secondary decay mode $H \rightarrow \tau^+ \tau^-$ has come under scrutiny as a means of bolstering the statistics for Higgs discovery in the low mass region. A trigger that is capable of selecting hadronic tau decays by means of isolated, stiff tracks or very narrow jets may give access to the gluon-fusion production mode $gg \rightarrow H \rightarrow \tau^+ \tau^-$ for lower Higgs masses. This mode can also be important in some of the large $\tan\beta$ SUSY scenarios, where the Higgs coupling to $b\bar{b}$ is reduced, leaving $H \rightarrow \tau^+ \tau^-$ as the dominant decay mode for the lightest Higgs.

The higher Higgs mass regime will be covered by selecting events from $p\bar{p} \rightarrow H \rightarrow W^{(*)}W$ with one or two high-energy leptons from the $W \rightarrow \ell\nu$ decay. This decay mode thus requires a trigger on missing E_T in addition to leptons or leptons plus jets. Supersymmetric Higgs searches will require triggering on final states containing 4 b-quark jets. This will require jet triggers at L1 followed by use of the STT to select jets at L2.

¹ Report of the Higgs Working Group of the Tevatron Run 2 SUSY/Higgs Workshop, M. Carena *et al*, hep-ph/0010338.

2.6 Trigger Menu and Rates

As even this cursory review makes clear, the high- p_T physics menu for Run 2b requires efficient triggers for jets, leptons (including taus, if possible), and missing E_T at Level 1. The STT will be crucial in selecting events containing b quark decays; however, its rejection power is not available until Level 2, making it all the more critical that the Level 1 system be efficient enough to accept all the events of interest without overwhelming levels of backgrounds.

In an attempt to set forth a trigger strategy that meets the physics needs of the experiment, the Run 2 Trigger Panel suggested a preliminary set of Trigger Terms for Level 1 and Level 2 triggers². In order to study the expected trigger rates for various physics processes, many of these terms have been implemented into the Run 2 Trigger Simulation. While the results are still preliminary, the overall trend is very clear. The simple triggers we have currently implemented at Level 1 for Run2a will not be able to cope with the much higher occupancies expected in Run2b without a drastic reduction in the physics scope of the experiment and/or prescaling of important physics triggers. Our rate studies have used QCD jets samples in order to determine the effects of background, including multiple low- p_T minimum bias events superimposed on the dominant processes. For example, in a sample of jet events including jets down to a p_T of 2 GeV, a high- p_T electron/photon trigger requiring a 10 GeV electromagnetic tower in the central calorimeter has very low rate at a luminosity of $4 \times 10^{31} \text{ cm}^{-2} \text{ s}^{-1}$; this rate at $5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ is 5.4 kHz, which exceeds the Level 1 trigger bandwidth. A di-electron or di-photon trigger requiring a 10 GeV electromagnetic tower in the central region and a 5 GeV electromagnetic tower in the calorimeter endcaps is expected to reach a rate of 2.7 kHz at a luminosity of $5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$. A two-track trigger requiring one track with a p_T greater than 10 GeV with a total of two tracks above 5 GeV reaches an expected rate of 10 kHz. A number of triggers have rates that grow significantly faster than the increase in luminosity, which is due to the effects of pileup and increased occupancy at high luminosity. Even given the uncertainties in the simulation of multiple interactions, these results demonstrate that the current Level 1 trigger system will not function as desired in the high-occupancy, high-luminosity Run 2b environment.

We now turn to discussions of potential upgrades to the trigger system in order to cope with the large luminosities and occupancies of Run 2b.

² The report of the Run 2 Trigger Panel can be found at http://d0server1.fnal.gov/projects/run2b/Trigger/Docs/Trigger_Panel_Report.ps.

3 Level 1 Tracking Trigger

The Level 1 Central Tracking Trigger (CTT) plays a role in the full range of L1 triggers. In this section, we outline the goals for the CTT, describe the implementation and performance of the present track trigger, and examine three options for upgrading the CTT.

3.1 Goals

The goals for the CTT include providing track triggers, combining tracking and preshower information to identify electron and photon candidates, and generating track lists that allow other trigger systems to perform track matching. It is a critical part of the L1 muon trigger. We briefly discuss these goals below.

3.1.1 Track Triggers

The CTT provides various Level 1 trigger terms based on counting the number of tracks whose transverse momentum (p_T) exceeds a threshold. Track candidates are identified in the axial view of the Central Fiber Tracker (CFT) by looking for hits in all 8 layers within predetermined roads. Four different sets of roads are defined, corresponding to p_T thresholds of 1.5, 3, 5, and 10 GeV, and the number of tracks above each threshold can be used in the trigger decision. For example, a trigger on two high p_T tracks could require two tracks with $p_T > 5$ GeV and one track with $p_T > 10$ GeV.

Triggering on isolated tracks provides a complementary approach to identifying high- p_T electron and muon candidates, and is potentially useful for triggering on hadronic tau decays. To identify isolated tracks, the CTT looks for additional tracks within a 12° region in azimuth (ϕ).

3.1.2 Electron/Photon Identification

Electron and photon identification is augmented by requiring a significant energy deposit in the preshower detector. The Central Preshower (CPS) and Forward Preshower (FPS) detectors utilize the same readout and trigger electronics as the fiber tracker, and are included in the discussion of tracking triggers. Clusters found in the axial layer of the CPS are matched with track candidates to identify central electron and photon candidates. The FPS cannot be matched with tracks, but comparing energy deposits before/after the lead radiator allows photon and electron candidates to be distinguished.

3.1.3 Track Matching

Track candidates found in the CTT are probably most important as input to several other trigger systems. CTT information is used to both correlate tracks with other detector measurements and to serve as seeds for pattern recognition algorithms. We mention below the ways tracks are used in other trigger systems.

The Level 1 muon trigger matches CTT tracks with hits in the muon detector. To meet timing requirements, the CTT tracks must arrive at the muon trigger on the same time scale as the muon proportional drift tube (PDT) information becomes available.

The current Level 1 trigger allows limited azimuthal matching of tracking and calorimeter information at the quadrant level (see section 2.1). Significantly increasing the flexibility and granularity of the calorimeter track matching is under consideration for Run 2b (see section 11). This option would require sending track lists to the calorimeter trigger.

The L2 Silicon Track Trigger (STT) uses tracks from the CTT to generate roads for finding tracks in the Silicon Microstrip Tracker (SMT). The precision of the SMT measurements at small radius, combined with the larger radius of the CFT, allows displaced vertex triggers, sharpening of the momentum thresholds for track triggers, and elimination of fake tracks found by the CTT. The momentum spectrum for b-quark decay products extends to low p_T . The CTT therefore aims to provide tracks down to the lowest p_T possible. The Run 2a CTT generates track lists down to $p_T \approx 1.5$ GeV. The CTT tracks must also have good azimuthal (ϕ) resolution to minimize the width of the road used by the STT.

In addition to the track lists sent to the STT, each portion of the L1 track trigger (CFT, axial CPS, and FPS) provides information for the Level 2 trigger decision. The stereo CPS signals are also sent to L2 to allow 3-D matching of calorimeter and CPS signals.

3.2 Description of Current Tracking Trigger

We have limited our consideration of potential track trigger upgrades to those that preserve the overall architecture of the current tracking trigger. The sections below describe the tracking detectors, trigger segmentation, trigger electronics, outputs of the track trigger, and the trigger algorithms that have been developed for Run 2a.

3.2.1 Tracking Detectors

The CFT is made of scintillating fibers mounted on eight low-mass cylinders. Each of these cylinders supports four layers of fibers arranged into two doublet layers. The innermost doublet layer on each cylinder has its fibers oriented parallel to the beam axis. These are referred to as Axial Doublet layers. The second doublet layer has its fibers oriented at a small angle to the beam axis. These are referred to as Stereo Doublet layers. Only the Axial Doublet layers are incorporated into the current L1 CTT. Each fiber is connected to a visible light photon counter (VLPC) that converts the light pulse to an electrical signal.

The CPS and FPS detectors are made of scintillator strips with wavelength-shifting fibers threaded through each strip. The CPS has an axial and two stereo layers outside mounted on the outside of the solenoid. The FPS has two stereo layers in front of a lead radiator and two stereo layers behind the radiator. The CPS/FPS fibers are also readout using VLPCs.

3.2.2 CTT Segmentation

The CTT is divided in ϕ into 80 Trigger Sectors (TS). A single TS is illustrated schematically in Figure 2. To find tracks in a given sector, information is needed from that sector, called the home sector, and from each of its two

neighboring sectors. The TS is sized such that the tracks satisfying the lowest p_T threshold (1.5 GeV) is contained within a single TS and its neighbors. A track is 'anchored' in the outermost (H) layer. The ϕ value assigned to a track is the fiber number at the H layer. The p_T value for a track is expressed as the fiber offset in the innermost (A) layer from a straight-line trajectory.

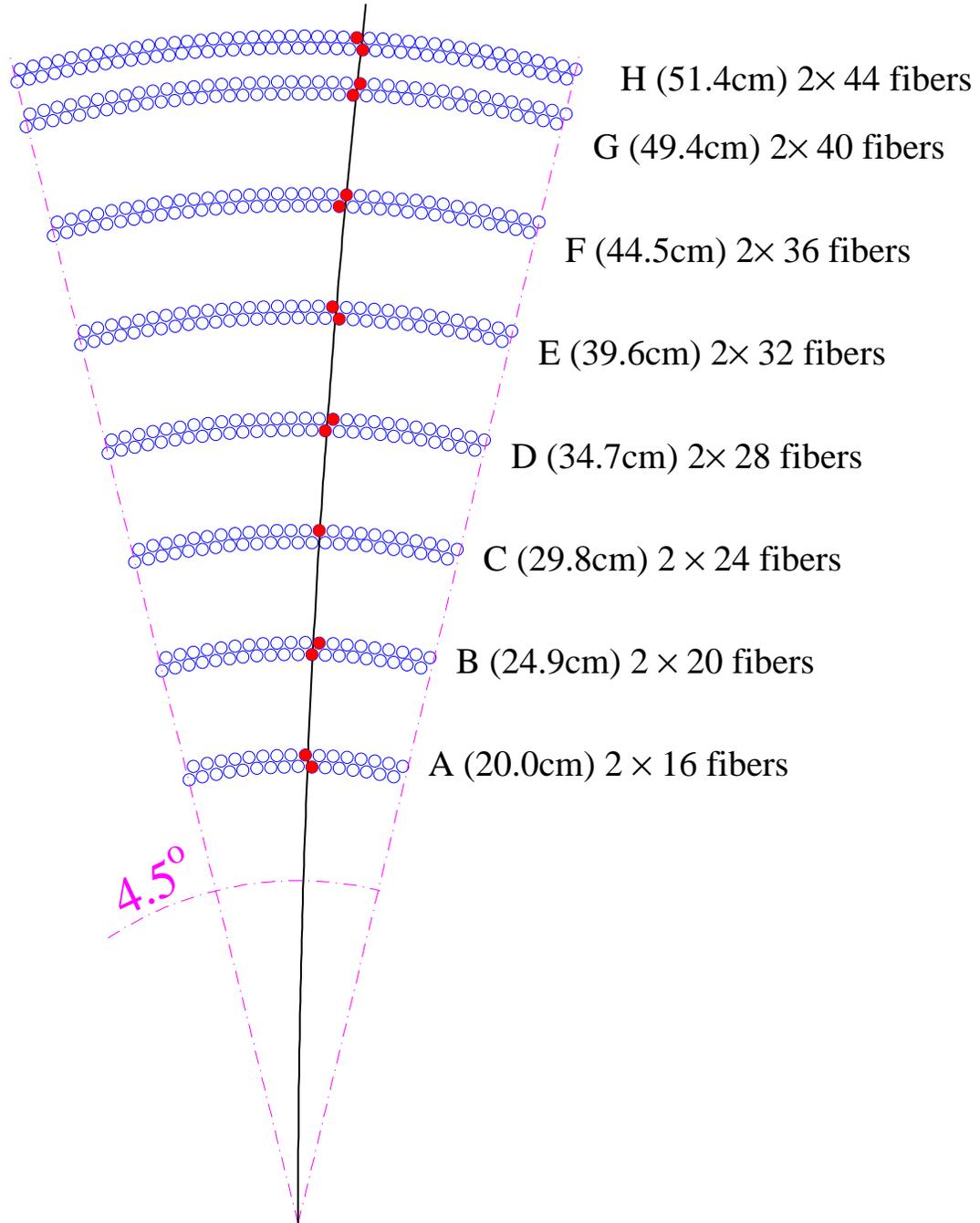


Figure 2. Illustration of a CTT trigger sector and the labels assigned to the eight CFT cylinders. Each of the 80 trigger sectors has a total of 480 axial fibers.

The home sector contains 480 axial fibers. A further 368 axial fibers from 'next' and 'previous' sectors are sent to each home sector to find all the possible axial tracks above the p_T threshold. In addition, information from 16 axial scintillator strips from the CPS home sector and 8 strips from each neighboring sector are included in the TS for matching tracks and preshower clusters.

3.2.3 CTT Electronics

The tracking trigger hardware has three main functional elements. The first element is the Analog Front-End (AFE) boards that receive signals from the VLPCs. The AFE boards provide both digitized information for L3 and offline analysis as well as discriminated signals used by the CTT. Discriminator thresholds should be set at a few photoelectrons for the CFT and at the 5 – 10 MIP level for the CPS and FPS. Discriminator outputs for 128 channels are buffered and transmitted over a fast link to the next stage of the trigger. The axial layers of the CFT are instrumented using 76 AFE boards, each providing 512 channels of readout. The axial CPS strips are instrumented using 10 AFE boards, each having 256 channels devoted to axial CPS readout and the remaining 256 channels devoted to stereo CFT readout. The FPS is instrumented using 32 AFE boards. Additional AFE boards provide readout for the stereo CPS strips and remaining stereo CFT fibers.

The second hardware element is the Mixer System (MS). The MS resides in a single crate and is composed of 20 boards. It receives the signals from the AFE boards and sorts them for the following stage. The signals into the AFE boards are ordered in increasing azimuth for each of the tracker layers, while the trigger is organized into TS wedges covering all radial CFT/CPS axial layers within 4.5 degrees in ϕ . Each MS board has sixteen CFT inputs and one CPS input. It shares these inputs with boards on either side within the crate and sorts them for output. Each board then outputs signals to two DFEA boards (described below), with each DFEA covering two TS.

The third hardware element is based on the Digital Front-End (DFE) motherboard. These motherboards provide the common buffering and communication links needed for all DFE variants and support two different types of daughter boards, single-wide and double-wide. The daughter boards implement the trigger logic using Field Programmable Gate Array (FPGA) chips. The signals from the Mixer System are received by 40 DFE Axial (DFEA) boards. There are also 5 DFE Stereo (DFES) boards that prepare the signals from the CPS stereo layers for L2 and 16 DFEF boards that handle the FPS signals.

3.2.4 CTT Outputs

The current tracking trigger was designed to do several things. For the L1 Muon trigger it provides a list of found tracks for each crossing. For the L1 Track Trigger it counts the number of tracks found in each of four p_T bins. It determines the number of tracks that are isolated (no other tracks in the TS or its neighbors). The sector numbers for isolated tracks are recorded to permit triggers on acoplanar high p_T tracks. Association of track and CPS clusters provides the ability to recognize both electron and photon candidates. FPS clusters are

categorized as electrons or photons, depending on an association of MIP and shower layer clusters. Finally, the L1 trigger boards store lists of tracks for each beam crossing, and the appropriate list is transferred to L2 processors when an L1 trigger accept is received.

The L1 CTT must identify real tracks within several p_T bins with high efficiency. The nominal p_T thresholds of the bins are 1.5, 3, 5, and 10 GeV. The L1 CTT must also provide rejection of fake tracks (due to accidental combinations in the high multiplicity environment). The trigger must perform its function for each beam crossing at either 396 ns or 132 ns spacing between crossings. With the exception of the front end electronics, the system as constructed should accommodate both crossing intervals³.

A list of up to six found tracks for each crossing is packed into 96 bits and transmitted from each of the 80 trigger sectors. These tracks are used by the L1 Muon trigger and must be received within 1000ns of the crossing. These track lists are transmitted over serial copper links from the DFEA boards.

The L1 CTT counts the number of tracks found in each of the four p_T bins, with subcategories such as the number of tracks correlated with showers in the Central Preshower Detector, and the number of isolated tracks. Azimuthal information is also preserved so that information from each ϕ region can be correlated with information from other detectors. The information from each of the 80 TS is output to a set of 8 Central Tracker Octant Card (CTOC) boards, which are DFE mother boards equipped with CTOC type double wide daughter boards. During L1 running mode, these boards collect the information from each of 10 DFEA boards, combine the information and pass it on to a single **CTTT** board. The CTTT board, also a DFE-type mother board equipped with a similar double wide daughter board, assembles the information from the eight CTOC boards and reformats it for transmission to the Trigger Manager (TM). The TM constructs the 32 AND/OR terms that are used by the Trigger Framework in forming the L1 trigger decision. For example, the term "TPQ(2,3)" indicates two tracks associated with CPS hits were present in quadrant 3. Additional AND/OR terms provide CPS and FPS cluster characterization for use in L1. The Trigger Framework accommodates a total of 256 such terms, feeding them into a large programmable AND/OR network that determines whether the requirements for generating a trigger are met.

The DFEA boards store lists of tracks from each crossing, and those lists are transferred to the L2 processors when an L1 trigger accept is received. A list of up to 6 tracks is stored for each p_T bin. When an L1 trigger accept is received, the normal L1 traffic is halted and the list of tracks is forwarded to the CTOC board. This board recognizes the change to L2 processing mode and combines the many input tracks lists into a single list that is forwarded to the L2 processors. Similar lists of preshower clusters are built by the DFES and DFEF boards for the

³ Work is in progress to upgrade the AFE boards to AFE2 versions that will support operation at 132 ns crossings. See section 3.4

CPS stereo and FPS strips and transferred to the L2 processors upon receiving an L1 trigger accept.

3.2.5 Tracking Algorithm

The tracking trigger algorithm currently implemented is based upon hits constructed from pairs of neighboring fibers, referred to as a “doublet”. Fibers in doublet layers are arranged on each cylinder as illustrated in Figure 3. In the first stage of the track finding, doublet layer hits are formed from the individual axial fiber hits. The doublet hit is defined by an OR of the signals from adjacent inner and outer layer fibers in conjunction with a veto based upon the information from a neighboring fiber. In Figure 3, information from the first fiber on the left on the upper layer would be combined by a logical OR with the corresponding information for the second fiber from the left on the lower layer. This combination would form a doublet hit unless the first fiber from the left on the lower layer was also hit. Without the veto, a hit in both the first upper fiber and the first lower fiber would result in two doublet hits.

Doublet Layer

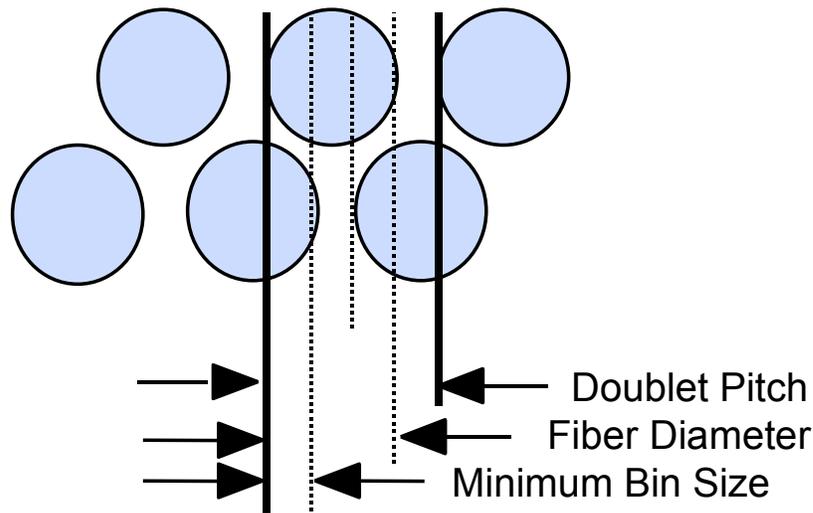


Figure 3. Sketch illustrating the definition of a fiber doublet. The circles represent the active cross sectional areas of individual scintillating fibers. The boundaries of a doublet are shown via the thick black lines. The dashed lines delineate the four distinguishable regions within the doublet.

The track finding within each DFEA board is straightforward. Each daughter board has 4 large FPGA chips, one for each of the four p_T bins. Within each chip the track roads are represented by equations which correspond to a list of which doublets can be hit for a track with a given p_T and ϕ . For each possible road the eight fibers for that road are combined into an 8-fold-AND equation. If all the

fibers on that road were hit then all 8 terms of the AND are TRUE and the result is a TRUE. The FPGA chips are loaded with the equations for all possible real tracks in each sector in each p_T range. Each TS has 44 ϕ bins and 24 possible p_T bins and in addition about 12 different routes through the intermediate layers. This results in about 12K equations per TS.

The individual track results are then OR'ed together by ϕ bin and sorted by p_T . Up to six tracks per TS are reported out to the trigger. This list of 6 tracks is then sent to the fifth or backend chip on the daughter board for all the remaining functions.

The FPGA chips have a very high density of gate logic which lends itself well to the track equations. Within these chips all 12k equations are processed simultaneously in under 200 ns. This design also keeps the board hardware as general as possible. The motherboard is simply an I/O device and the daughter boards are general purpose processors. Since algorithms and other details of the design are implemented in the FPGA, which can be reprogrammed via high level languages, one can re-download different triggers configurations for each run or for special runs and the trigger can evolve during the run.

3.3 Performance with the Run 2a Tracking Trigger

We have simulated the rates to be expected for purely track triggers in Run 2b, taking into account the overlay of minimum bias events within the beam crossing of interest.

3.3.1 Minimum Bias Event Models

At present, the DØ Monte Carlo is making a transition in its modeling of the minimum bias events. The old model uses the **ISAJET** Monte Carlo for QCD processes with $p_T > 1.0$ GeV. The new model uses the **PYTHIA** Monte Carlo with parameters that have been tuned to match CDF minimum bias data samples. The **PYTHIA** samples also include diffractive processes. As illustrated in Figure 4, the trigger rates obtained using these two models are substantially different. Table 1 provides a comparison of the mean CFT occupancy in each fiber layer due to minimum bias events from both models. The table also includes collider data taken with the solenoid magnet on. The **ISAJET** model seems to result in higher occupancies than currently observed in minimum bias data, while the **PYTHIA** model generates substantially fewer hits than observed. Part of this difference is due to the diffractive events generated by **PYTHIA**, which are expected to generate few CFT hits and have low efficiency for firing the minimum bias trigger used in collecting the data. Furthermore, the CFT readout electronics used to collect the data were pre-prototypes of the analog front end (AFE) boards. It is probable that noise on these boards also accounts for some of the factor of two difference between the new **PYTHIA** model and data. It is not currently possible to determine whether the occupancies in the AFE data will eventually be a better match to results from the **ISAJET** or the **PYTHIA** model of the minimum bias events.

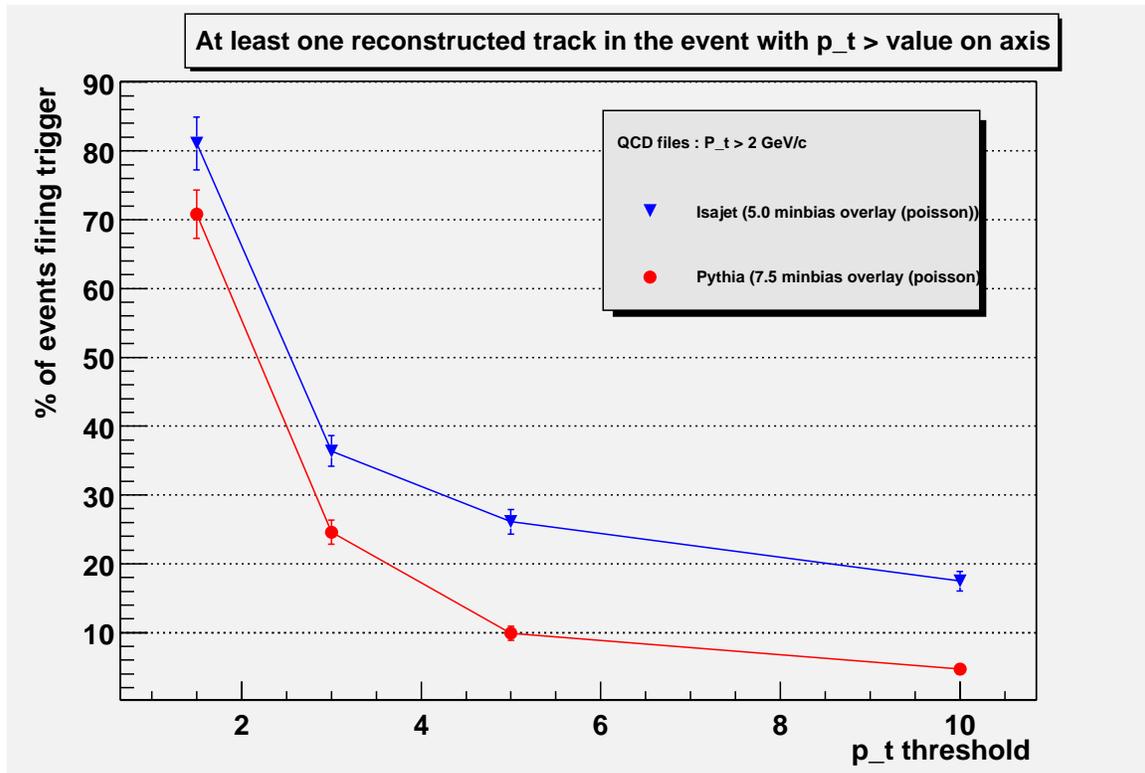


Figure 4. Comparison of the percentage of Monte Carlo QCD events that satisfy the trigger as a function of the threshold of the track for events generated using **ISAJET** and **PYTHIA** models of overlaid minimum bias interactions.

Table 1. Comparison of the percentage occupancy of various layers of the CFT as calculated using two different minimum bias models of a single minimum bias interaction and as measured using low luminosity magnet on data.

CFT Layer	ISAJET (Old) Model (%)	PYTHIA (New) Model (%)	Data (%)	Old/Data	New/Data
A	4.9	2.1	-	-	-
B	3.7	1.6	3.4	1.1	0.47
C	4.3	1.8	3.7	1.2	0.49
D	3.5	1.5	-	-	-
E	2.9	1.2	2.3	1.3	0.52
F	2.5	1.0	-	-	-
G	2.1	0.87	1.6	1.3	0.54
H	2.0	0.82	1.6	1.3	0.51

3.3.2 Simulations of the Run 2a trigger

Under Run 2a conditions, the current track trigger performs very well in simulations. For example, for a sample of simulated muons with $p_T > 50$ GeV/c, we find that 97% of the muons are reconstructed correctly; of the remaining 3%, 1.9% of the tracks are not reconstructed at all and 1.1% are reconstructed as two tracks due to detector noise. (As the background in the CFT increases, due to overlaid events, we expect the latter fraction to get progressively higher). Since the data-taking environment during Run 2b will be significantly more challenging, it is important to characterize the anticipated performance of the current trigger under Run 2b conditions.

To test the expected behavior of the current trigger in the Run 2b environment, the existing trigger simulation code was used with an increased number of overlaid minimum bias interactions. The minimum bias interactions used in this study were generated using the **ISAJET** Monte Carlo model. As described above; this should give a worst case scenario for the Run 2b trigger.

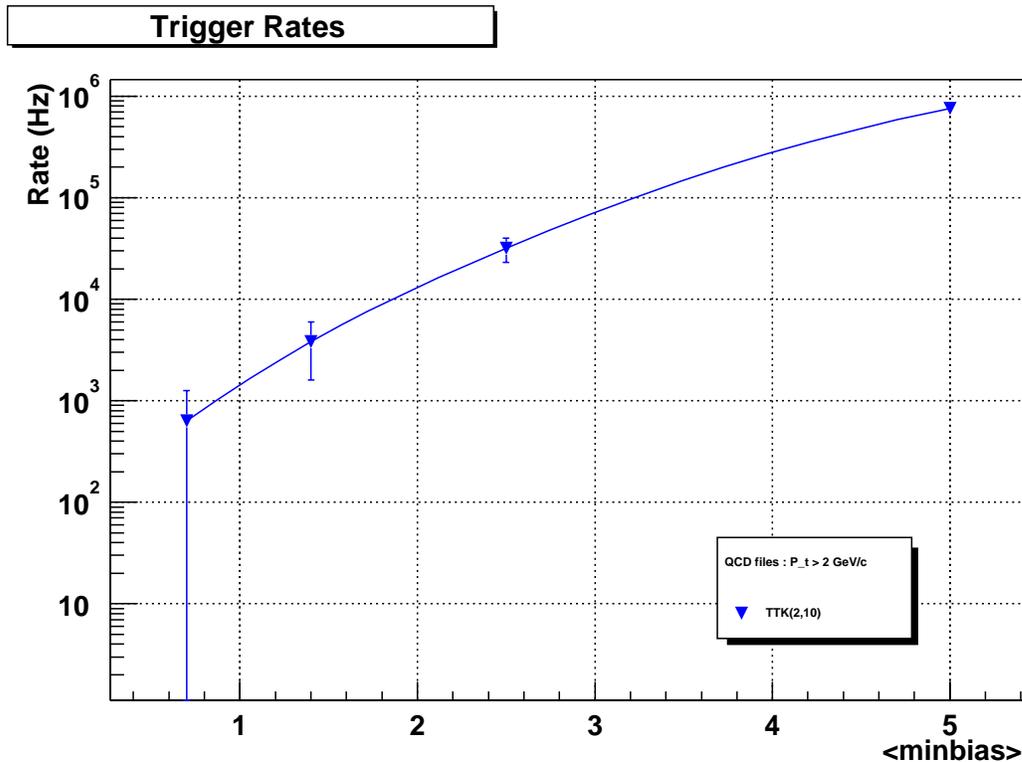


Figure 5. Track trigger rate as a function of the number of underlying minimum bias interactions. TTK(2,10) is a trigger requiring 2 tracks with transverse momentum greater than 10 GeV.

Figure 5 shows the rate for a trigger requiring two tracks with $p_T > 10$ GeV as a function of the number of underlying minimum bias interactions, and hence luminosity. During Run 2b, we expect that the mean number of underlying interactions will be about 5. Figure 5 shows that the tracking trigger rate for the current trigger version is expected to rise dramatically due to accidental hit

combinations yielding fake tracks. This results in an increasingly compromised tracking trigger.

Figure 6 shows the probability for three specific track trigger terms to be satisfied in a given crossing. They are strongly dependent upon the number of underlying minimum bias interactions. These studies indicate that a track trigger based upon the current hardware will be severely compromised under Run 2b conditions. Not shown on the figure, but even more dramatic, is the performance of the 5 GeV threshold track trigger. This is satisfied in more than 95% of beam crossings with 5 minbias overlaid events. It will clearly not be possible to run the current stand-alone track trigger in Run 2b. But much worse, the information available to the muon, electron, and STT becomes severely compromised by such a high rate of fake high- p_T tracks.

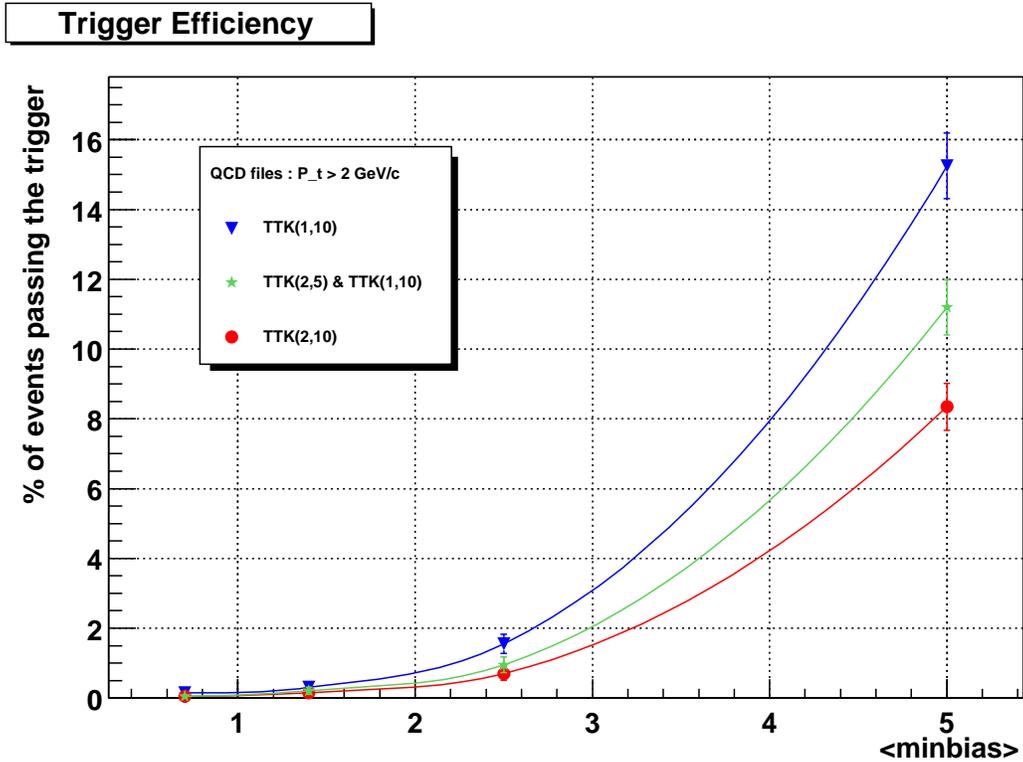


Figure 6. The fraction of events satisfying several track term requirements as a function of the number of minimum bias events overlaid. TTK(n, p_T) is a trigger requiring n tracks with transverse momentum greater than p_T .

To investigate these effects further, we examined a sample of W events, where the W decays to $\mu\nu$. These are representative of a class of physics events that require a high- p_T CFT track at L1. We found a substantial number of fake tracks that generated a track trigger, as expected given the previous results. However, we observed that the rate for these fakes was strongly related to the CFT activity in the sectors where they were found. This effect is clearly

illustrated in Figure 7, which shows how the fake rate varies with the number of doublets hit in a sector.

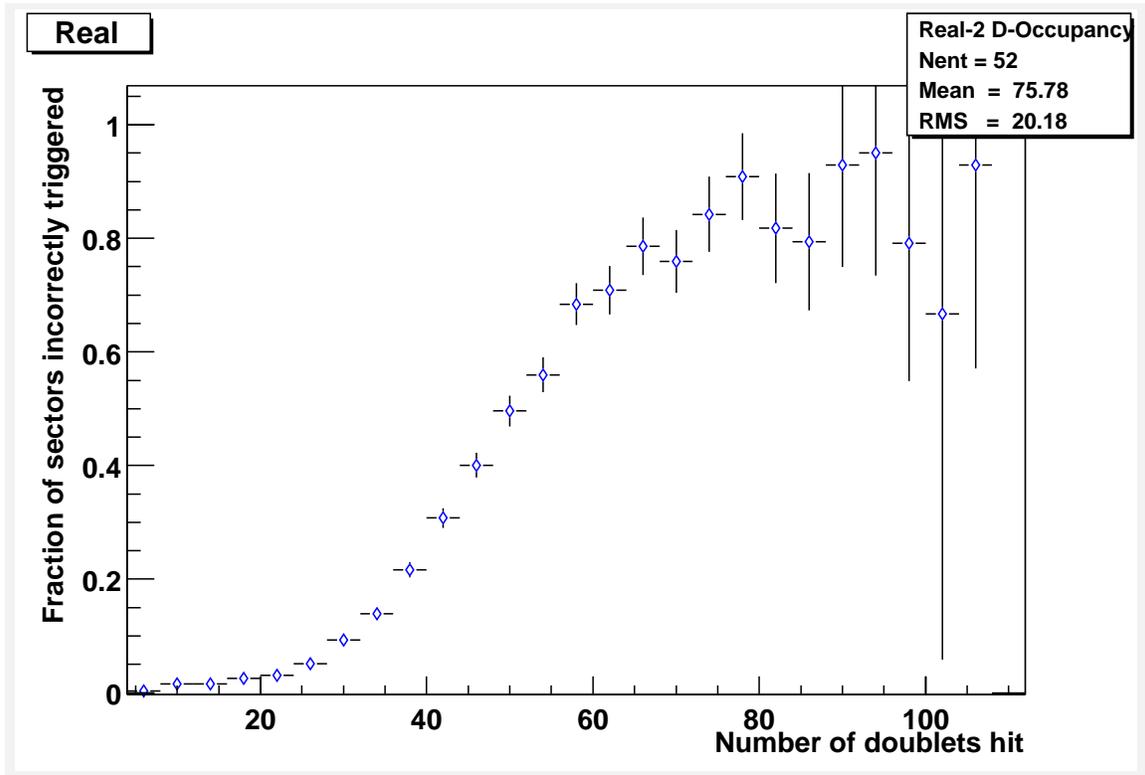


Figure 7. Fake rate vs. number of fiber doublets hit, for $W \rightarrow \mu\nu$ physics events, for a trigger on $p_T > 5$ GeV/c tracks. The plot shows the clear impact of the doublet occupancy rate on the fake trigger rate, which rises dramatically as the sector of interest becomes “busier”. The events used in this constructing this graph were generated using the **PYTHIA** Monte Carlo generator, and included a Poisson distribution of overlaid minimum bias interactions with a mean of 7.5 minimum bias interactions.

It is possible that the strong correlation between the fake rate and the sector doublet occupancy could be used to combat the large background rate at high luminosities. This is indicated in Figure 8 where the occupancy for good and fake tracks are seen to have different distributions of number of doublets hit. It is clear from Figure 7 and Figure 8 that sectors with high levels of doublet occupancy have little real value in a trigger of this nature. While a cut of this type by itself would not fully solve the problems of the current track trigger in Run 2b, it would be of certain value in separating the signal from background rates.

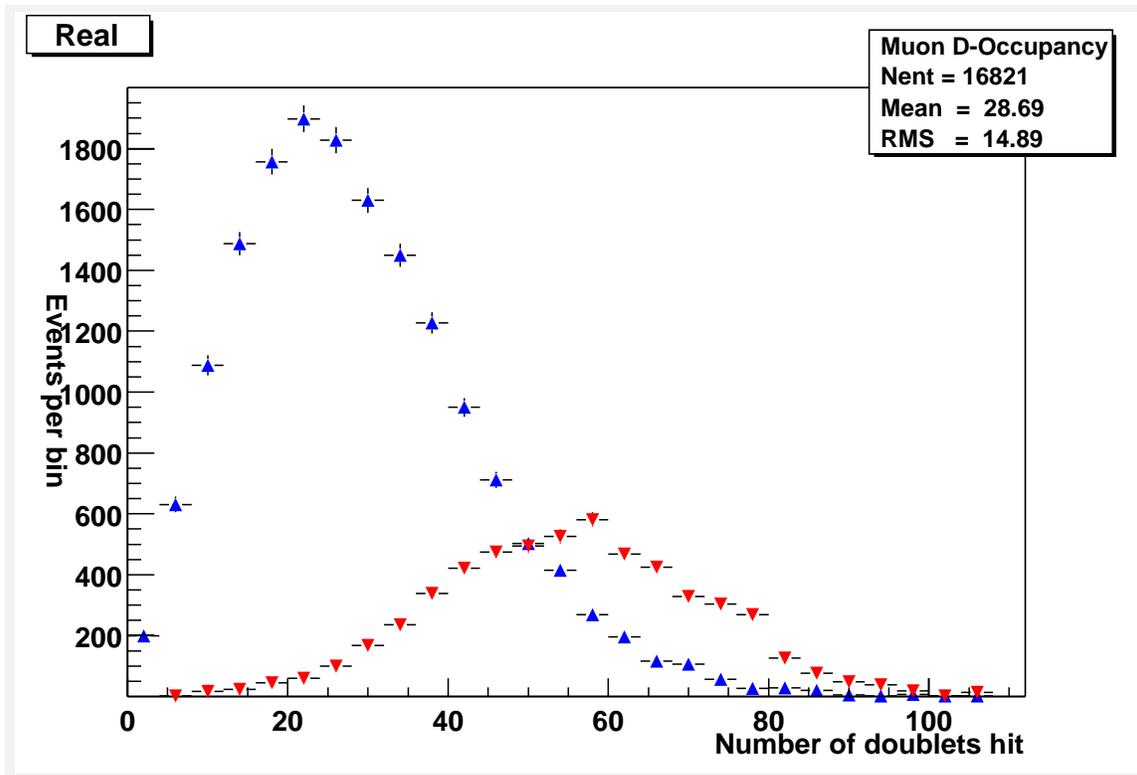


Figure 8. The number of sectors reconstructed with a $p_T > 5$ GeV/c track versus the number of doublets hit within that sector. The sectors where fake tracks have been reconstructed are shown with inverted (red) triangles; the sectors where the tracks have been properly reconstructed are shown with apex up triangles (blue). This plot demonstrates that there is a significant difference between the sectors where fake tracks are reconstructed and those where the tracks are genuine muons.

Based upon these simulations, we believe that the significant numbers of background overlay events in Run 2b and the large CFT occupancy fractions they induce, will compromise performance of the current tracking trigger.

3.3.3 Comments on the CFT Lifetime

The primary radiation damage effect on the CFT is a reduction in the scintillating fiber attenuation length. There is essentially no change in the intrinsic light yield in the scintillator. The expected dose to the CFT as a function of radius was determined from analytical studies, GEANT simulations, and data taken at CDF on a prototype fiber system installed at the end of Run I. From these data we determined that the total dose to the fibers on the CFT inner barrel ($r=20\text{cm}$) would be approximately 150 krad after 30 fb^{-1} . To determine the radiation damage effects on the fiber, we performed both short-term high-rate exposures and long term (1 year), low-rate (14 rad/hr) exposures on sample fibers. Data from both these sets of measurements were in agreement and indicated that the attenuation length of our scintillating fiber would decrease from 5 m at zero dose to 2.3 m at 150 krad. The radiation damage effect is logarithmic in nature, so the effect at 1000 krad further reduces the attenuation length only to 1.6 m.

The light yield of the CFT production fibers was studied in an extensive cosmic ray test. The mean number of photoelectrons (pe) from a single fiber was approximately 12 pe for a waveguide length of 7.7 m and approximately 7 pe for 11.4 m. A Monte Carlo program was used to relate these cosmic ray test results to beam conditions. The fiber attenuation length was degraded as a function of dose following our radiation damage measurements. The Monte Carlo simulated the AFE board performance and used the measured VLPC gains. The results are shown in Table 2. The trigger efficiency is given as a function of the fiber discriminator trigger threshold in fC (7 fC corresponds to approximately 1 pe) and radiation dose. We required 8 out of 8 hits in the CFT axial layers. The CFT fiber discriminator trigger threshold is expected to be below 2 pe (14 fC) for all channels. The numbers in the left hand columns of the table correspond to the full rapidity coverage of the CFT (± 1.6), and those in the right hand columns correspond to the central ± 0.5 units of rapidity. We find that the track trigger efficiency should remain above 95% even after 30 fb^{-1} of accumulated luminosity.

Table 2: Expected trigger efficiency as a function of fiber discriminator threshold for at various radiation exposures. Left hand (right hand) columns correspond to consideration of full (central) region of the tracker. See text for details.

Trig Thresh (fC)	Efficiency							
	0 fb^{-1}		2 fb^{-1}		30 fb^{-1}		90 fb^{-1}	
7	0.997	0.996	0.997	0.995	0.996	0.994	0.994	0.987
10	0.995	0.989	0.992	0.986	0.987	0.979	0.982	0.965
13	0.993	0.985	0.992	0.984	0.986	0.973	0.976	0.955
16	0.987	0.970	0.984	0.968	0.969	0.939	0.953	0.902
21	0.975	0.941	0.969	0.932	0.937	0.874	0.902	0.802

3.4 AFE Board Upgrade for 132 ns Bunch Spacing

The present front-end AFE boards are not capable of discriminating and digitizing signals arriving at 132 ns intervals.

DØ currently uses a special chip to provide a hardware trigger for the Central Fiber Tracker. This SIFT chip is housed within Multi-Chip Modules (MCM) mounted on the AFE boards, together with the SVX2 digitizing chip. The SIFT is upstream of the SVX2, and downstream of the VLPCs, in the CFT readout chain. It provides 16 channels of discriminator output formed before charge transfer to the input of SVX2. For the CFT to perform with an adequate efficiency, collection times of 50 to 70 ns are needed. For these collection times, the performance of the current SIFT chip is marginal when operated at 132 ns. We are therefore designing a modified version of the SIFT and SVX2 chips, needed for Run 2 physics goals with 132 ns accelerator operation.

The new replacement design will replace the MCMs with a small daughter board using one custom integrated circuit, a commercially available ADC, and an

FPGA. Each such board will accommodate 64 fiber inputs, providing discriminated digital outputs for the trigger, and digitized pulse heights for readout. This design is a simplification from the present MCM, and is expected to perform adequately for 132ns crossing operation. In addition, the option of mounting the TriP chips directly to redesigned AFE boards, is also being considered. We give more details below.

3.4.1 Overview

The new SIFT design must have excellent noise performance and threshold uniformity for the CFT, as well as sufficient dynamic range and adequate energy resolution for the preshower detectors. While it might be possible to replace only the chips housed within the MCM, this is a high-risk solution both for design (very high speed, low noise operation of the current MCM is required) and for manufacturing and production (very high yields are necessary in order to contain the cost). As our baseline design, we are pursuing the replacement of the current MCM with a standard printed circuit daughter board containing three new elements that functionally emulate the current SIFT chip: the Trigger and Pipeline (TriP) chip, a high speed ADC for analog readout, and a Field Programmable Gate Array (FPGA) to buffer the data and emulate the current SVX2 chip during readout. In this design, the AFE motherboard would not be modified. We are also considering a design in which the new components would be mounted directly on the AFE board without the need of a daughter board. For this option, the TriP chip would have to be packaged, for example, in a standard thin quad flat pack and new AFE boards would have to be manufactured. Although this latter option would allow for a simpler AFE motherboard design with reduced functionality compared to the present version, it would require a new layout and production cycle, and would therefore be more costly than our current baseline design. A preliminary outline of the costs of these two options, along with sub-project milestones and remarks on the current status, is given in Table 3 and Table 4.

3.4.2 SIFT Replacement: the TriP ASIC

This TriP chip will be a custom IC manufactured in the TSMC 0.25 micron process, powered by a 2.5 - 3V supply. The new chip is simple in concept and design, and is based on several already-existing sub-designs of other chips. It would replace the four SIFT chips on the current MCMs with a single 64 channel chip that performs the two functions: (1) the trigger output for every channel above a preset threshold, and (2) a pipeline delay so that analog information is available for channels above threshold on receipt of a L1 accept decision. The rest of the devices on the daughter board are readily available commercial parts.

3.4.2.1 Amplifier/ Discriminator

Because of the possibility of large signals from the detectors, the preamplifier needs to be reset after every crossing. The input charge range is 4 to 500 fC. This circuit will be used in both the CFT and preshower detectors; the latter produce signals that are up to 16 times larger than for the CFT. Thus, the preamplifier will have programmable gain. Four binary-weighted capacitors that

can be switched into the amplifier feedback loop will provide the desired flexibility for setting the gain range.

The discriminator will be set as a fraction of the selected full range of the preamp. It will be digitally controlled and have approximately 8 bit resolution. The discriminators will be uniform across the chip to 1%. The chip will include a provision for test inputs to allow a known amount of charge to be injected into selected channels. The input will be AC coupled and will present a capacitive load of 30 to 40 pF. Signal rise time of the VLPC is less than 600 ps, so rise time at the input is entirely determined by the input capacitance. The chips will collect 95% of the signal charge in 50 to 75ns.

64 bits of discriminator information must be sent from the MCM to the trigger system every crossing. It is necessary to output the discriminator bits outside the 75 ns interval devoted to charge collection, while the preamp is inactive. If the discriminator outputs are multiplexed by a factor of two in an effort to reduce the number of lines required, the switching frequency of the discriminator bits is still manageable: lines would switch at a maximum frequency of once every 25ns. The discriminator outputs would be sent to the FPGA on the same daughter, board only a few centimeters away, and would require only about 7% of the energy of the present design.

3.4.2.2 Pipeline and MUX

The TriP chip will use the pipeline designed for the SVX4 chip being designed for the silicon detector for Run 2b, including the on-chip bypass capacitors. This 47-deep pipeline is adequate for this application. Only minimal modifications will be required to match the full-scale output of the preamp. The 64 channels will be multiplexed out to an external bus, which will be connected to a commercial ADC. It is possible to fit two dual input 10 bit ADCs on the daughter board: this will allow the analog outputs to work at 7.6 MHz with four 16-to-1 multiplexers on the TriP chip.

3.4.3 High Speed ADC

This ADC envisioned is a commercially available, 10 bit, dual input device with impedance inputs and less than 10 pF input capacitance. The device is capable of 20 million samples per second (MSPS) but will run at a frequency of only 7.6 MSPS. With two ADCs per daughter board, the time required to digitize 64 channels is 2.2 μ s, approximately the same as for the SVX2 chip. The ADC digital outputs will be connected to a small FPGA on the daughter board for further processing before readout. At least two component parts from different manufacturers are available that meet all the design requirements related to power needs and consumption, space, speed, performance and cost.

3.4.4 FPGA

Field Programmable Gate Arrays have developed rapidly in the last few years. A small FPGA placed on the daughter board can provide the processing power and speed needed to emulate an SVX2. The FPGA provides the

necessary data storage for buffering the discriminator information during the trigger latency, and flexible I/O to provide level translation and control functions.

The FPGA is connected to both the TriP chip and the ADCs on the daughter board. It also interfaces with the SVX bus and the trigger data path. The FPGA senses the MODE lines of the SVX bus to control the rest of the devices on the daughter board. In ACQUIRE mode, the TriP chip will output the discriminator information on 32 lines during a part of the crossing, using LVCMOS2 or similar signal levels (2 bits per line, time-multiplexed.) The FPGA will latch the 64 bits, add 7 bits of status information, and repackage the bits into 10-bit-wide packets that will be sent to the motherboard at 53 MHz and then passed on to the LVDS drivers. At the same time, the discriminator bits will be stored in the FPGA-embedded RAM blocks so the information is available for readout to the offline system. Even a small FPGA, such as the Xilinx XC2S30, has 24KB of block RAM, much more than is required to implement a 32-stage digital pipeline for the 64 trigger bits. However, the RAM will be used for other purposes as well. Once a L1 accept signal is received, the SVX bus will change from the ACQUIRE mode to the DIGITIZE mode. The FPGA would sense this mode change, stop the analog pipeline inside the TriP chip, and start the analog multiplexers and the ADCs. The FPGA would collect the digital data from the ADCs; reformat the 10 bits into a floating-point format, and temporarily save it in RAM pending readout. Once the READOUT phase starts, the FPGA would emulate the SVX functionality by generating the chip ID, status and channel ID, and retrieving the discriminator and analog information from the on-chip RAM and putting it on the SVX bus.

3.4.5 Preliminary Cost Estimate

As described above, there are two viable options for replacement of the SIFT. We have rejected the replacement of the SIFT on existing MCMs as the technical risks are serious. In option 1 we would replace the MCM with daughter boards. In this option, the TriP chip can be used in bare-die form by wire-bonding it directly onto the daughter board or in packaged form prior to mounting it on the daughter cards. The current AFE boards would be used in this option, but the existing MCMs would have to be removed and the boards restuffed with the new daughter cards. There is some technical risk associated with the MCM removal procedure that is a concern, although initial tests on relatively small samples have yielded encouraging results. In option 2 the AFE boards would be redesigned to accommodate a direct mounted TriP chip. In this version, the daughter boards would not be needed, and the TriP must be packaged. The space on the AFE board that would be needed for the redesigned SIFT would be exactly the same as the area occupied by the daughter board mounted on the existing AFE board in option 1. The rest of the AFE replacement board could use the same layout and components as those in the present version. There would be some engineering effort required to design and lay out the new AFE, but these changes consist of relatively straightforward modifications to the present design. We estimate the cost for each of the options in Table 3 below. At this time, we consider removal of large numbers of MCMs a risky procedure

that we would like to avoid. We therefore have chosen option 2 as our baseline option for the SIFT replacement.

The current plan for the TriP ASIC submission takes advantage of a concurrent submission of a similar chip already being planned and paid for by the Laboratory in conjunction with the BTeV experiment. Currently, we expect that DØ will fabricate the TriP chip on the tail end of the BTeV run to save the cost associated with an additional fabrication phase. This should yield more parts than are needed for the SIFT project if they function as expected. Our experience indicates, however, that a second submission will be needed in order to obtain chips that function to specification; we therefore include in the cost estimate a line item covering this additional submission.

Table 3. Preliminary cost estimate for the SIFT replacement. Total cost for option (1) and the AFE replacement option (2) are shown (see text for details). Estimated cost for outside engineering known to be required for layout work is included. Additional manpower is not included.

Item		M&S			Contingency		Total Cost (\$k)	
		number	Unit cost	M&S Total	Cost			
#	Description	unit	(incl. spares)	(\$)	(\$k)	%	(\$k)	
1	New parts (FPGA, ADCs, etc.)	MCM	2000	40	80	50	40	120
2	Replacement daughter boards	Ea	2000	150	300	50	150	450
3	TriP ASIC packaging	Ea	2200	15	33	50	16.5	49.5
4	New AFE motherboards	Ea	240	1,500	360	50	180	540
5	TriP ASCI (see notes)	Lot	1	185,000	185	25	231	231
6	Layout Engineering	Lot	1	30,000	30	10	30	60
1,2,5,6	Option 1	Total cost			\$595			\$861
1,3,4,5,6	Option 2	Total cost			\$688			\$1001

3.4.6 Milestones

In Table 4 we show a series of milestones extracted from a preliminary schedule for the SIFT replacement. This schedule assumes two rounds of daughter board prototypes and two rounds of ASIC submissions for the TriP chip.

Table 4: Preliminary milestones for the SIFT replacement project.

1	1-Sep-01	Prototype daughter board available
2	15-Oct-01	AFE-daughter board integration demonstrated
3	20-Dec-01	TriP ASIC submitted to fab
4	10-Jan-02	Pre-production daughter board submitted for manufacture
5	15-Apr-02	AFE operation at 132ns demonstrated
6	15-Jun-02	Second ASIC submission
7	15-Jul-02	Daughter boards submitted for production
8	1-Oct-02	Final ASIC available (diced and tested)
9	20-Dec-02	Daughter boards ready for mounting on AFE

An analog engineer experienced in chip design from the Electrical Engineering Department in the PPD has been working on the design of the TriP chip since early summer, 2001. The September 1 milestone, by which a prototype daughter board was to be made available, was met. The next critical date is the initial submission of the TriP chip on December 20, 2001. Work is progressing at a rate consistent with meeting this milestone. The December 20, 2002 end date is still roughly consistent with the latest plan for the changeover of the accelerator to accommodate 132 ns running. However, the schedule contingency is small, and efforts are underway to identify means by which portions of the project might be accelerated. We note that the schedule shown assumes two ASIC submissions – this may in fact prove to be unnecessary, and therefore might prove to be a source of schedule contingency for future use.

The SIFT replacement project was reviewed by the Run 2b Project Management in September 2001. The review committee consisted of three Fermilab engineers from outside DØ, and two DØ physicists.

3.5 Overview of Options for Track Trigger

As demonstrated above, the primary concern with the track trigger is the increase in rate for fake tracks as the tracker occupancy grows. Since the current track trigger requires hits in all 8 axial doublet layers, the only path to improving trigger rejection is to improve the trigger selectivity by incorporating additional information into the trigger algorithm. The short timescale until the beginning of Run 2b and resource limitations conspire to make it unlikely that the physical granularity of the fiber tracker can be improved, or that additional tracking layers can be added to the CFT. A variety of approaches for increasing the track trigger selectivity were investigated as part of this report:

1. Increasing the number of tracking layers by treating the Central Preshower (CPS) axial strips as a ninth layer in the tracking trigger. A study of this option is presented in section 3.6.
2. Incorporating the information from the CFT stereo view fibers in the tracking trigger. A particular implementation of this concept is presented in Section 3.7.
3. Improving the granularity of the tracking trigger by implementing the individual single fiber hits from the axial fibers in the trigger equations rather than using the fiber doublet hits. Two implementations of the singlet equations are presented in Section 3.8.
4. Matching the tracking information to other surrounding detectors. The studies of track calorimeter matching are presented Section 4.8 as part of the calorimeter trigger upgrades.

Studies of all four options are presented in this report. While options 1 and 2 provide some increase in trigger selectivity, our studies indicate that options 3 and 4 show the greatest promise for improving the selectivity of the tracking trigger and are the focus of our current efforts.

3.6 Axial CPS as Ninth Layer

3.6.1 Concept and Implications

The CPS detector has a similar structure to the CFT. Consequently, the axial layer of the CPS might be employed as an effective ninth tracking layer for triggering purposes. If the AFE boards used to readout the CPS had dual threshold capability with one threshold set for efficient MIP recognition, this option could present minimal tradeoff. However, the current design of the AFE2 boards provides only one threshold per channel, and the minimum threshold that can be set is in the vicinity of 1-2 MIPs, too high to see minimum ionizing tracks efficiently. In any case, the η range of this nine-layer tracker would be ± 1.3 , while the eight-layer tracker extends out to ± 1.6 . This corresponds to an $\approx 20\%$ reduction in acceptance.

3.6.2 Implementation

The implementation of the axial CPS layers as a ninth layer of the tracking trigger is a relatively straightforward task. The threshold of the CPS discriminators on the appropriate AFE boards would need to be lowered to a level such that minimum ionizing particles satisfy the discriminator threshold. A minimum ionizing particle deposits on average about 1.2 MeV in a CPS doublet, and as described below, ranges of thresholds below that level were studied.

3.6.3 Efficiency/Acceptance

The efficiency of this trigger was studied using samples of between 500 and 1000 single muon events which also contained a Poisson distribution of (ISAJET) minimum bias overlay interactions with a mean of five. Table 5 shows that this nine-layer trigger is better than 80% efficient for axial CPS hit thresholds below

0.25 MeV. The single muons in the Monte Carlo sample were generated in the range $-1.2 < \eta < 1.2$, to isolate the CPS acceptance issue from the performance of the nine layer tracking trigger.

Table 5. Efficiency of the tracking trigger for 15 GeV muons within the acceptance of the CPS (in percent) when the axial CPS information is used as the ninth layer in the tracking trigger.

Axial CPS Hit Threshold	9 Hit Track $p_T \geq 10$ GeV	≥ 8 Hit Track $p_T \geq 10$ GeV	9 Hit Track $p_T \geq 5$ GeV	≥ 8 Hit Track $p_T \geq 5$ GeV
1.0 MeV	52.4	93.2	53.6	94.0
0.5 MeV	75.5	95.3	76.0	95.3
0.25 MeV	82.1	94.9	83.7	94.9
0.15 MeV	79.7	95.4	81.3	96.3

3.6.4 Rates and Rejection Improvements

To study the potential improvements provided by this nine layer trigger, Monte Carlo samples of QCD events with a minimum p_T of 2 GeV were generated and overlaid with a Poisson distribution of (ISAJET) minimum bias interactions with a mean of five minimum bias interactions. The improvement in rejecting fake tracks is fairly minimal. The probability that certain CTT terms were satisfied for these events is shown in Table 6. Using a threshold which provides almost no efficiency for real tracks, the rejection of fake tracks is about 35%. If the threshold is reduced so that the efficiency for real tracks is larger than 80%, then the rejection of fake tracks is about 17%.

The fact that the fake rates do not increase as the CPS hit threshold is reduced from 0.25 MeV to 0.15 MeV is likely an artifact of energy thresholds in the Monte Carlo, and may account for the observation that the efficiency of the nine hit tracks as reported in Table 5 fails to reach the same level as the 8 hit tracks.

Table 6. Percentage of events from the 2 GeV QCD sample that satisfy various trigger requirements as a function of the threshold for the hit in the axial CPS which is serving as the ninth layer of the tracking trigger in this simulation.

Axial CPS Hit Threshold	9 Hit Track $p_T \geq 10$ GeV	≥ 8 Hit Track $p_T \geq 10$ GeV	9 Hit Track $p_T \geq 5$ GeV	≥ 8 Hit Track $p_T \geq 5$ GeV
3.0 MeV	11.6	15.6	18.0	24.8
1.0 MeV	13.6	17.6	19.0	25.0
0.5 MeV	15.2	18.0	22.8	28.0
0.25 MeV	15.0	17.6	21.0	25.0
0.15 MeV	15.0	17.6	21.0	25.0

3.6.5 Conclusions

The 15 to 20% background rate rejection achieved by using the axial CPS as a ninth layer in the tracking trigger is insufficient to meet our Run 2b needs, while degrading our ability to use the CPS for EM identification. We have therefore eliminated this option from further consideration.

3.7 Stereo Track Processor

3.7.1 Concept

A second strategy to reduce the L1 CTT fake rate would implement a second fast digital processor that can incorporate the hits in the stereo layers of the CFT in the L1 CTT. This upgrade has the additional advantage that three-dimensional tracks would be available at Level 1 for matching to calorimeter hits and even allowing invariant mass calculations at L1.

The overall strategy for adding stereo hit information to the axial tracks is predicated on the availability of the axial track parameters (ϕ and p_T) in order to make the problem tractable. Then, a pattern of 7 or 8 stereo hits can be matched to the pre-determined trajectory of the axial track. The algorithm is shown schematically in Figure 9.

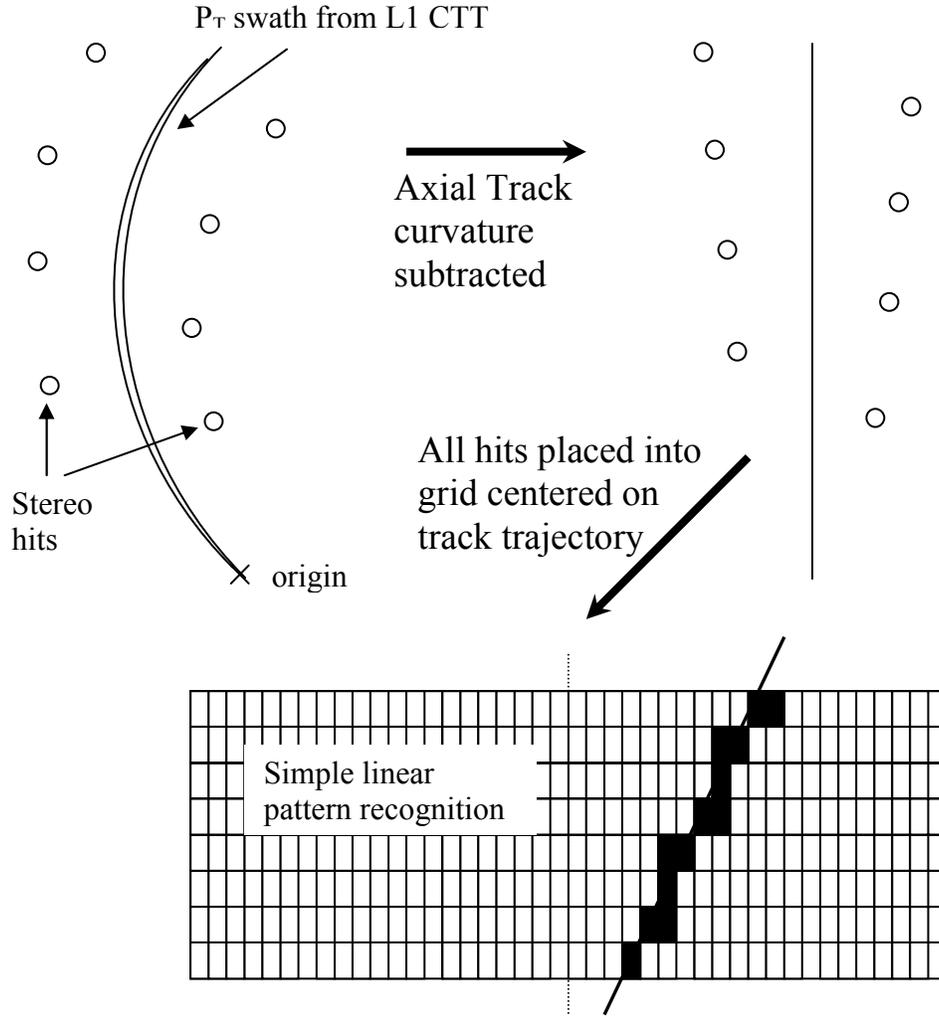


Figure 9. Schematic representation of the algorithm used to attach stereo hits to an axial seed track. See text for a detailed description.

The stereo tracking algorithm makes use of the linear relation between the difference in stereo ($r\phi_s$) and axial ($r\phi_a$) fiber indices and the r-z track parameters z_0 and $\cot(\theta)$: $r\phi_s - r\phi_a = (z_0 + r\cot(\theta)) / \tan(\lambda)$ where r is the radius of the layer and $\tan(\lambda)$ is the stereo angle. First, axial tracks are received from the current L1 CTT. The information contained in a “track” consists of a fiber index on the outermost CFT cylinder and, for high-momentum tracks, a range in p_T allowed by the pattern of hits. The fiber index provides precise ϕ location. This, combined with the constraint that the track must pass through the origin, allows the definition of a crescent-shaped region in the r - ϕ plane, which should contain the true trajectory of the axial track. In order to reduce the complexity of the problem, the centroid of the trajectory is defined as the locus of the track in each axial layer. Then, all CFT stereo fibers that cross the central axial fiber are searched for hits. The difference in fiber indices between the stereo and axial fibers is computed for each stereo hit. In this space, the U and V hits form

approximately straight lines on either side of the straightened axial track, as shown in Figure 9. The U-fiber hits, which have the opposite sign for $\tan(\lambda)$, are flipped about the central trajectory, and the offset of all single-fiber hits from the central trajectory is entered into a grid. This is done for all accessible stereo fibers. The track-finding algorithm reduces to a simple search for 7 or 8 hits connected in a straight line. To reduce the combinatoric background, a χ^2 fit is done separately to U and V hits to determine whether or not they lie in straight lines around the central trajectory. (Small errors in the centroid position resulting from imprecise knowledge of the track p_T can result in different slopes for the different sets of stereo hits.) In the results presented below, no attempt has been made to merge neighboring hits into clusters; only the single fiber hits are used for this track finding.

In the results that follow, the added stereo hits have only been used to confirm the validity of the input L1 CTT axial tracks. No attempt has been made to examine the stereo track parameters and place cuts on the z position where the track crosses the beam line or on the track η . In any case, the Monte Carlo studies show that tracks with extreme values of z or η are a relatively small fraction of the total number of fake tracks. The stereo tracking algorithm could potentially make available the z coordinate and track η .

3.7.2 Simulation

A simulation of the stereo tracking algorithm was inserted into the existing trigger simulation in order to make as realistic an estimate as possible of the actual operating conditions. Axial tracks from the L1 CTT simulation code were fed to a Stereo Track Processor (STP) that executed the algorithm described above. High efficiency (99%) was achieved for matching stereo hits to axial tracks found in high- p_T single muon events.

In order to estimate the additional rejection against fake tracks provided by the stereo hit information, the rate of tracks found by the STP is compared with that from the current L1 CTT. This is shown in Table 7 for single high- p_T muon events with *fixed* numbers of minimum bias interactions overlaid. The rate calculated corresponds to the number of fake tracks with $p_T > 5$ GeV generated per event. The minimum bias events in these samples were generated by **ISAJET** and potentially overestimate the occupancy of the CFT by a small amount. For this table, 8 out of 8 possible stereo hits are required to confirm an axial track. This information is shown graphically in Figure 10.

Table 7. The effect of minimum bias events on the track trigger rate. The fake track rate is the number of fake tracks with $p_T > 5$ GeV generated per event. The column labeled “L1 CTT” is the rate of fake tracks from the default Level 1 track trigger. The column labeled “after Stereo Hits” gives the rate of fake tracks with the combined stereo and axial track triggers. The final column gives the fraction of fake tracks produced by the axial trigger that are rejected by the addition of stereo hits.

# min bias events	L1 CTT Fake track rate	Fake track rate after Stereo Hits	Extra rejection
1	0.136	0.001	0.99
2	0.235	0	1.00
3	0.347	0.057	0.84
4	0.578	0.199	0.66
5	0.972	0.377	0.61

Reduction of L1CTT Rate with UV Information

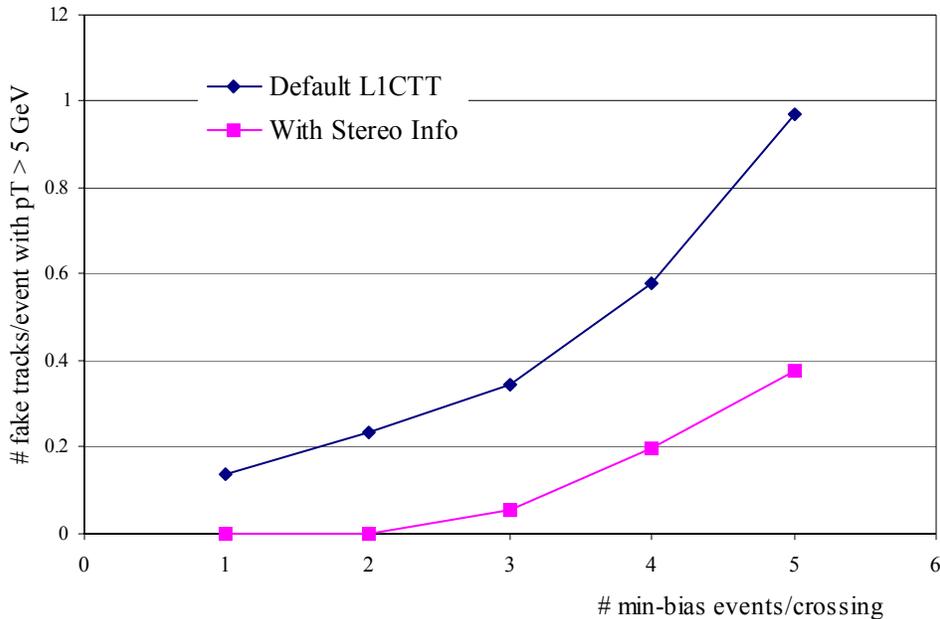


Figure 10. The additional rejection power provided by adding stereo hits to the found axial tracks. The rate of fake tracks with $p_T > 5$ GeV generated per event is plotted for the default L1 CTT and after the addition of stereo hits.

Studies requiring only 7 out of 8 stereo hits to form a valid track show that the extra rejection provided by the stereo information drops from 61% to 26% for a sample of high- p_T muon events with exactly 5 minimum bias events overlaid.

3.7.3 Implementation

Due to the stereo angle, each axial fiber can cross up to 300 fibers in the outer CFT layers, making the number of possible track-hit combinations very large. In addition, since such a large fraction of the CFT stereo hits will need to be compared to an arbitrary axial track, much of the total stereo hit information will need to be available on any Stereo track-finding board. These considerations lead one to an architecture where all of the stereo data is sent to a small number of processing boards where the actual track finding takes place. The data-transfer rate requirements are severe, but presumably tractable, especially since the stereo information can be transferred while waiting for the axial track parameters to arrive from the current axial track-finding boards. Large buffers and substantial on-board data buses would be required in order to hold and process the large quantity of data. A possible schematic is shown in Figure 11. Essentially, a parallel data path very similar to what will exist for the L1 CTT would need to be built, but without the added complexity of the “mixer box” that sorts the discriminator signals into sectors. Moving the SIFT signals from the AFE boards for the stereo layers is relatively simple; sorting and processing them once they reach the track-finding boards will require a substantial engineering effort.

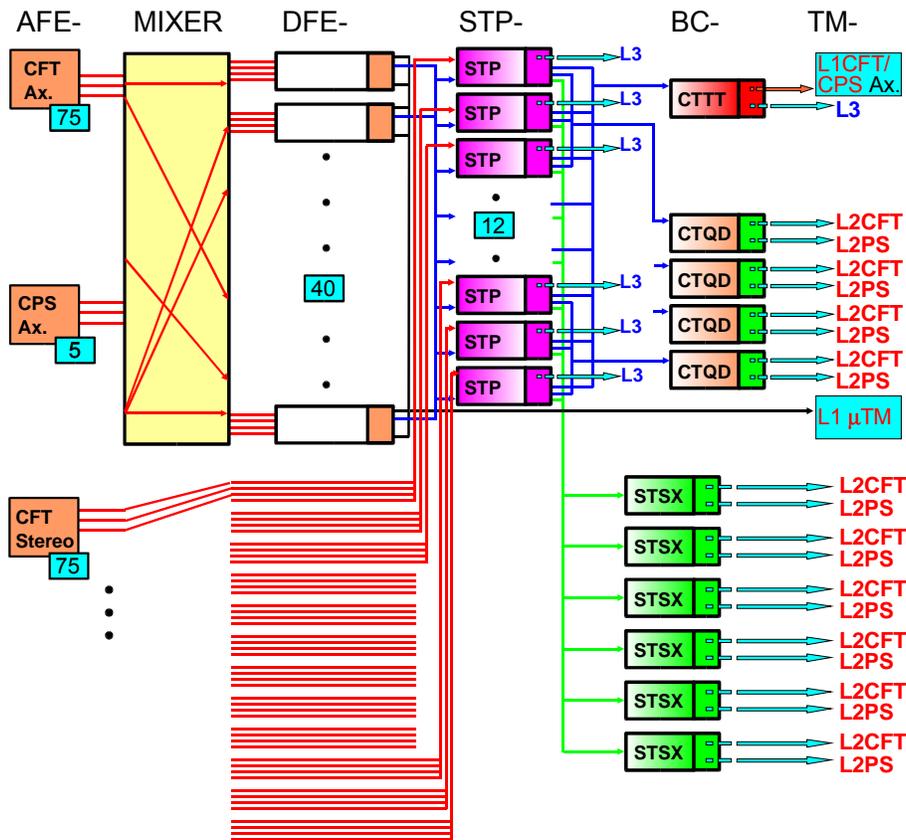


Figure 11. Schematic diagram of the implementation of stereo tracking in the trigger.

This upgrade would also require small modifications to the transition boards at the back end of the current L1 CTT system so that the axial track candidates could be shipped to the new stereo track processor. The inputs to the L2STT would also be modified so that L2 could take full advantage of the refined track information.

3.7.4 Conclusions

The addition of stereo information provides good rejection of fake tracks at high transverse momentum, but the high complexity and correspondingly large expense of the system probably does not justify its construction given the modest expected reduction in trigger rate.

3.8 Singlet Equations

3.8.1 Concept

The idea behind singlet equations is illustrated in Figure 3, which shows a fragment of a CFT doublet layer. The thick black lines mark the area corresponding to a doublet hit. As one can see from Figure 3, the doublet is a little larger than the fiber diameter, which suggests that roads based on single fibers will be a little narrower and therefore have reduced fake probability. Also, if one requires a particular single fiber hit pattern in the doublet hit, the size of the hit becomes even smaller (thin dotted lines in Figure 3) promising even more background rejection.

It is clear, however, that increased granularity of the trigger leads also to an increase in the number of equations. A concrete estimate of the FPGA resources needed is yet to be done. Keeping in mind this uncertainty we considered two trigger configurations: when four out of eight CFT layers are treated as pairs of singlet layers, giving effectively a 12 layer trigger, and the all-singlet case (*i.e.* 16 layer). For the first case, the hits from axial fibers mounted on the inner four cylinders (cylinders A, B, C, and D) were treated as singlets, while the hits from axial fibers on the outer four cylinders (cylinders E through H) were treated as doublets in the same manner as the Run 2a CTT. Equations for both configurations were generated. The probability that a track will have ≥ 8 , ≥ 9 , ≥ 10 , ≥ 11 and 12 hits out of 12 possible for the first trigger scheme is shown in Figure 12. The probability that a track will have ≥ 8 , ≥ 10 , ≥ 11 , ≥ 12 and 13 hits out of 16 possible for the second trigger scheme is shown in Figure 13. In both cases, it is assumed that fibers are 100% efficient.

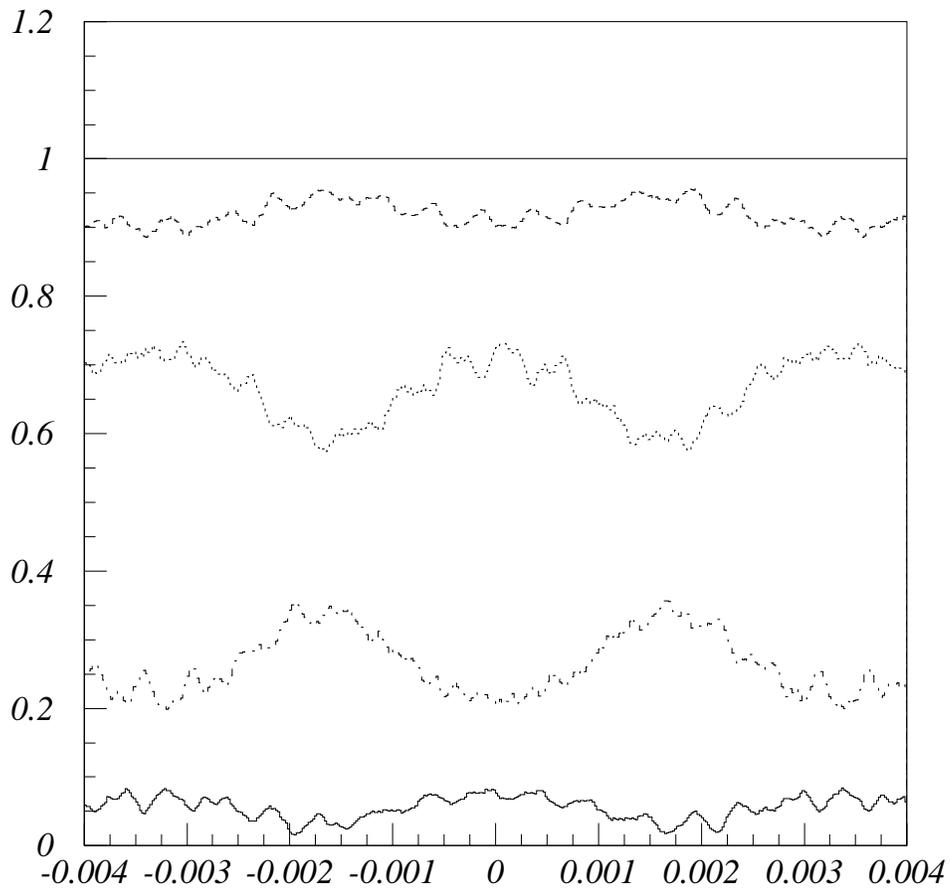


Figure 12. Geometrical acceptance for a charged particle to satisfy a ≥ 8 (solid line), ≥ 9 (dashed curve), ≥ 10 (dotted curve), ≥ 11 (dot-dashed curve) and ≥ 12 (solid curve) hit requirement in the 12-trigger layer configuration, versus the particle track sagita, $s = 0.02 \cdot e / p_T$.

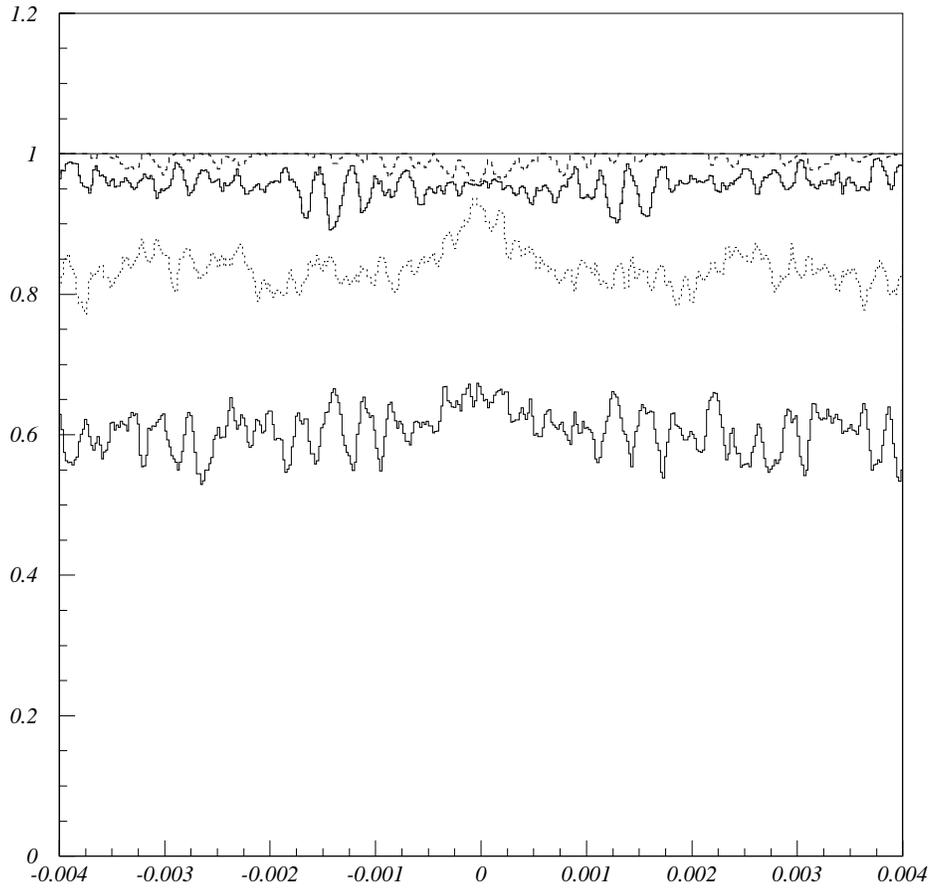


Figure 13. Geometrical acceptance for a charged particle to satisfy a ≥ 8 (solid line), ≥ 10 (dashed curve), ≥ 11 (dotted curve), ≥ 12 (dot-dashed curve) and 13 (solid curve) hit requirement in the 16-trigger layer configuration, versus the particle track sagita, $s = 0.02 \cdot e / p_T$.

The maximum rejection achievable, compared to the standard doublet equations, can be estimated without complicated simulation by comparing sets of singlet and doublet equations as follows. In an equation a doublet hit can originate from four different combinations of single fiber hits (see the four different regions indicated by the dashed lines between the thick black lines in Figure 3). The combination of pitch and active fiber diameter is such that all four combinations are about equally probable. Therefore each doublet equation can be represented as a set of $4^4 = 256$ equations in the 12-layer trigger configuration. Some of these expanded equations will be identical to some of the true singlet equations. Some will just have eight or more hits in common with them. Since the background rate is expected to be proportional to the number of equations, the additional rejection from incorporating fiber singlets can be estimated as the fraction of expanded equations that can be matched to the true singlet equations. We determined this fraction considering all true singlet roads,

only those with nine or more hits and then those with ten or more hits to be 0.44, 0.18 and 0.03 respectively. From Figure 12 these three cases correspond to trigger efficiencies of 100%, ~93%, and ~65%.

These numbers, though encouraging, may be too optimistic in two ways. First, the impact of imperfect fiber efficiency is a little worse for singlet than for doublet equations. Second, singlet roads require that certain fibers not be hit, which can introduce inefficiency in a high occupancy environment⁴.

Both concerns can be addressed and their impact reduced. One can soften requirements on the match of the road with hit fibers. One can increase the number of the roads to pick up the tracks that would otherwise be lost due to fiber inefficiency or extra hits. This presents an optimization problem that can be rigorously solved. The optimization parameters are the amount of FPGA resources (*i.e.* number of equations, matching algorithm and number of trigger layers), signal efficiency, and background rate.

Such an optimization has not yet been performed. For this document, we considered a conservative approach. The singlet road fires if 1) the doublet road which this singlet road corresponds to fires and 2) if more than eight elements of the singlet road fire. The second requirement was varied to optimize signal to background ratio. The first requirement guarantees that each of the doublet layers has a hit and is also a disguised veto requirement on certain neighboring fiber hits.

3.8.2 Rates and Rejection Improvements and Efficiency

The existing trigger simulation was adapted to make a realistic estimate of the trigger performance. Single muons were generated, overlaid on events containing exactly five (ISAJET) minimum bias interactions and put through the detailed $D\bar{O}$ simulation. They were then put through the modified trigger simulator. Single fiber efficiency is still assumed to be perfect. The fraction of events that had a trigger track matching the muon measures the trigger efficiency, while the number of high p_T tracks that do not match the generated muons measures the accidental background rate.

The results of the procedure described above for a 1300 event sample of 12 GeV muons are summarized in Table 8 for 12-layer and Table 9 for 16-layer trigger. For the case of 12-layer equations with ≥ 9 out of 12 hits, the background is reduced by a factor of about two without significant loss of efficiency. For 16-layer case the improvement is larger and is about factor of five for high p_T tracks.

Note also, that the fraction of mis-reconstructed muons, *i.e.* muons which give trigger in the wrong p_T bin is also reduced when going to singlet equations, especially for 16-layer case. It is very important for STT, which depends on the quality of the seed tracks from L1CTT.

⁴ Note that current triggering scheme also requires that some fibers will not be hit. This requirement is implemented in the doublet formation phase.

Table 8. Numbers of events (out of 1300) that satisfy various track trigger requirements for an implementation of the tracking trigger that uses singlets for the axial fibers on the inner four cylinders and doublets for the axial fibers on the outer four cylinders. TTK(n, p_T) is a trigger requiring n tracks with transverse momentum greater than p_T .

	Doublet Equations	Singlet Equations	Singlet Equations (≥ 9 of 12)	Singlet Equations (≥ 10 of 12)
# matched $p_T > 10$	1199	1200	1191	1019
# matched $5 < p_T < 10$	37	14	16	26
# fakes $p_T > 10$	91	61	50	31
# fakes $5 < p_T < 10$	206	136	124	77
Fake TTK(1,10)	79	55	45	31
Fake TTK(2,10)	10	5	4	0
Fake TTK(1,5)	159	115	103	69
Fake TTK(2,5)	34	18	18	7

Table 9. Numbers of events (out of 1300) that satisfy various track trigger requirements for a trigger based upon singlet equations for all sixteen possible axial layers. TTK(n, p_T) is a trigger requiring n tracks with transverse momentum greater than p_T .

	Doublet Equations	Singlet Equations (≥ 10 of 16)	Singlet Equations (≥ 11 of 16)	Singlet Equations (≥ 12 of 16)
# matched $p_T > 10$	1199	1210	1172	1046
# matched $5 < p_T < 10$	37	5	5	4
# fakes $p_T > 10$	91	26	16	10
# fakes $5 < p_T < 10$	206	70	33	21
Fake TTK(1,10)	79	26	16	10
Fake TTK(2,10)	10	0	0	0
Fake TTK(1,5)	159	63	47	30
Fake TTK(2,5)	34	7	2	1

3.8.3 Implementation, Cost & Schedule

The implementation, cost and schedule depends largely on the algorithm chosen and how much FPGA chip resources that algorithm requires. For an

algorithm requiring a modest increase in resources, the present daughter boards (DB) could be reworked and reused. This would be accomplished by removing the present FPGA chips that are in Ball Grid Array (BGA) packages and mounting new ones. If the algorithm were more complicated and larger, so more powerful chips with new footprints were required, then the daughter boards would also have to be replaced. Preliminary cost estimates for these two options, which are based on our experience fabricating and instrumenting the current boards, are shown in Table 10 and Table 11 below.

Table 10: Preliminary cost estimate for upgrade to the track trigger associated with the handling of fiber singlets that does not include replacement of the daughter boards. A contingency of 50% is applied.

Item/process	Unit Cost (\$)	# Required	Total Cost (\$k)	Total Cost + 50% Contingency (\$k)
Remove FPGA	20	350	7	10.5
Remount FPGA	20	350	7	10.5
Purchase new FPGA	500	350	175	263
<i>TOTAL</i>			<i>\$189</i>	<i>\$284</i>

Table 11: Preliminary cost estimate for upgrade to the track trigger associated with the handling of fiber singlets that includes replacement of the daughter boards. A contingency of 50% is applied.

Item/process	Unit Cost (\$)	# Required	Total Cost (\$k)	Total Cost + 50% Contingency (\$k)
Fabricate/stuff new Daughter Boards	500	88	44	66
Purchase new FPGA	900	350	315	473
<i>TOTAL</i>			<i>\$360</i>	<i>\$540</i>

It should be pointed out that this upgrade affects only the 88 DFEA daughter boards. All of the AFE, MB and other DFE type boards are not changed or modified in any way. The engineering time associated with this FPGA upgrade is consequently of limited scope and the production is limited to a single board series; much of the effort and resources will necessarily be focused on the algorithm logic and FPGA programming. We have selected Option 2 (replacement of the daughter boards) as the preferred choice since it avoids the technical and schedule risk associated with replacing the FPGAs on existing daughter boards and allows the use of more powerful FPGAs. A preliminary schedule for replacing the daughter boards is given in Table 12.

Table 12. Preliminary schedule for the fiber singlet DFEA upgrade.

Prototype algorithm coded and simulated using FPGA simulation tools	2/02
Target algorithm coded and simulated using FPGA simulation tools	6/02
Prototype boards delivered	1/03
Production boards delivered	10/03
Daughter boards tested and ready for installation	4/04

3.8.4 Conclusions

Increasing the capacity of the FPGA available for the implementation of the track trigger is among the most straightforward of the options to implement in the hardware. Upgrading the current track trigger in this fashion is likely to be both cost effective and to be possible to execute in the available timescale. Furthermore, this upgrade is among the most flexible, allowing for the implementation of additional improvements late in the game as insights gleaned from the operation of the current version of the trigger and additional detailed studies of possible singlet configurations become available. This upgrade looks most promising and detailed studies of this option should be pursued.

3.9 L1 Tracking Trigger Summary and Conclusions

Based upon current simulation results, it seems likely that the L1 CTT may need to be upgraded in order to maintain the desired triggering capabilities as a result of the anticipated Run 2b luminosity increases. Because of the tight timescales and limited resources needed to address this particular challenge, significant alterations to the tracking detector installed in the solenoid bore are not considered feasible.

Other possibilities to effectively enhance the coincidence level employed in the L1 CTT have been explored. Using the axial CPS detector as a ninth layer in the trigger may provide some small background suppression at the expense of the L1 CTT electron capability as well as a reduction in the η acceptance of the L1 CTT. The CPS threshold needed to see single MIP particles will be difficult to achieve. This does not appear to be an attractive option.

The stereo track processor could potentially be incorporated into the L1 CTT to enhance background rejection, and simulation results indicate that a substantial gain in background rejection could be achieved by this technique. Unfortunately, the implementation of the stereo trigger would likely require significant resources in the development phase as well as increases in the infrastructure including the cable plant on the platform. Since other less expensive techniques to achieve similar rejection rates has been identified, the stereo track processor is not considered a viable option.

Improving the resolution of the L1 CTT by treating at least some fraction of the CFT axial layers as singlets rather than doublet layers in the L1 trigger should improve the background rejection of an upgraded L1 CTT by a significant

amount. Simulation studies that treat the fibers on the inner four CFT cylinders as singlet layers in the trigger indicate that about a factor of two improvement in the background rejection can be achieved (with only a small impact on the trigger efficiency). Studies that treat the hits from fibers on all axial layers as singlets in the trigger yield improvements in the fake rejection rate by more than a factor of five.

The performance of the Run 2b detector will almost certainly be enhanced if the FPGA are upgraded to allow for a significant increment in the number of equations that can be handled. This particular upgrade is very likely to facilitate a substantial improvement in the background rejection rate at a moderate cost. Even if singlet equations are not implemented in the FPGA, the FPGA upgrade provides a significant enhancement in flexibility of the track finding algorithms that may be implemented, and consequently should be given serious consideration.

4 Level 1 Calorimeter Trigger

4.1 Goals

The primary focus of Run 2b will be the search for the mechanism of electroweak symmetry breaking, including the search for the Higgs boson, supersymmetry, or other manifestations of new physics at a large mass scale. This program demands the selection of events with particularly large transverse momentum objects. The increase in luminosity (and thus increasing multiple interactions), and the decreased bunch spacing (132ns) for Run 2b will impose heavy loads on the Level 1 (L1) calorimeter trigger. The L1 calorimeter trigger upgrade should provide performance improvements over the Run 2a trigger system to allow increased rejection of backgrounds from QCD jet production, and new tools for recognition of interesting signatures. We envision a variety of improvements, each of which will contribute to a substantial improvement in our ability to control rates at the L1 trigger. In the following sections we describe how the L1 calorimeter trigger upgrade will provide

- An improved capability to correctly assign the calorimeter energy deposits to the correct bunch crossing via digital filtering
- A significantly sharper turn-on for jet triggers, thus reducing the rates
- Improved trigger turn-on for electromagnetic objects
- The ability to make shape and isolation cuts on electromagnetic triggers, and thus reducing rates
- The ability to match tracks to energy deposition in calorimeter trigger towers, leading to reduced rates
- The ability to include the energy in the intercryostat region (ICR) when calculating jet energies and the missing ET
- The ability to add topological triggers which will aid in triggering on specific Higgs final states.

The complete implementation of all these improvements will provide us with the ability to trigger effectively with the calorimeter in the challenging environment of Run 2b.

4.2 Description of Run 2a Calorimeter Electronics

4.2.1 Overview

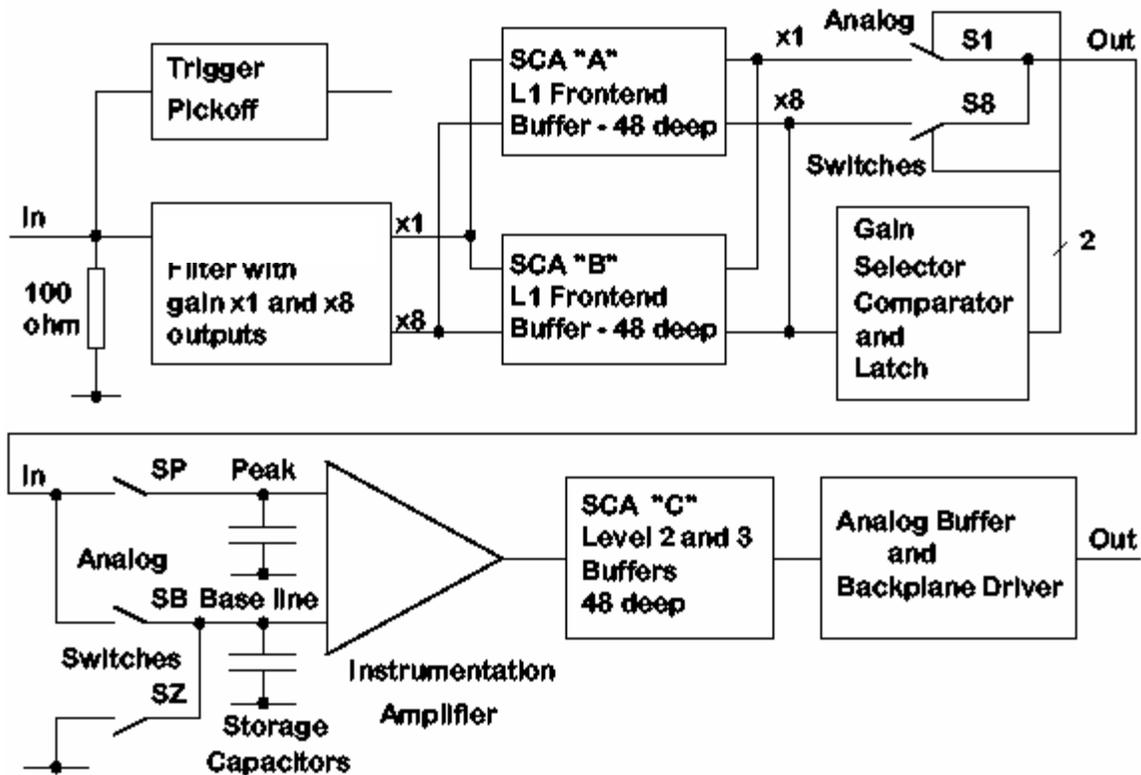


Figure 14. Functional diagram of the BLS system showing the precision readout path and the location of the calorimeter trigger pickoff signal.

The charge from the calorimeter is integrated in the charge sensitive preamplifiers located on the calorimeter. The preamplifier input impedance is matched to the $30\ \Omega$ coaxial cable from the detector (which have been equalized in length), and the preamplifiers have been compensated to match the varying detector capacitances, so as to provide signals that have approximately the same rise time (trace #1 in Figure 15). The fall time for the preamp signals is $15\ \mu\text{s}$. The signals are then transmitted (single ended) on terminated twisted-pair cable to the baseline subtractor cards (BLS) that shape the signal to an approximately unipolar pulse (see Figure 14 for a simple overview). The signal on the trigger path is further differentiated by the trigger pickoff to shorten the pulse width, leading to a risetime of approximately $120\ \text{ns}$ (trace #2 in Figure 15). The signals from the different depths in the electromagnetic and hadronic sections are added with appropriate weights to form the analog trigger tower sums. These analog sums are output to the L1 calorimeter trigger after passing through the trigger sum drivers. The signals are then transported differentially (on pairs of $80\ \Omega$ coaxial cable) $\sim 80\text{m}$ to the L1 calorimeter trigger (the negative side of a differential pair is shown in trace #4 in Figure 15). The key elements of the calorimeter trigger path are described in more detail in the following sections.

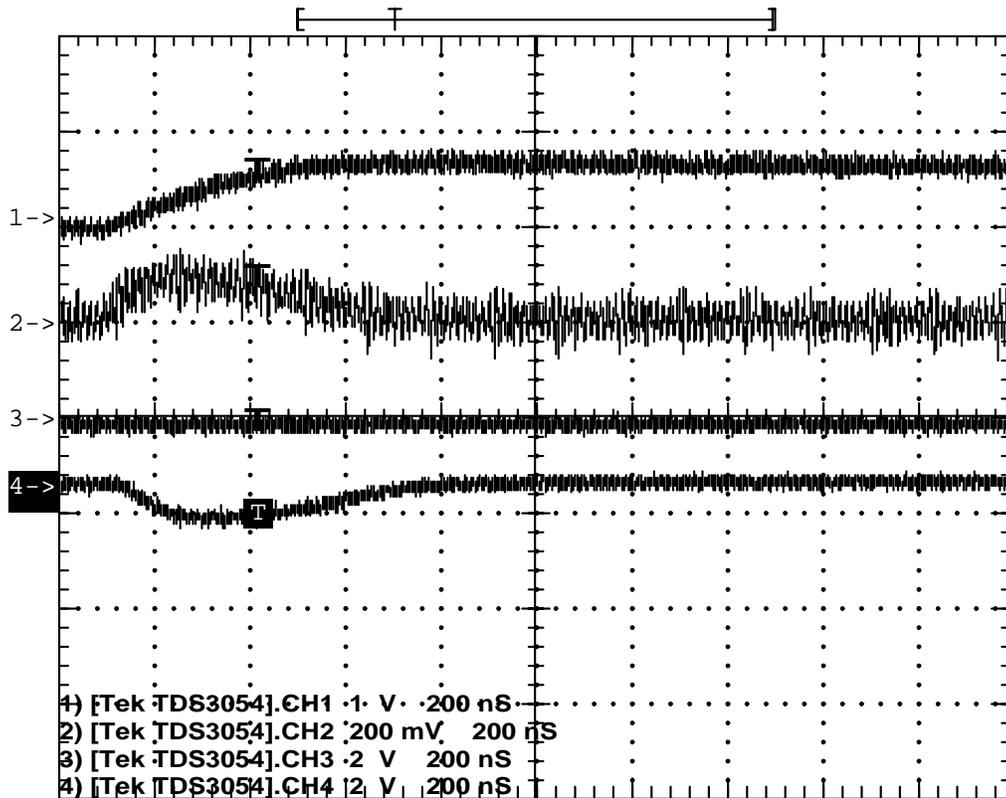


Figure 15. Scope traces for actual detector signals for an EM section. The horizontal scale is 200ns/large division. The top trace (#1, 1V/div) is of a preamp output signal as seen at the input to the BLS. The second trace (#2, 200mV/div) is of the trigger pickoff output on the BLS card (the large noise is due to scope noise pickup, so is not real). The fourth trace (#4, 2V/div) is the negative side of the differential trigger sum driver signal at the BLS that is sent to the L1 calorimeter trigger.

4.2.2 Trigger pickoff

The trigger pickoff captures the preamplifier signal before any shaping. A schematic of the shaping and trigger pickoff hybrid is shown in Figure 16 (the trigger pickoff section is in the upper left of the drawing). The preamplifier signal is differentiated and passed through an emitter follower to attempt to restore the original charge shape (a triangular pulse with a fast rise and a linear fall over 400 ns). This circuitry is located on a small hybrid that plugs into the BLS motherboard. There are 48 such hybrids on a motherboard, and a total of 55,296 for the complete detector.

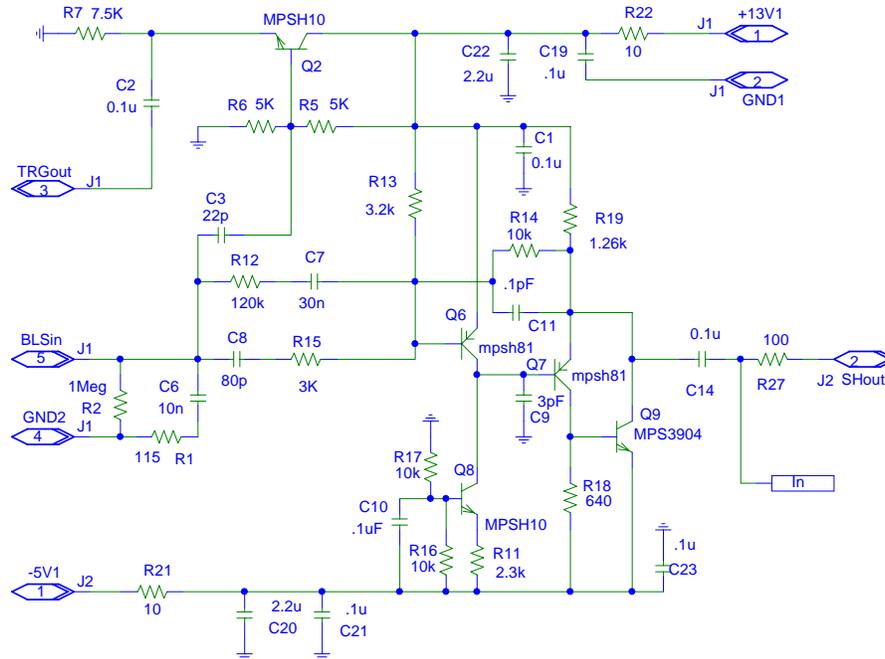


Figure 16. Schematic of the trigger shaper and trigger pickoff (upper left of picture). Pin 5 is the input, pin 3 is the trigger pickoff output, and pin 2 is the shaped precision signal output.

4.2.3 Trigger summers

The trigger pickoff signals for EM and HAD sections in individual towers (note these are not the larger trigger towers) are routed on the BLS board to another hybrid plug-in that forms the analog sums with the correct weighting factors for the different radial depth signals that form a single tower. The weighting is performed using appropriate input resistors to the summing junction of the discrete amplifier. A schematic for this small hybrid circuit is shown in Figure 17.

A single 48 channel BLS board has 8 trigger summer hybrids (4 EM towers and 4 HAD towers). There are a total of 9,216 hybrid trigger summers made up of 75 species. Since they are relatively easy to replace, changes to the weighting schemes can be considered. Recall, however, that access to the BLS cards themselves requires access to the detector as they are located in the area directly beneath the detector, which is inaccessible while beam is circulating.

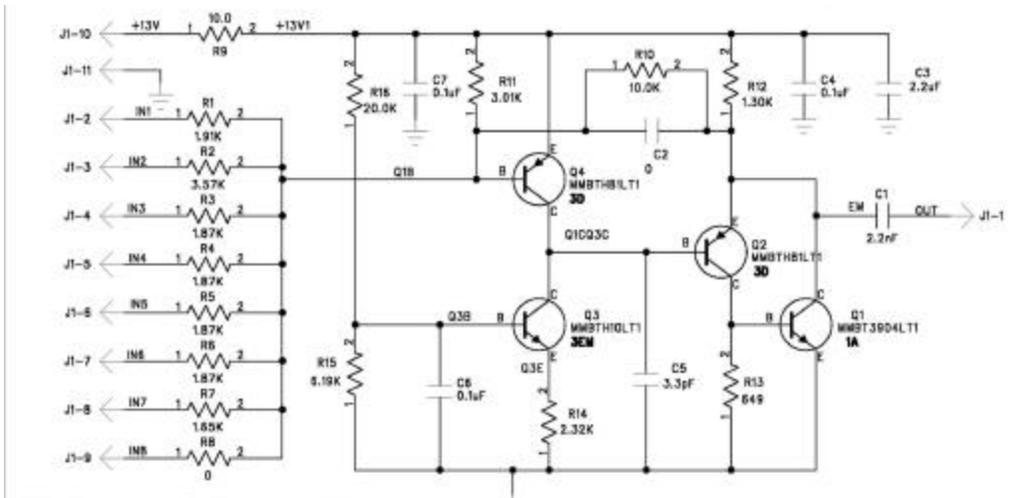


Figure 17. Schematic of the trigger summer hybrid. Up to 8 inputs from the various layers in a single tower can be summed with varying gains determined by the resistors to the summing junction (shown at left).

4.2.4 Trigger sum driver

The outputs of the 4 EM trigger summers on a single BLS board are summed (except at high η) once more by the trigger sum driver circuit (see the schematic in Figure 18) where a final overall gain can be introduced. This circuit is also a hybrid plug-in to the BLS board and is thus easily replaceable if necessary (with the same access restrictions discussed for the trigger summers). In addition the driver is capable of driving the coaxial lines to the L1 Calorimeter trigger. There are a total of 2,560 such drivers in 8 species (although most are of two types).

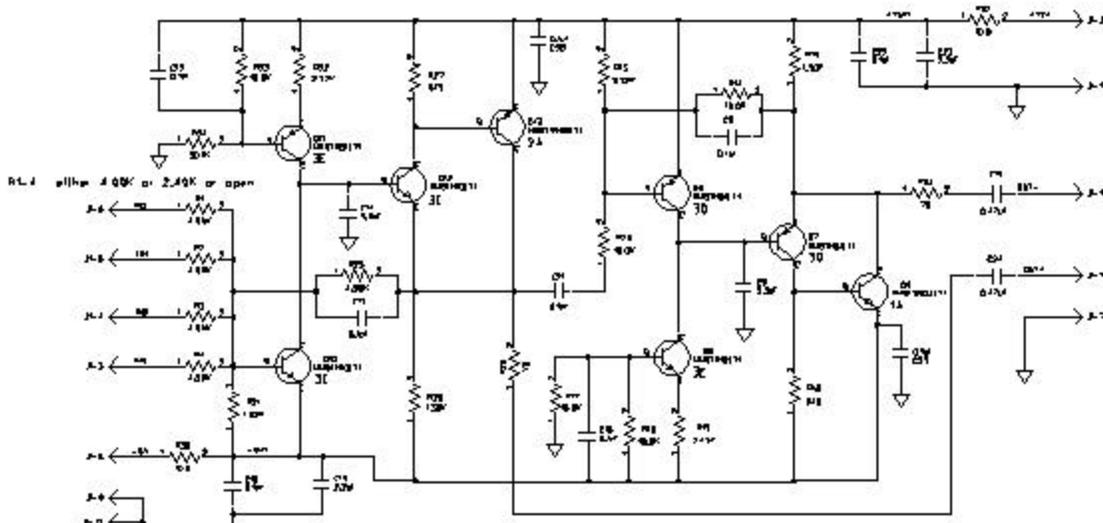


Figure 18. Schematic of the trigger sum driver hybrid. This circuit sums the outputs of up to 4 trigger summer outputs of the type shown in Figure 17.

If finer (x2) EM granularity in ϕ is required for the calorimeter trigger (see section 4.8 for a discussion of physics impact of finer segmentation), these

hybrids could be replaced to handle the finer segmentation, since there are two output pins on the hybrid that are connected to two coax cables. We expect about 4 man months of work to modify and replace these hybrids. If further simple shaping of the trigger signal is required it could be implemented on this circuit or at the receiver end on the L1 calorimeter trigger.

4.2.5 Signal transmission, cable dispersion

The signals from the trigger driver circuits are transmitted differentially on two separate miniature coax (0.1") cables. The signal characteristics for these cables are significantly better than standard RG174 cable. However first indications are that the signal seen at the end of these cables at the input to the L1 calorimeter trigger are somewhat slower than expected (an oscilloscope trace of such a signal is shown in Figure 19 for EM and Figure 20 for HAD). The cause of the deviation from expectations is not presently known and is under investigation. It is possible that the signal dispersion in these coaxial cables is worse than expected and possible replacements are under investigation. In any case, we must deal with these pulses that are over 400ns wide (FWHM) and thus span a few 132ns bunch crossings. While there are possible intermediate solutions to deal with this signal shape for 132ns bunch crossings, the most effective treatment calls for further processing of the signal through digital filtering to extract the proper bunch crossing. This option is described in more detail in later sections.

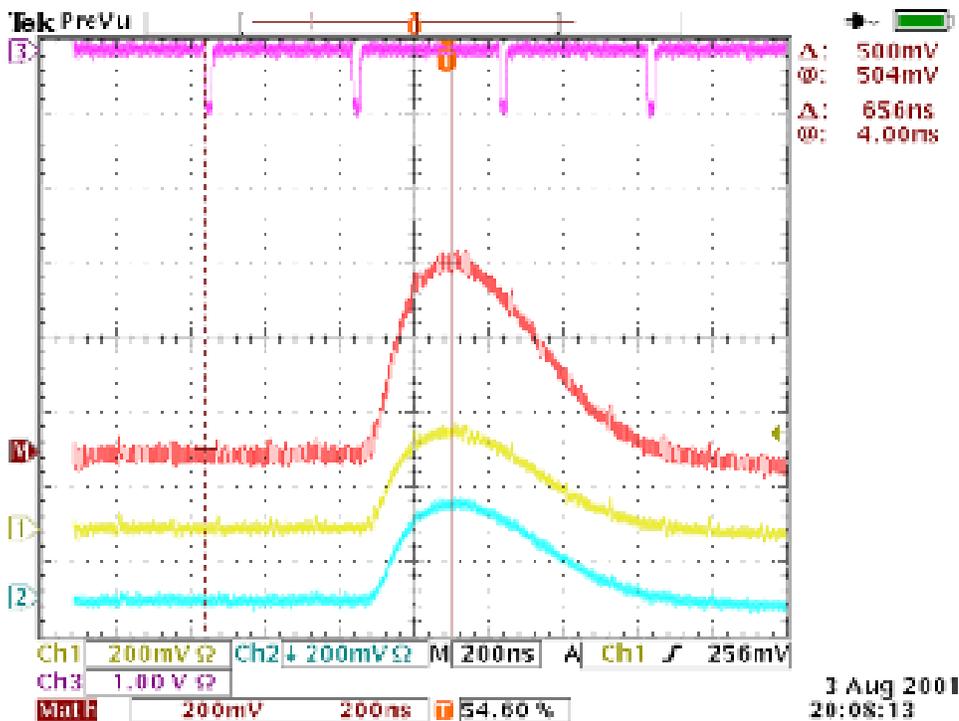


Figure 19. Actual traces of EM trigger tower ($\eta=+1$, $\phi=17$) data from the trigger sum driver signal as measured at the input to the L1 calorimeter trigger. The top trace (#3) shows the time of the beam crossings (396ns). The second trace (M) shows the addition of the two differential

signals after inversion of the negative one. The third trace (#1) is the positive side of the differential pair. The fourth trace (#2) is the inverted trace for the negative side of the differential pair.

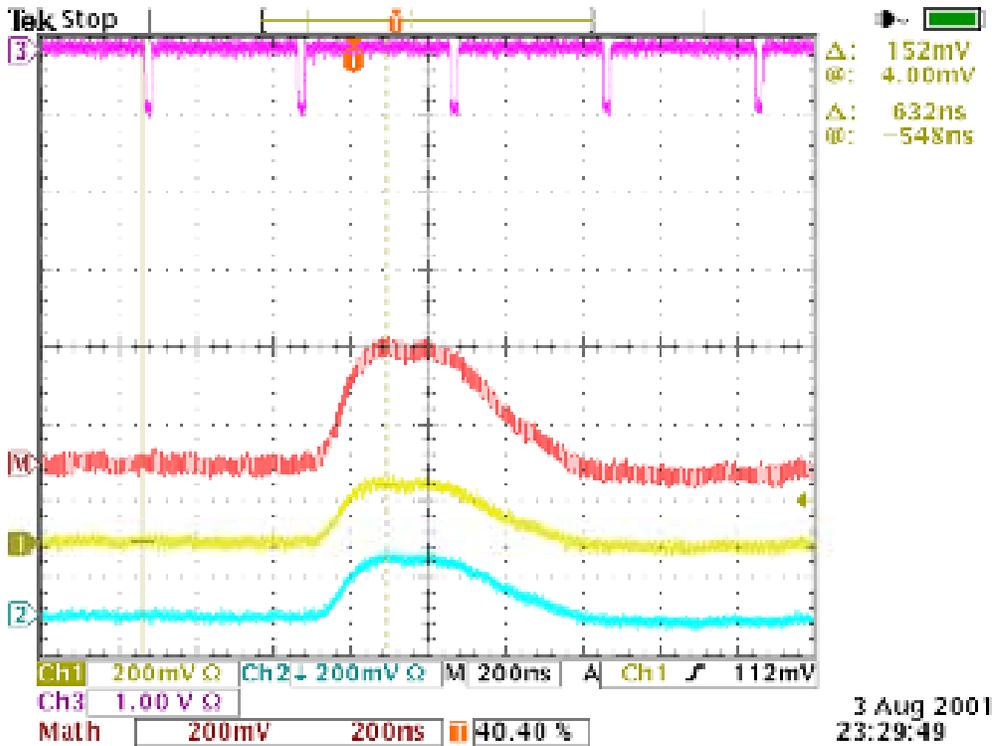


Figure 20. Actual traces of HAD trigger tower ($\eta=+1$, $\phi=17$) data from the trigger sum driver signal as measured at the input to the L1 calorimeter trigger. The top trace (#3) shows the time of the beam crossings (396ns). The second trace (M) shows the addition of the two differential signals after inversion of the negative one. The third trace (#1) is the positive side of the differential pair. The fourth trace (#2) is the inverted trace for the negative side of the differential pair.

4.3 Description of Current L1 Calorimeter Trigger

4.3.1 Overview

The $D\phi$ uranium-liquid argon calorimeter is constructed of projective towers covering the full 2π in the azimuthal angle, ϕ , and approximately 8 units of pseudo-rapidity, η . There are four subdivisions along the shower development axis in the electromagnetic (EM) section, and four or five in the hadronic (H) section. The hadronic calorimeter is divided into the fine hadronic (FH) section with relatively thin uranium absorber, and the backing coarse (CH) section. In the intercryostat region $0.8 < |\eta| < 1.6$ where the relatively thick cryostat walls give extra material for shower development, a scintillator based intercryostat detector (ICD) and extra ‘massless gap’ (MG) liquid argon gaps without associated absorber are located.

The calorimeter tower segmentation in $\eta\phi$ is 0.1×0.1 , which results in towers whose transverse size is larger than the expected sizes of EM showers but, considerably smaller than typical sizes of jets.

As a compromise, for triggering purposes, we add four adjacent calorimeter towers to form trigger towers (TT) with a segmentation of 0.2×0.2 in $\eta\phi$. This yields an array that is 40 in η and 32 in ϕ or a total of 1,280 EM and 1,280 H tower energies as inputs to the L1 calorimeter trigger.

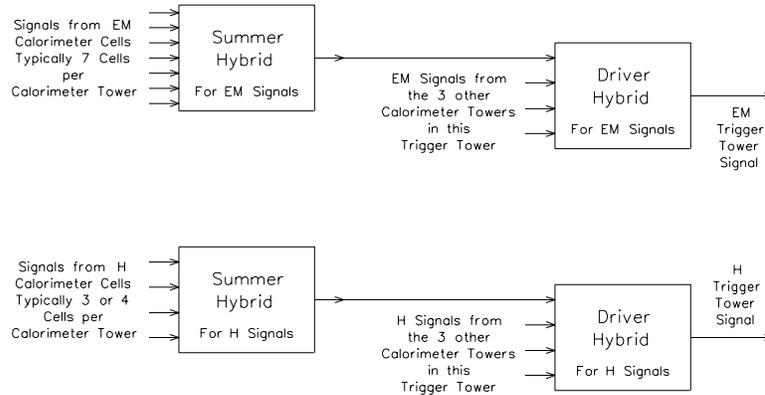


Figure 21. Trigger tower formation.

The analog summation of the signals from the various calorimeter cells in a trigger tower into the EM and H TT signals takes place as described on page 52. This arrangement for summing the calorimeter cells into trigger towers is shown schematically in Figure 21.

Long ribbons of coaxial cable route the 1280 EM and H analog trigger tower signals from the detector platform through the shield wall and then into the first floor of the moving counting house (MCH) where the Level 1 calorimeter trigger is located. The first step in the Level 1 calorimeter trigger is to scale these signals to represent the E_T of the energy deposited in each trigger tower and then to digitize these signals at the beam-crossing rate (132ns) with fast analog to digital converters. The digital output of these 2560 converters is used by the subsequent trigger logic to form the Level 1 calorimeter trigger decision for each beam crossing. The converter outputs are also buffered and made available for readout to both the Level 2 Trigger system and the Level 3 Trigger DAQ system.

The digital logic used in the Level 1 Calorimeter Trigger is arranged in a "pipe-lined" design. Each step in the pipe-line is completed at the beam crossing rate and the length of the pipe-line is less than the maximum $D\phi$ Level 1 trigger latency for Run 2a which is $3.3 \mu\text{sec}$ (driven by the calorimeter shaping times, cables lengths, drift times etc). This digital logic is used to calculate a number of quantities that are useful in triggering on specific physics processes. Among these are quantities such as the total transverse energy and the missing transverse energy, which we will designate as "global" and information relating to

"local" or cluster aspects of the energy deposits in the calorimeter. The latter would include the number of EM and H-like clusters exceeding a set of programmable thresholds.

4.3.2 Global Triggers

Interesting global quantities include:

the total transverse energies:

$$\left(E_T^{EM}\right)_{Total} = \sum_{i=1}^{1280} \left(E_T^{EM}\right)_i$$

$$\left(E_T^H\right)_{Total} = \sum_{i=1}^{1280} \left(E_T^H\right)_i$$

and

$$\left(E_T\right)_{Total} = \left(E_T^{EM}\right)_{Total} + \left(E_T^H\right)_{Total}$$

the missing transverse energy:

$$Mp_T = \sqrt{E_x^2 + E_y^2}$$

where:

$$E_x = \sum_{i=1}^{1280} \left[\left(E_T^{EM}\right)_i + \left(E_T^H\right)_i \right] \cos(\phi_i)$$

and

$$E_y = \sum_{i=1}^{1280} \left[\left(E_T^{EM}\right)_i + \left(E_T^H\right)_i \right] \sin(\phi_i)$$

Any of these global quantities can be used in constructing triggers. Each quantity is compared to a number of thresholds and the result of these comparisons is passed to the Trigger Framework where up to 128 different Level 1 triggers can be formed.

4.3.3 Cluster Triggers

The DØ detector was designed with the intent of optimizing the detection of leptons, quarks and gluons. Electrons and photons will manifest themselves as localized EM energy deposits and the quarks and gluons as hadron-like clusters.

Energy deposited in a Trigger tower is called EM-like if it exceeds one of the EM E_T thresholds and if it is not vetoed by the H energy behind it. Up to four EM E_T thresholds and their associated H veto thresholds may be programmed for each of the 1280 trigger towers. Hadronic energy deposits are detected by calculating the EM $E_T + H E_T$ of each Trigger tower and comparing each of these 1280 sums to four programmable thresholds.

The number of Trigger towers exceeding each of the four EM thresholds (and not vetoed by the H energy behind it) is calculated and these four counts are compared to a number of count thresholds. The same is done for the four EM $E_T + H E_T$ thresholds. The results of these count comparisons on the number of Trigger towers over each threshold are sent to the Trigger Framework where they are used to construct the Level 1 Triggers.

4.3.4 Hardware Implementation

4.3.4.1 Front End Cards

The analog signals from the calorimeter, representing energies, arrive at the Calorimeter Trigger over coaxial differential signal cables and are connected to the analog front end section of a Calorimeter Trigger Front End Card (CTFE). A schematic diagram of one of the four cells of this card is shown in Figure 22.

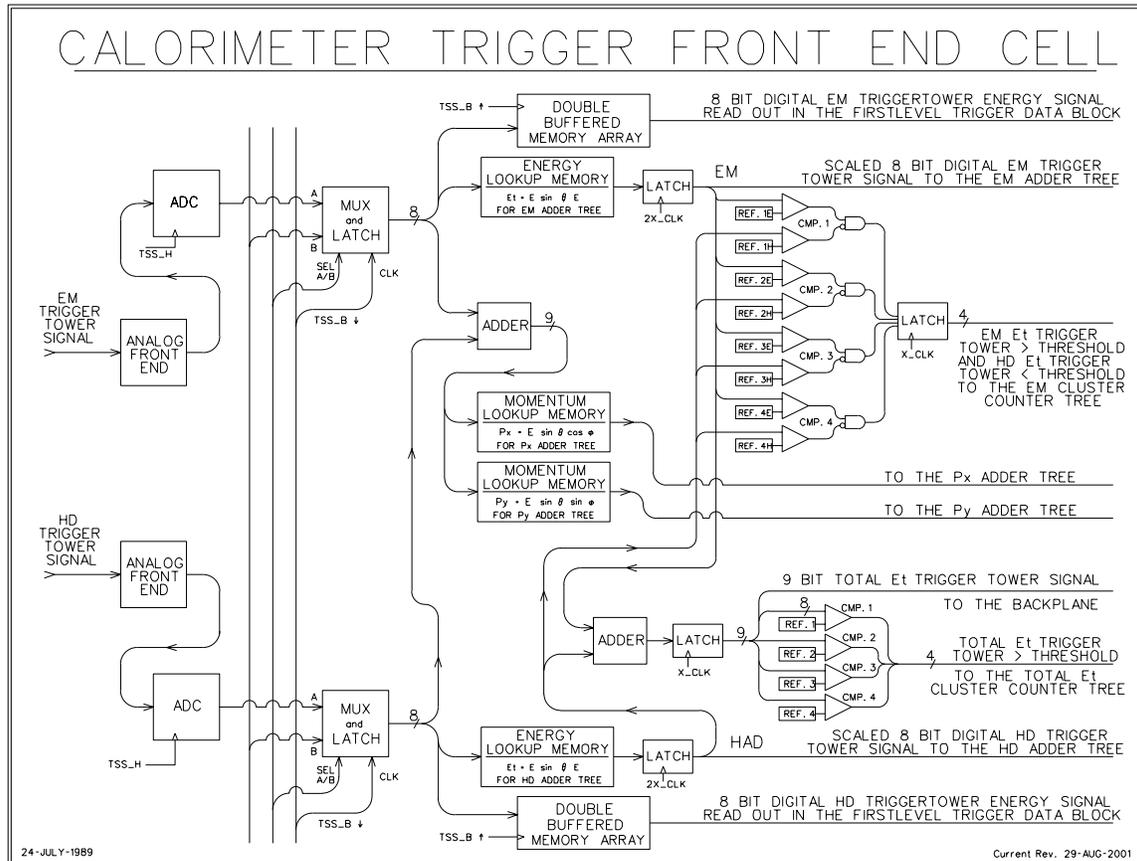


Figure 22. Calorimeter trigger front end cell (CTFE).

The front-end section contains a differential line receiver and scales the energy signal to its transverse component using a programmable gain stage. The front end also contains digital to analog circuitry for adding a positive bias to the tower energies in accord with downloaded values.

Immediately after the analog front end, the EM or H signal is turned into an 8 bit number by fast (20 ns from input to output) FADC's. With our current choice of 0.25 GeV least count this gives a maximum of 64 GeV for the single tower transverse energy contribution.

The data are synchronized at this point by being clocked into latches and then follow three distinct parallel paths. One of these paths leads to a pipeline register for digital storage to await the L1 trigger decision and subsequent readout to the Level 2 Trigger system and the Level 3 Trigger DAQ system.

On the other two paths, each 8-bit signal becomes the address to a look up memory. The content of the memory at a specified address in one case is the transverse energy with all necessary corrections such as lower energy requirements etc. In the other case, the EM + H transverse energies are first added and then subjected to two look-ups to return the two Cartesian components of the transverse energy for use in constructing MP_T . The inherent flexibility of this scheme has a number of advantages: any energy dependent quantity can be generated, individual channels can be corrected or turned off at this level and arbitrary individual tower efficiencies can be accommodated.

The CTFE card performs the function of adding the E_T 's of the four individual cells for both the EM and H sections and passing the resulting sums onto the Adder Trees. In addition it tests each of the EM and EM+H tower transverse energies against the four discrete thresholds and increments the appropriate counts. These counts are passed onto the EM cluster counter trees and the total E_T counter trees, respectively.

4.3.4.2 Adder and Counter Trees

The adder and counter trees are similar in that they both quickly add a large number of items to form one sum. At the end of each tree the sum is compared to a number of thresholds and the result this comparison is passed to the Trigger Framework. A typical adder tree is shown in Figure 23.

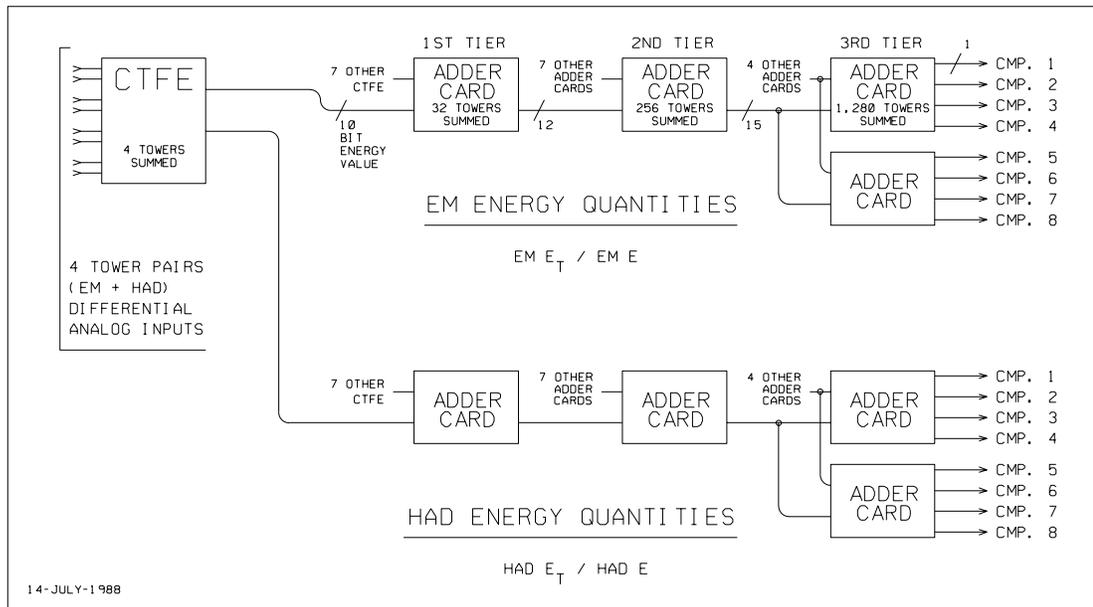


Figure 23. Adder tree for EM and Had quantities.

4.3.5 Physical Layout

Ten racks are used to hold the Level 1 Calorimeter Trigger, which is located in the first floor moving counting house. The lower section of each rack contains the CTFE cards for 128 Trigger towers (all 32 ϕ 's for four consecutive η 's). The upper section of each rack contains a component of one of the Adder or Counter Trees.

4.4 Performance of the Current Calorimeter Trigger

In order to compare the performance of the present L1 calorimeter trigger, the following simulation is used. The jet performance is studied using a Monte-Carlo sample of QCD events (PYTHIA, with parton p_T cuts of 5, 10, 20, 40 GeV and 0.5 overlaid minimum bias events). A cone algorithm with a radius of 0.4 in $\eta\phi$ is applied to the generated stable hadrons in order to find the generated jets and their direction. The direction of each generated jet is extrapolated to the calorimeter surface; leading to the "center TT" hit by the jet (TT stands for Trigger Tower). The highest E_T TT in a 3x3 trigger tower region (which is 0.6x0.6 in $\eta\phi$ space) around this center is then used to define the "trigger E_T " corresponding to the jet. Other comparisons of the current calorimeter trigger for electrons is discussed in section 4.10

4.4.1 Energy measurement and turn-on curves

In the present L1 calorimeter trigger, the trigger towers are constructed using fixed $\eta\phi$ towers. Thus we expect that a trigger tower only captures a small fraction of the total jet energy since the size of the 0.2 x 0.2 trigger towers is small compared to the spatial extent of hadronic showers. This is illustrated in

Figure 24, which shows, for simulated 40 GeV E_T jet events, the ratio of the E_T observed by the trigger to the generated E_T . It can be seen in Figure 24 that this transverse energy is only 25% of the jet E_T on average. Therefore we must use low jet trigger thresholds if we are to be efficient even for relatively high energy jets. Moreover the trigger E_T has poor resolution, as can be seen in Figure 24. As a result, the trigger efficiency (the efficiency for having at least one TT with E_T above a given threshold) rises only slowly with increasing jet E_T , as shown in the turn-on curves in Figure 25. A similar effect occurs for the EM triggers as well; even though a typical EM shower can be reasonably well contained within a TT, often the impact point of an electron or photon is near a boundary between TTs.

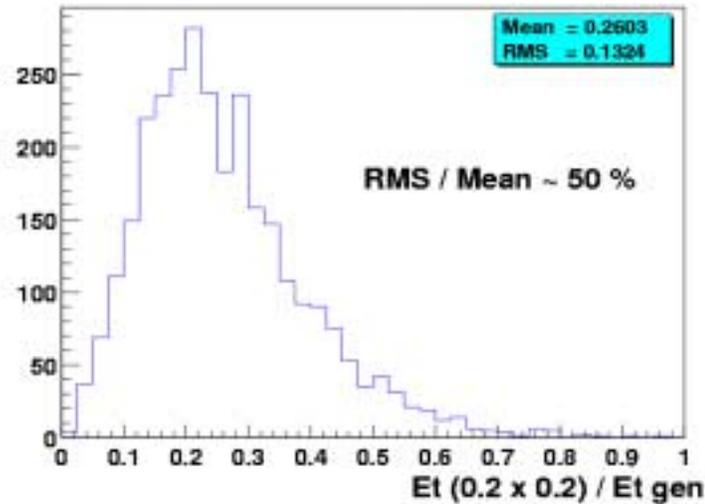


Figure 24. Ratio of the trigger E_T to the transverse energy of the generated jet. Only jets with $E_T \approx 40$ GeV are used in this figure.

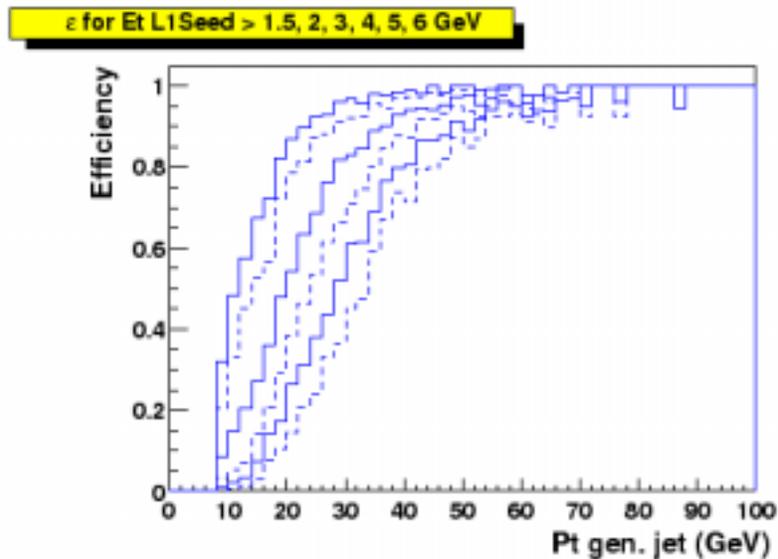


Figure 25. Trigger efficiency as a function of the transverse energy of the generated jet. The curves correspond to thresholds of 1.5, 2, 3, 4, 5 and 6 GeV (respectively from left to right).

4.4.2 Trigger rates

The trigger E_T resolution, convoluted with the steeply falling p_T spectrum of QCD events, leads to, on average, the “promotion” of events to larger E_T 's than the actual E_T . The number of QCD events which pass the L1 trigger is thus larger than what it would be with an ideal trigger E_T measurement. Due to the very large cross-section for QCD processes, this results in large trigger rates⁵. For example, as shown in Figure 26, an inclusive unprescaled high E_T jet trigger, requiring at least one TT above a threshold defined such that the efficiency for 40 GeV jets is 90%, would yield a rate for passing the L1 calorimeter trigger of at least 10 kHz at $2 \times 10^{32} \text{ cm}^2 \text{ s}^{-1}$. Maintaining this rate below 1 kHz would imply an efficiency on such high E_T jets of only 60%. Trigger rates increase faster than the luminosity due to the increasing mean number of interactions per bunch crossing. Trigger rates are shown in Figure 27 as a function of the mean number of minimum bias events which pile up on the high p_T interaction. These are shown for two multi-jet triggers: the first requiring at least two TT above 5 GeV (indicated as CJT(2,5)); the second requiring at least two TT above 5 GeV and at least one TT above 7 GeV (indicated as CJT(1,7)*CJT(2,5)). These triggers correspond to reasonable requirements for high p_T jets because, as can be seen in Figure 26, a threshold of 5 GeV leads, for 40 GeV jets, to an 80 % efficiency. The rates in Figure 27 are shown for a luminosity of $2 \times 10^{32} \text{ cm}^2 \text{ s}^{-1}$. For the higher luminosity of $5 \times 10^{32} \text{ cm}^2 \text{ s}^{-1}$ expected in Run 2b, the L1 bandwidth of 5kHz could be saturated by such dijet conditions alone, unless large prescale factors are applied.

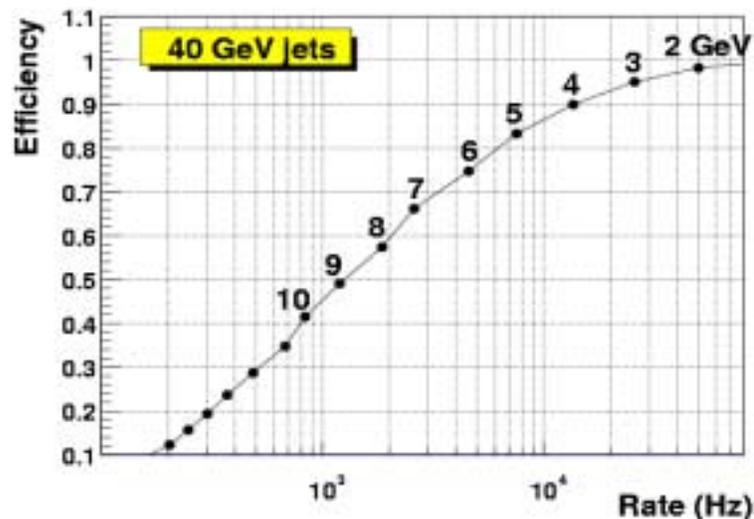


Figure 26. The efficiency to trigger on 40 GeV jets as a function of the inclusive trigger rate when one TT above a given threshold is required. Each dot corresponds to a different threshold (in steps of 1 GeV), as indicated. The luminosity is $2 \times 10^{32} \text{ cm}^2 \text{ s}^{-1}$.

⁵ These rates are estimated here from samples of PYTHIA QCD events with parton $p_T > 2 \text{ GeV}$, passed through a simulation of the trigger response.

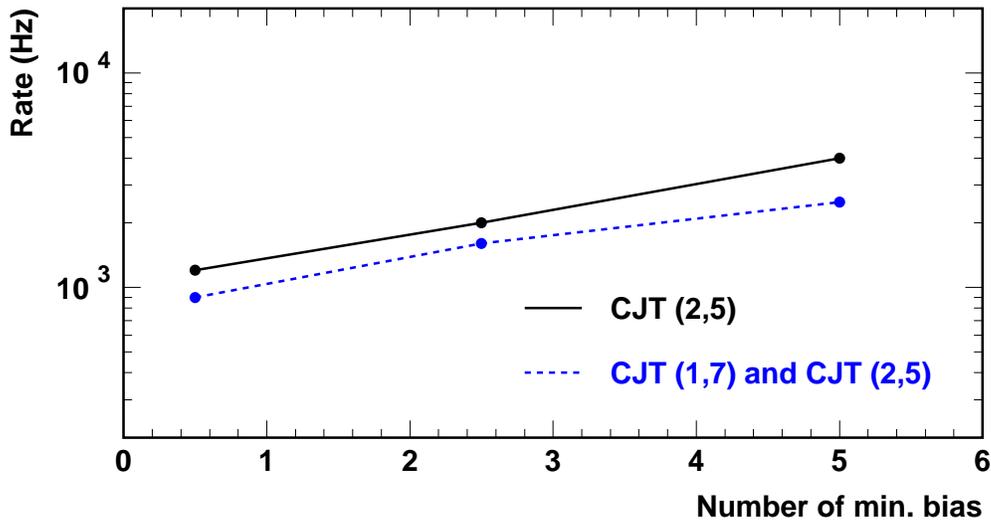


Figure 27. The inclusive trigger rate as a function of the mean number of minimum bias events overlaid on the high p_T interaction. The rates are shown for two di-jet trigger conditions corresponding to two TTs above 5 GeV (CJT(2,5)) and two TTs with above 5GeV and at least one above 7 GeV (CJT(1,7)*CJT(2,5)). The luminosity is $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$.

A more exhaustive study of the evolution of the L1 trigger rate with increasing luminosity has been carried out⁶. In that document a possible trigger menu was considered, in which ~75 % of the L1 bandwidth is used by multijet triggers. The results are shown in Table 13. It can be seen that, at the luminosity foreseen for Run 2b (corresponding to the second row), the trigger rates should be reduced by at least a factor of two in order to maintain a reasonably small dead time. We note that the need to preserve jet triggers is required by some of the Higgs boson physics (see for example section 4.7.4).

Table 13. The overall level 1 trigger rates as a function of luminosity.

Luminosity	High Pt L1 rate (Hz)	Total L1 rate (Hz)
$1 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$	1,700	5,000
$2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$	4,300	9,500
$5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$	6,500	20,000

4.4.3 Conclusions/implications for high luminosity

From these studies, it is clear that there is a need to significantly improve the rejection of the L1 calorimeter trigger (while maintaining good efficiency) if we are to access the physics of Run 2b. One obvious way to help achieve this is to migrate the tools used at L2 (from Run 2a) into L1. In particular, the ability to

⁶ B. Bhattacharjee, "Transverse energy and cone size dependence of the inclusive jet cross section at center of mass energy of 1.8 TeV", PhD Thesis, Delhi University.

trigger on “objects” such as electromagnetic showers and jets would help significantly. The “clustering” of TT’s at L1, could reduce the trigger rates by a factor 2 to 4 as will be shown later. The principal reason for this gain comes from the improvement in the quality of the energy cut, when applied to a cluster of trigger towers. Transferring to level 1 some of the functions that currently belong to level 2 would also permit the introduction of new selection algorithms at the L1 trigger level. So while it is clear that there are additional gains to be made through EM trigger tower shape cuts and missing E_T filtering, they will require further study to quantify the specific gains. These studies remain to be done.

From a conceptual viewpoint, an important consequence of selecting physics “objects” at level 1 is that it allows a more “inclusive” and hence less biased selection of signatures for the more complicated decays to be studied in Run 2b. Thus we expect that the trigger menus will become simpler and, above all, less sensitive to biases arising from the combinations of primary objects.

4.5 Overview of Options for Improvement

4.5.1 Global view of options considered

To accomplish the goals listed above, the L1 calorimeter trigger will need to be completely replaced – it is not possible to modify the existing trigger to incorporate the new features. We have studied various ways to improve the L1 rejection rates. Although a final design implementation is not complete, we discuss these in turn below. They include:

- the necessary hardware improvements in filtering to allow proper triggering on the correct bunch crossing;
- studies of the gains from a “sliding window” algorithm for jets and electrons;
- the ability to better correlate tracks from the fiber tracker to calorimeter trigger towers;
- the addition of presently unused calorimeter energy information from the intercryostat region (ICR) region and massless gaps (MG) in the L1 trigger;
- optimizing trigger tower thresholds;
- some topological cuts.

Following the discussion of each of these improvements, we outline an implementation that can provide the upgraded calorimeter trigger. The costs are shown at the end of this chapter.

4.6 Digital Filtering

Digital filtering offers a way to reduce the effect of unwanted triggers due to collisions in close proximity to the desired trigger.

4.6.1 Concept & physics implications

The pulse shape, and particularly the rise time, of the trigger pickoff signal is not optimized for 132ns beam bunch crossing operation (see Figure 19 and Figure 20). Since the trigger pickoff pulse width significantly exceeds the 132ns bunch spacing time of Run 2b, the ability to correctly identify the correct trigger bunch crossing is compromised. There may be intermediate solutions to address this problem at the lower luminosities, but a long-term solution must be developed. This could be done by means of an analog filter with shorter shaping, but this is only achieved with a further loss in signal. A digital filter is a better solution because it is much more flexible for a similar cost.

The trigger pickoff signal is at the end of the calorimeter electronic chain described above. The ideal energy deposition shape is a “saw-tooth” pulse (infinitely fast rise and a linear ~ 400 ns fall) from energy deposited in the cells of the calorimeter at each beam crossing. This is modified by the transfer function of the electronics. The inverse transfer function will transform the pickoff signal back to original energy deposition pulse shape. Digital filtering would be implemented at this stage. The inverse function can be implemented by a FIR (Finite Impulse Response) digital filter. In the presence of noise, the digital filter offers an additional advantage: one can use the theory of *optimal filtering* to minimize the noise contribution.

In order to define the exact form of a digital filter best suited to the task, a measurement of noise in the trigger pickoff signals is needed. As such measurements become available, a refined design will be undertaken.

4.6.2 Pileup rejection

Two different “pile-up” effects arise with increasing luminosity, the first is due to extra collisions in the crossing of interest (and thus unavoidable), and the second is due to collisions in neighboring crossings that contribute to the crossing of interest because of signal shapes.

In the first case, we find that as the luminosity increases, then for each triggered beam crossing there are several minimum bias events that appear in that same beam crossing. The number of such additional events is Poisson distributed with a mean proportional to the luminosity. The energy added by these events has a distribution close to that of a double exponential (Laplacian). It is possible to minimize the contribution of this noise by using an appropriate digital filter (Matched Median Filter).

In the second case, because the width of the trigger pickoff signal extends over several beam crossing (6 at 132ns on the positive side of the signal), then when two such pulses are close in time, there is some overlap and thus the shape of the pickoff signal becomes more complicated than that of a single isolated pulse. The inverse filter will extract from this signal the two original pulses. Consequently, the problems caused by overlapping pulses are minimized if one uses digital filtering.

4.6.3 Simulation

Simulations of the FIR response will be performed once the noise measurements are obtained. These simulations will result in a set of coefficients for the filter algorithm. The most reasonable way to compute coefficients is to use the mean squared (LMS) optimization. This proceeds by minimizing the sum of the square of the differences between many input excitations and their filtered outputs; each input excitation produces a pulse at the input of the ADC and contributes several terms to the sum: one for each beam crossing where the pulse is non-zero. A realistic simulation of the noise must be added to the theoretical pulse (derived from the transfer function of the calorimeter).

4.6.4 Implementation

An effective range of 8 bits for the transverse energy of each trigger tower seems sufficient to meet the desired performance and is technically practical. The calorimeter pulses are proportional to the energy deposited in the calorimeter while the trigger algorithms use transverse energy (rather than energy) in their calculations. Thus the L1 calorimeter trigger must convert the calorimeter energy measurements to transverse energy. It is possible to carry out this conversion with a programmable analog circuit placed in front of each ADC but a digital solution is more practical and flexible. In order to preserve a dynamic range of 8 effective bits for signals in transverse energy, one should use a 10 bit ADC to digitize the analog energy signals.

The conversion rate needs to be at least equal to the beam-crossing rate, but it can be higher than that. On the other hand, if the over-sampling rate is too high, then it does not provide any more improvement because of the relatively slow input signals from the trigger sum drivers.

Such 10 bit ADCs have a “pipelined” architecture, with a latency of 4 to 6 cycles. Since the level 1 trigger operates on a very tight latency budget, one is driven to conversion rates that are larger than the beam-crossing rate because otherwise the data conversion would have too large a latency. ADCs in the 20-60 MHz range are now common and inexpensive. If only a fraction of the samples produced by each ADC are required for filtering, then the additional samples can be ignored. One should note that because the signal may be over-sampled, then it would seem natural to use those data to improve the overall performance of the digital filtering operation. Recalling Shannon’s sampling theorem, it can be shown that a FIR filter implementation of the exact inverse transfer function considered must have at least a sampling frequency that is twice that of the beam crossing. However in this particular application where the trigger sum pickoff signal is relatively slow, the over-sampling may not provide much benefit. Further study is needed.

4.6.5 Conclusions

Given the relatively slow trigger sum driver pulse shapes observed in Figure 19 and Figure 20, we believe that a digital filter is required to suppress the contributions from signals in nearby bunch crossings to that containing a high p_T

trigger. The exact implementation details and the final performance specifications require further study.

4.7 Sliding Trigger tower Windows for Jets

A “sliding window” algorithm⁷ has the potential to significantly sharpen the trigger turn on curves.

4.7.1 Concept & physics implications

Various algorithms can be used to cluster the trigger towers and look for “regions of interest” (R), i.e. for regions of fixed size, S , in $\eta \times \phi$ in which the deposited E_T has a local maximum. To find those regions of interest, a window of size S is shifted in both directions by steps of 0.2 in η and ϕ . By convention each window is unambiguously (although arbitrarily in the 2 x 2 case) anchored on one trigger tower T and is labeled $S(T)$. Examples are shown in Figure 28.



Figure 28. Examples of (a) a 3x3 and (b) 2x2 sliding window $S(T)$ associated to a trigger tower T . Each square represents a 0.2 x 0.2 trigger tower. The trigger tower T is shown as the shaded region.

The sliding tower algorithm aims to find the optimum region of the calorimeter for inclusion of energy from jets (or EM objects) by moving a window grid across the calorimeter η , ϕ space so as to maximize the transverse energy seen within the window. The window of towers so found, together perhaps with a specified set of neighbors, is called the region of interest, R , and is referenced by a specific TT within R as indicated in Figure 28 for a 3x3 or a 2x2 window. The total E_T within R and in the defined neighbor region is termed the trigger E_T relevant to the jet or EM object. A specific example of how the local maximum could be defined is shown in Figure 29.

⁷ This type of algorithm has been developed for Atlas as described in the Trigger Performance Status Report, CERN/LHCC 98-15.

≥	>	>	>	>
≥	≥	>	>	>
≥	≥	S(T)	>	>
≥	≥	≥	>	>
≥	≥	≥	≥	>

Figure 29. An illustration of a possible definition of a local E_T maximum for a R candidate. The 0.2×0.2 cluster is accepted if it is more energetic than the neighboring clusters marked as “>” and at least as energetic as those marked “≥”. This method resolves the ambiguities when two equal clusters are seen in the data.

4.7.2 Simulation

Several algorithms defining the regions of interest have been considered and their performance has been compared using samples of simulated events:

- The R size is 0.6×0.6 (Figure 28a) and the trigger E_T is the E_T contained in the RoI.
- The R size is 0.4×0.4 (Figure 28b) and the trigger E_T is the E_T contained in the 0.8×0.8 region around the RoI.
- The R size is 1.0×1.0 and the trigger E_T is the E_T contained in the R .

In each case, the algorithm illustrated in Figure 29 is used to find the local maxima R . For each algorithm, the transverse energy seen by the trigger for 40 GeV jets is shown in Figure 30. This is to be compared with Figure 24, which shows the E_T seen by the current trigger. Clearly, any of the “sliding window” algorithms considerably improves the resolution of the trigger E_T . For the case of the 40 GeV jets studied here, the resolution improves from an rms of about 50% of the mean (for a fixed 0.2×0.2 $\eta \times \phi$ trigger tower) to an rms of 30% of the mean (for a sliding window algorithm), and the average energy measured in the trigger tower increases from ~26% to 56-63% (depending on the specific algorithm).

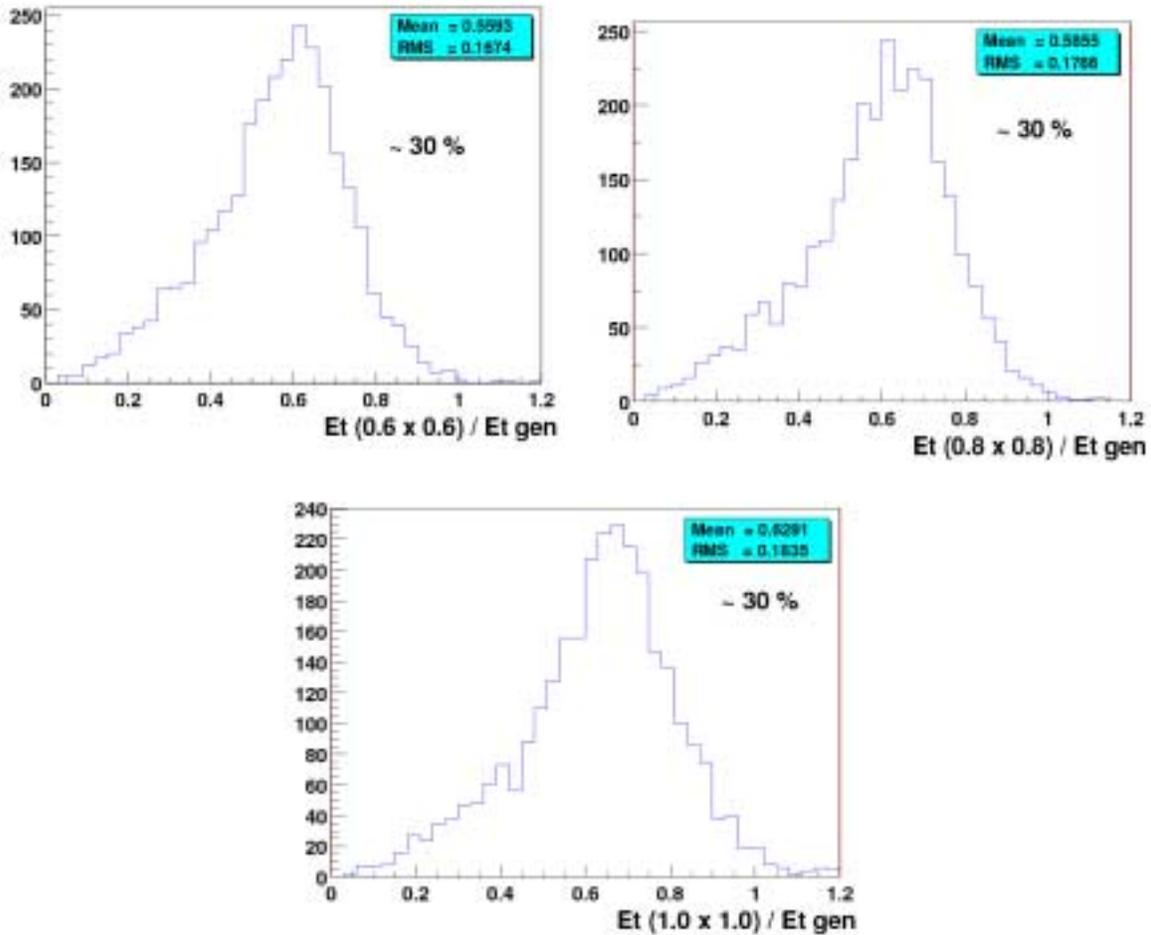


Figure 30. Ratio of the trigger E_T to the transverse energy of the generated jet, using three different algorithms to define the regions of interest. Only jets with $E_T \approx 40$ GeV are used here. The ratio of the rms to the mean of the distribution, the value 30%, is written on each plot.

Since the observed resolution is similar for all three algorithms considered, then the choice of the R definition (*i.e.* of the algorithm) will be driven by other considerations including hardware implementation or additional performance studies. In the following, we will only consider the (b) algorithm.

4.7.3 Efficiency

The simulated trigger efficiency for the (b) algorithm, with a threshold set at 10 GeV, is shown as a function of the generated E_T in Figure 31. The turn-on of the efficiency curve as a function of E_T is significantly faster than that of the current trigger, also shown in Figure 31 for two values of the threshold. With a 10 GeV threshold, an efficiency of 80% is obtained for jets with E_T larger than 25 GeV.

In order to understand which part of these new algorithms are providing the improvement (the sliding window or the increased trigger tower size), we have studied the gain in efficiency which is specifically due to the sliding window

procedure by considering an algorithm where the TTs are clustered in fixed 4×4 towers (i.e. 0.8×0.8 in $\eta \times \phi$), without any overlap in η or ϕ . The comparison of the “fixed” and “sliding” algorithms is shown in Figure 32. One observes a marked improvement for the “sliding” windows compared to the “fixed” towers, indicating that the added complexity of implementing sliding windows is warranted.

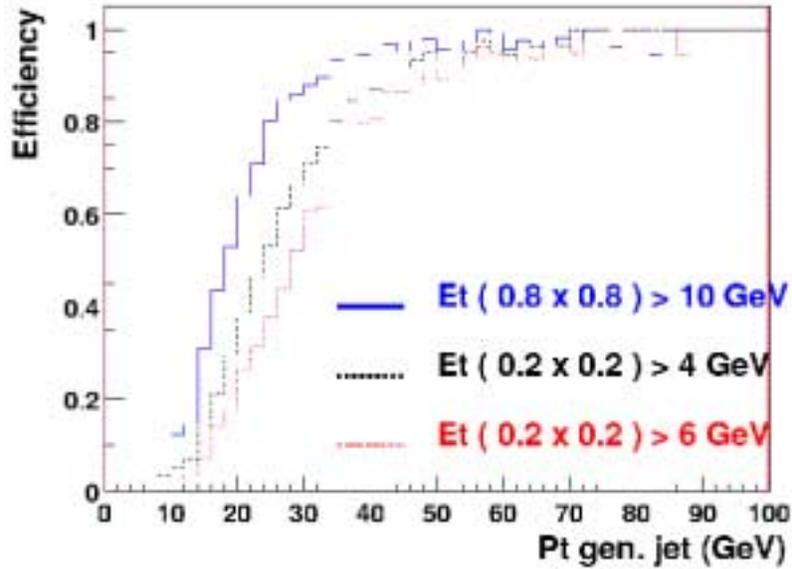


Figure 31. Trigger efficiency as a function of the transverse energy of the generated jet, for the (b) algorithm for $E_T > 10$ GeV (the solid line) and for the current trigger (fixed trigger towers with thresholds of 4 and 6 GeV shown as dashed and dotted lines respectively).

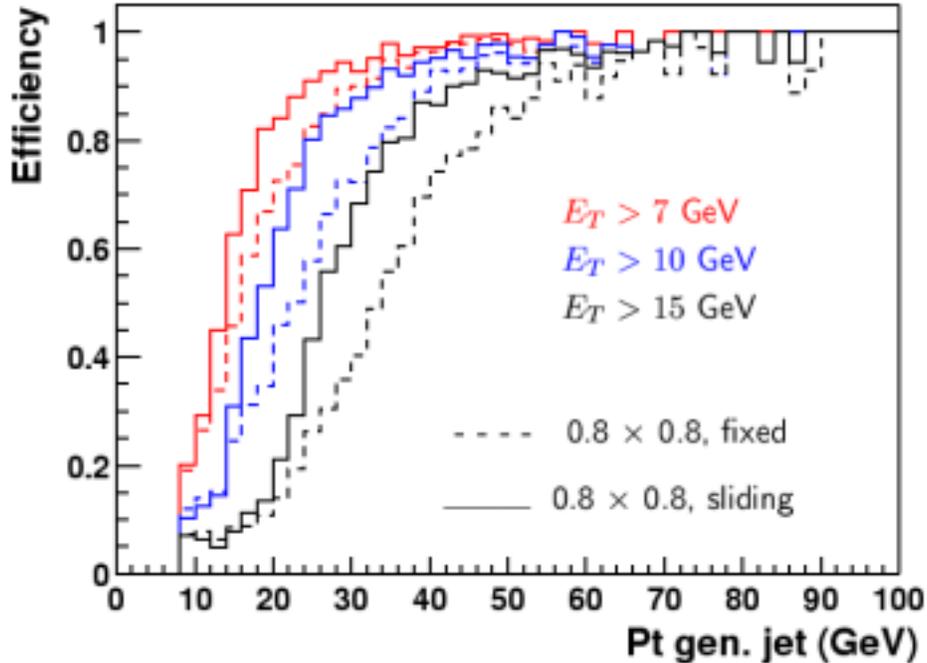


Figure 32. Trigger efficiencies as a function of the generated jet p_T for trigger thresholds $E_T > 7\text{ GeV}$, 10 GeV and 15 GeV (curves from right to left respectively). The solid curves are for the 0.8×0.8 “sliding window” algorithm, and the dashed curves are for a fixed 0.8×0.8 trigger tower in $\eta \times \phi$.

4.7.4 Rates and rejection improvements

In this section, we compare the performance of the sliding window and the existing trigger algorithms. We compare both of these algorithms’ trigger efficiencies and the associated rates from QCD jet events as a function of trigger E_T .

In these studies we require that for the sliding window (b) algorithm there be at least one region of interest with a trigger E_T above threshold which varies from 5 to 40 GeV in steps of 1 GeV. Similarly, for the current trigger algorithm, we require at least one TT above threshold which varies from 2 GeV to 20 GeV in steps of 1 GeV. For both algorithms and for each threshold, we calculate the corresponding inclusive trigger rate and the efficiency to trigger on relatively hard QCD events, *i.e.* with parton $p_T > 20\text{ GeV}$ and $p_T > 40\text{ GeV}$ respectively. To simulate high luminosity running, we overlay additional minimum bias events (a mean of 2.5 or 5 additional minimum bias events) in the Monte Carlo sample used to calculate the rates and efficiencies. While the absolute rates may not be completely reliable given the approximate nature of the simulation, we believe that the relative rates are reliable estimators of the performance of the trigger algorithms. Focusing on the region of moderate rates and reasonable efficiencies, the results are plotted in Figure 33 where lower curves (open squares) in the plots are for the current trigger algorithm and the upper curve (solid circles) corresponds to the sliding window (b) algorithm. It is apparent from Figure 33 the sliding window algorithm can reduce the inclusive rate by a factor

of 2 to 4 for any given efficiency. It is even more effective at higher luminosities (*i.e.* for the plots with 5 overlaid minimum bias events).

The improvement in jet triggering provided by the proposed algorithm is important for those physics processes that do not contain a high p_T lepton which in and of itself offers considerable rejection. Since the sliding window algorithm would be implemented in FPGA-type logic devices, it opens up the possibility of including further refinements in the level of trigger sophistication, well beyond simple counting of the number of towers above threshold. We have studied the trigger for two processes which demonstrate the gains to be expected from a sliding window trigger over the current trigger:

- The production of a Higgs boson in association with a $b\bar{b}$ pair. This process can have a significant cross-section in supersymmetric models with large $\tan\beta$, where the Yukawa coupling of the b quark is enhanced. Thus when the Higgs decays into two b quarks this leads to a $4b$ signature. The final state contains two hard jets (from the Higgs decay) accompanied by two much softer jets. Such events could easily be separated from the QCD background in off-line analyses using b -tagging. But it will be challenging to efficiently trigger on these events while retaining low inclusive trigger rates.
- The associated production of a Higgs with a Z boson, followed by $H \rightarrow b\bar{b}$ and $Z \rightarrow \nu\bar{\nu}$. With the current algorithm, these events could be triggered on using a di-jet + missing energy requirement. The threshold on the missing energy could be lowered if a more selective jet trigger were available.

Figure 34 shows the efficiency versus inclusive rate for these two processes, where three different trigger conditions are used:

1. At least two fixed trigger towers of 0.2×0.2 above a given threshold (dotted curves, open squares).
2. At least one TT above 10 GeV and two TT above a given threshold (dot-dash curve, solid stars).
3. At least two “trigger jets” whose summed trigger E_T ’s are above a given threshold (solid curve, solid circles).

It can be seen that the third condition is the most efficient for selecting signal with high efficiency but low rates from QCD jet processes.

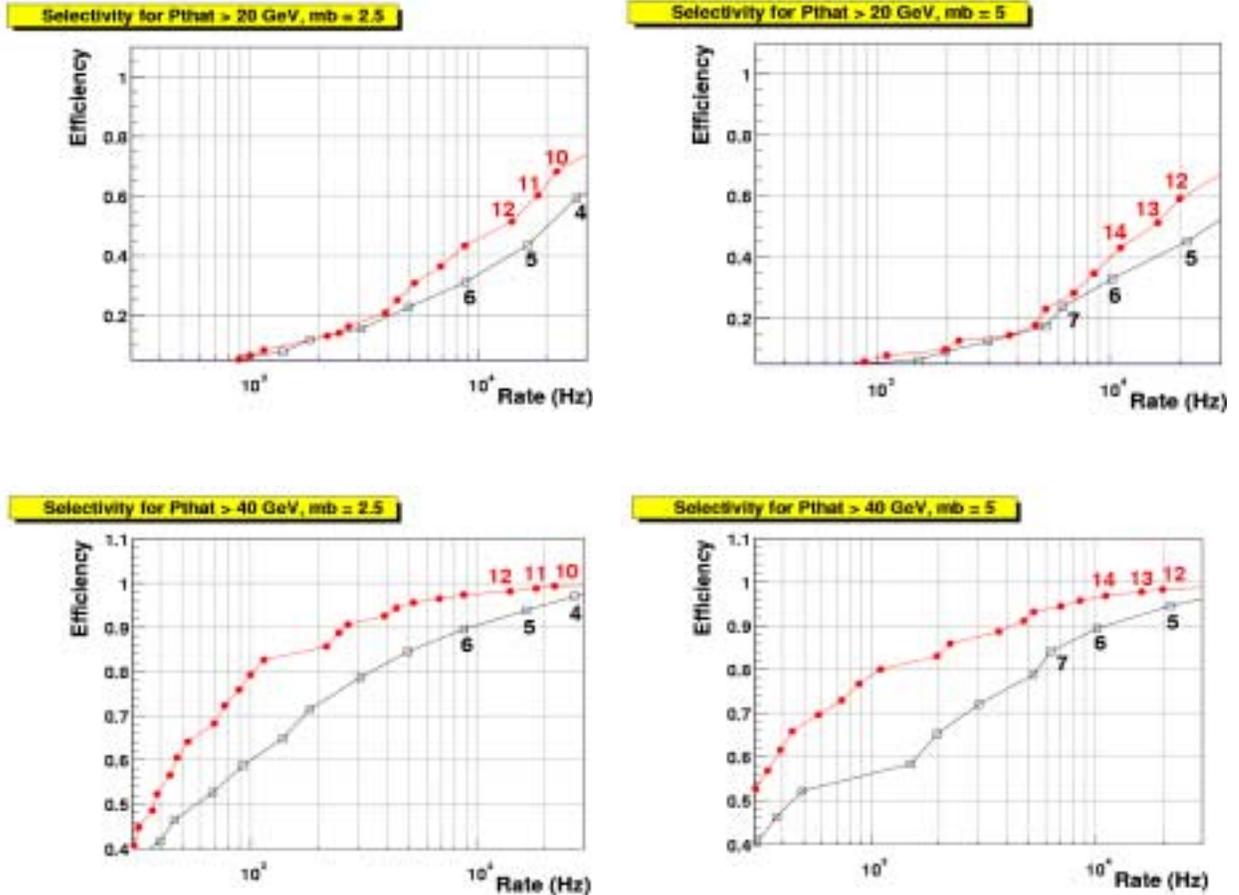


Figure 33. Trigger efficiency for events with parton $p_T > 20$ GeV (upper plots) and parton $p_T > 40$ GeV (lower plots) as a function of the inclusive trigger rate, for the (b) algorithm (solid circles) and the current algorithm (open squares). Each dot (solid circle or open square) on the curves corresponds to a different trigger threshold; the first few are labeled in GeV, and they continue in 1 GeV steps. The luminosity is $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ and the number of overlaid minimum bias (mb) events follows a Poisson distribution of mean equal to 2.5 (left hand plots) or to 5 (right hand plots).

4.7.5 Implementation

These triggering algorithms can be implemented in Field Programmable Gate Arrays (FPGA) on logical processing cards. Each of these cards has responsibility for a region of the calorimeter. Necessarily, there are overlapping areas of these regions as the algorithms must see data belonging to neighboring towers to the tower being analyzed. We can assume that for the processing of one tower, it is necessary to have access to data from a region of maximum size $(\Delta\eta \times \Delta\phi) = 1.0 \times 1.0$ centered on the tower. This mandates overlap regions of

size $\Delta\eta/\Delta\phi = 1.6$ or $\Delta\eta/\Delta\phi = 0.8$ between processing cards, depending on the ultimate ϕ segmentation.

We estimate that the size of electronic circuits available in one year will be large enough to contain the algorithms for a region $(\Delta\eta \times \Delta\phi) = 4.0 \times 1.6$. Choosing the largest possible elementary region has the salutary consequence of minimizing the duplication of data among cards. With this choice, the new trigger system will consist of only eight logical processing cards (to be compared with the more than 400 cards in the old system).

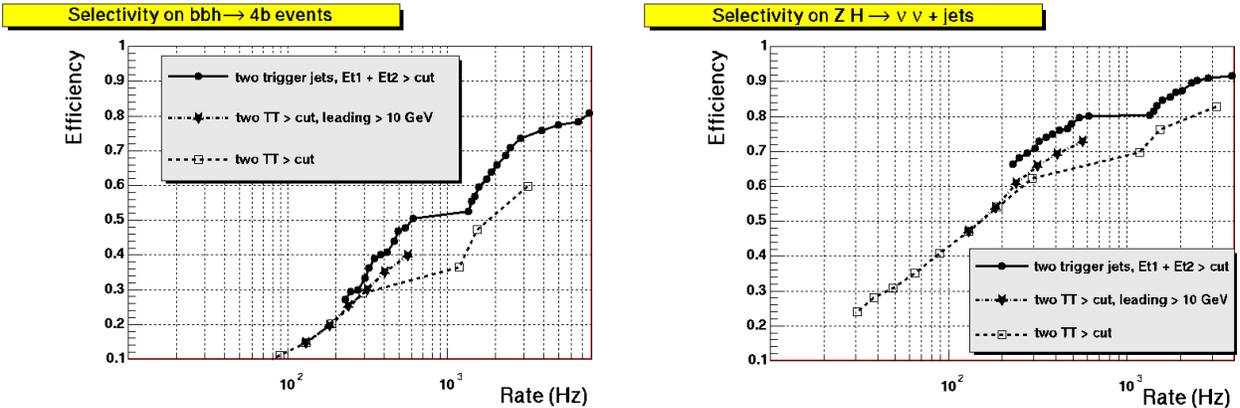


Figure 34. Efficiency to trigger on bbh (left) and ZH (right) events as a function of the inclusive rate. The three conditions shown require: at least two TT above a threshold (dotted, open squares), at least one TT above 10 GeV and two TT above a threshold (dot-dash, solid stars), at least two trigger jets such that the sum of their trigger E_T 's is above a given threshold (solid circles).

4.7.6 Comments

The improvement in the trigger turn on curves and the reduction of QCD backgrounds lead us to conclude that a sliding window trigger algorithm should be adopted for Run 2b. The details of the implementation will require further study.

4.8 Track Matching and Finer EM Segmentation

4.8.1 Concept & physics implications

For the Run2a trigger, the capability to match tracks that are found in the central fiber tracker (CFT) with trigger towers (TT) in the calorimeter at Level 1 is only present in a rudimentary form. Due to restrictions of the calorimeter trigger architecture, the ϕ position of a calorimeter trigger tower can only be localized to a 90-degree quadrant, whereas the CFT tracks are found in 4.5-degree sectors. The full specification of the track parameters within the trigger (e.g., tracks as passed to L1Muon or L2STT) can improve the knowledge of the track position to the single-fiber level ($\Delta\phi \approx 0.1^\circ$) at the outer layer of the CFT. In this section we explore the benefits of significantly increasing the calorimeter ϕ granularity used in track matching. Such an upgrade would be a significant augmentation of the

DØ detector's triggering ability, improving our ability to identify electrons and potentially providing a crucial handle to some of the more difficult but desirable physics we wish to study in Run2b, such as $H \rightarrow \tau\tau$.

4.8.2 Simulation

In this section, we consider first the problem of a calorimeter-centric trigger in which a search for high- p_T EM objects is made by placing thresholds on tower EM E_T . The main objective is to quantify the gain in rejection one can achieve by matching the towers to tracks in order to verify the presence of an electron.

Since the calorimeter trigger tower granularity is currently 2.5 times coarser in ϕ than one tracking sector, we have considered all three of the CFT sectors which at least partially overlap a trigger tower. If there is at least one track with $p_T > 1.5$ GeV pointing at the trigger tower, we consider there to be a match. For comparison, we have also studied the performance of quadrant-track matching, where we group towers into their respective quadrants and match these to overlapping track trigger sectors. (This is the current Run 2a algorithm.)

We note that in these studies there was no attempt made to simulate the sliding tower algorithm, so we might expect some improvements in the final system over what is reported here.

4.8.3 Rates and rejection improvements for calorimeter-based triggers

As a starting point, it is useful to quantify the rate at which high- p_T tracks and high- E_T trigger towers overlap for typical QCD jet events. Table 14 shows the trigger-tower-track occupancy for inclusive QCD jet samples of increasing energy. The occupancy is defined by the fraction of trigger towers with EM E_T above a given threshold which are matched to at least one track, where the matching criteria are those given in the previous section. The MC samples used in this study are generated with an average of 0.7 ISAJET minimum bias events per crossing, which corresponds to a luminosity of $4 \times 10^{31} \text{ cm}^{-2}\text{s}^{-1}$. The fact that more towers with high- E_T are matched to tracks for high- p_T jets is not surprising; the overall trends in the table are as expected.

Table 14. Trigger-tower-track occupancy for different tower E_T thresholds and jet p_T 's, where the entries for every E_T threshold correspond to the total number of towers (denominator) and the number of track-matched towers (numerator). The numbers in parentheses give the fractional occupancy.

EM E_T (GeV)	Jet $p_T > 2\text{GeV}$	Jet $p_T > 5\text{GeV}$	Jet $p_T > 20\text{GeV}$	Jet $p_T > 80\text{GeV}$
>0.5	9k/197k (4.6%)	18k/240k (7.5%)	42k/161k (26%)	73k/147k (50%)
>2	69/297 (23%)	300/1147 (26%)	4k/7506 (53%)	16k/19k (84%)
>5	5/9 (50%)	27/63 (43%)	920/1587 (58%)	7800/9121 (86%)
>10	--	3/7 (50%)	157/273 (58%)	4070/4579 (89%)

As the luminosity increases, we expect a corresponding increase in the rate of real CFT tracks as well as fake tracks. There will also be additional pileup in the calorimeter, leading to more deposited energy. The ability of a calorimeter-track-match algorithm to filter out this additional noise rests on the assumption that the effects of the increased occupancy in the two detector systems are essentially uncorrelated. We can test this assumption by studying the evolution of the trigger-tower-track occupancy as a function of luminosity. Table 15 shows a comparison of the occupancy for two of the samples of Table 14, which were generated at relatively low luminosity, with the occupancy for the same samples but from a simulation of the maximum expected Run 2b rates ($L=5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$). For nearly an order of magnitude increase in luminosity, the rate of correlation between trigger towers of significant energy and high- p_T tracks increases by less than 10% in each case. This suggests that track-calorimeter matching will continue to be a powerful tool for background rejection at the highest luminosities.

Table 15. Trigger-tower-track occupancy for 2 GeV and 20 GeV jet p_T and different tower E_T thresholds for low ($4 \times 10^{31} \text{ cm}^{-2} \text{ s}^{-1}$) and high luminosity conditions ($5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$). The entries in the Table are the same as in Table 14.

EM E_T (GeV)	Jet $p_T > 2$ GeV $4 \times 10^{31} \text{ cm}^{-2} \text{ s}^{-1}$	Jet $p_T > 20$ GeV $4 \times 10^{31} \text{ cm}^{-2} \text{ s}^{-1}$	Jet $p_T > 2$ GeV $5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$	Jet $p_T > 20$ GeV $5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$
>0.5	9k/197k (4.6%)	42k/161k (26%)	200k/1520k (13%)	92k/291k (33%)
>2	69/297 (23%)	4k/7506 (53%)	1100/3711 (30%)	2130/3482 (61%)
>5	5/9 (50%)	920/1587 (58%)	52/132 (39%)	480/703 (68%)
>10	--	157/273 (58%)	--	96/125 (77%)

The huge numbers of real (and fake) low-momentum tracks in minimum bias events will make it impractical to use a track p_T threshold of only 1.5 GeV, even for electron identification. More reasonable values will be more like 3 or 5 GeV, and maybe up to 10 GeV. Since the rate of fake tracks at these higher momentum thresholds also increases with luminosity, the rate of correlation as a function of track p_T must also be considered. Table 16 shows such a study, where the trigger-tower-track occupancy has been derived for a sample of low- p_T jet events at occupancies characteristic of a luminosity of $5 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$.

Table 16. Trigger-tower-track occupancy for a sample of jets with $p_T > 2$ GeV at 5×10^{32} cm⁻²s⁻¹. The rate at which tracks of varying p_T are matched to calorimeter trigger towers of increasing E_T thresholds is shown. The entries in the Table are the same as in Table 14.

EM E_T (GeV)	Track $P_T > 1.5$ GeV	Track $P_T > 3$ GeV	Track $P_T > 5$ GeV	Track $P_T > 10$ GeV
>0.5	200k/1520k (13.2%)	70k/1520k (4.6%)	30k/1520k (2%)	10k/1520k (0.7%)
>2	1100/3711 (30%)	600/3711 (16.2%)	211/3711 (6%)	60/3711 (2%)
>5	52/132 (39%)	34/132 (26%)	19/132 (14%)	11/132 (8%)
>10	4/12 (30%)	4/12 (30%)	2/12 (20%)	2/12 (20%)

These results show that the fake, high- p_T tracks resulting from the high CFT occupancy at high luminosity are as uncorrelated with towers of similar E_T as low- p_T tracks (fake or not) with analogous towers. Reductions in the EM trigger rate by a factor of 2 are easily possible by requiring that a high- E_T EM tower match a track of similar p_T . It is interesting to note that they also suggest the presence of a small irreducible background where high- p_T tracks point at high- E_T EM clusters even in this very low- p_T jets sample.

The above studies clearly demonstrate a potential reduction in the EM trigger rate by exploiting the correlation of track and calorimeter information. One remaining question is the relative gain of this approach over the current Run2a L1CAL algorithm, which can only match tracks to quadrants of the calorimeter. In order to simulate this situation we group trigger towers into their respective quadrants and match these to the overlapping CFT sectors. Table 17 shows a comparison of these two situations, where the trigger-tower-track occupancy is shown for the same high-luminosity low- p_T sample as Table 16, but with tracks matched to individual trigger towers or full calorimeter quadrants.

Table 17. Trigger-tower-track occupancy for a sample of jets with $p_T > 2$ GeV at 5×10^{32} cm⁻²s⁻¹. The table presents a comparison of the rate at which tracks of $p_T > 1.5$ GeV or $p_T > 10$ GeV are matched to an individual trigger tower or a calorimeter quadrant containing an EM tower above a given threshold. Each line in the table contains the number of matches divided by the total number of quadrants or towers above that E_T threshold.

EM E_T	Track $p_T > 1.5$ GeV (quadrants)	$p_T > 1.5$ GeV (towers)	Track $p_T > 10$ GeV (quadrants)	$p_T > 10$ GeV (towers)
2 GeV	2470/3711	1100/3711	225/3711	60/3711
5 GeV	103/132	52/132	21/132	11/132
10 GeV	8/12	4/12	2/12	2/12

While momentum-matching between the calorimeter and the tracking systems offers some background rejection, these results clearly indicate that the exploitation of the full calorimeter position resolution is necessary to attain the full rejection power of this algorithm. The track-calorimeter matching with higher spatial resolution offers another factor of 2 to 3 in rejection against the low p_T , high multiple-interaction events that are so problematic for the Level 1 trigger.

4.8.4 Rates and gains in rejection for tracking-based triggers

The previous section has presented clear evidence that the addition of track information can improve the rejection of an electron trigger by requiring a track close in ϕ to the high- E_T tower. In this section we explore the equally useful converse, namely that the calorimeter can be used to improve the selectivity and background-rejection of tracking triggers. Isolated high- p_T tracks are signatures of many types of interesting events. However, the triggers that select these tracks suffer from a large background of fakes, even for a track $p_T > 10$ GeV. As has been indicated elsewhere in this document, this problem worsens substantially as the number of multiple interactions increases. The matching of these tracks to signals in the calorimeter has the ability to confirm the existence of the tracks themselves, and also to verify their momentum measurement.

In this study, our matching algorithm considers individual sectors with at least one track of a given minimum p_T , and matches them in ϕ to whatever trigger towers they overlap. By doing this, we avoid double counting some of the redundant track solutions that cluster near to each other. In about one third of the sectors, these tracks will overlap two different trigger towers in ϕ : each match is counted separately. The results of this matching are shown in Table 18 for the same low p_T jets sample at high luminosity. Note that for this study, the E_T in the table is the Total E_T (EM+EH), not just the EM E_T . Given that most tracks are hadrons, this is more representative of the true energy that should be matched to a given track.

Table 18. Trigger-tower-track matching for a sample of jets with $p_T > 2$ GeV at 5×10^{32} $\text{cm}^{-2}\text{s}^{-1}$. The number of CFT trigger sectors containing at least one track above a given p_T threshold is shown, both without and with matching to calorimeter trigger towers of increasing total E_T .

track p_T	# sectors with tracks	Tot $E_T > 1$ GeV	> 2 GeV	> 5 GeV	> 10 GeV
> 1.5 GeV	52991	16252	3218	200	13
> 3 GeV	12818	5188	1529	144	13
> 5 GeV	4705	1562	476	73	9
> 10 GeV	2243	655	141	31	5

In this situation, we find substantial rejections from even mild trigger tower thresholds. For example, a 10 GeV track matching to a 5 GeV trigger tower

provides a factor of ~ 70 rejection against fakes. Matching any track to a 2 GeV tower provides approximately a factor of 10 rejection. The rejection shown in this table is essentially sufficient to allow the high- p_T single and di-track triggers to function at the highest luminosities. There are several caveats for these results: first, the Monte Carlo used for the simulation of the minimum bias backgrounds is the PYTHIA simulation, which may underestimate the CFT occupancy, lowering the number of fake tracks. It is not clear at this point whether this would lead to better or worse rejection results from the simulation. Second, it is likely that the rejection factor of the calorimeter is underestimated here, since in the actual system the track match can be done using the full CFT track parameters, which are much more precise than the sector location. This would lead to a match with a single calorimeter tower instead of all that overlap a given sector. In any case, further studies of efficiencies for various physics channels are underway. At this preliminary stage this is a very promising result.

4.8.5 Track-matching improvements with an EM granularity of $\Delta\phi=0.1$

Given the significant rejection factors and robustness to multiple interactions the sector-level matching gives, we would like to know if there is a further way of improving the rejection by segmenting the EM calorimeter towers more finely to better match the CFT granularity. Since the finer granularity causes large energy sharing among neighboring towers, the simplest study one could envision involves segmenting the EM energy appropriately and then crudely clustering it to retain the full shower energy, but with better position resolution. Ideally, we would like to apply the moving window scheme described elsewhere; instead for expediency we perform this study with a simpler algorithm. We take EM trigger tower seeds above 1 GeV and add the E_T 's of the surrounding eight towers. We also calculate the E_T weighted ϕ for the cluster in this 3x3 window. This simple algorithm is applied for both the 0.2 and 0.1 granularity scenarios. Naively, we expect about a factor of 2 in improved rejection due to the improved geometry. In practice, the granularity has an effect on how the energy is clustered (*i.e.* what E_T one calculates per cluster) in addition to the positioning of the cluster.

The sample we used was a high- p_T ($p_T > 20$ GeV) jet sample (1684 events) with no minimum bias overlay. The track-cluster matching started with sectors having tracks and matched them to EM clusters. For the match, we required that the sector center be within half the EM ϕ granularity of the EM cluster ϕ centroid. The resulting rates are given in Table 19.

Table 19. Comparison of the calorimeter-track matching rates for 0.1 and 0.2 $\Delta\phi$ granularities vs. the track p_T and EM cluster threshold. The second column gives the number of sectors with tracks above the given threshold, and the next four columns give the ratio of the number of sectors matching EM clusters of the given E_T threshold for 0.1/0.2 granularities respectively.

track Pt	sectors w/trks	EM>1GeV	EM>2GeV	EM>5GeV	EM>10GeV
>1.5GeV	7171	896/2101	740/1945	241/1139	52/379
>3GeV	3085	531/1201	451/1152	151/736	31/275
>5GeV	1107	240/493	210/483	89/326	21/136
>10GeV	217	60/98	52/97	39/77	10/42

The main feature of these results is that there seems to be a factor of 1.5 to 3 gain in rejection by going to 0.1 granularity in EM ϕ . This is likely just the geometrical gain from avoiding tracks randomly distributed in the jet containing the EM cluster. Surprisingly, larger relative rejections seem to be attained when we consider matching low p_T tracks with high E_T towers. These may be situations where the EM cluster is dominated by photon deposition from a leading π^0 , which may be anti-correlated with the low p_T tracks in the jet from charged hadrons. This requires further study.

4.8.6 Implementation

The track matching hardware could be accommodated in the proposed designs of the L1 calorimeter trigger system (see the hardware implementation section later on in the document). However, there are significant cost, design and manpower issues that are raised if finer (x2) EM trigger towers are implemented. The BLS trigger sum driver hybrid would be replaced with a new hybrid capable of driving (single-ended) the cable to the L1 calorimeter trigger system through the existing cable plant. The factor of two increase in the number of EM signals would essentially double the electronics count for those channels and add complexity to the system. The full ramifications of this finer segmentation are not yet fully understood and require further study.

4.8.7 Conclusions

The track matching studies show that there are considerable gains to be made by implementing this algorithm. The effects of high occupancy in the tracking and calorimeter systems seem to be largely uncorrelated, implying that the power of their combination to filter physics triggers from the background noise remains largely intact at high luminosities. Refining the position resolution of the track-calorimeter matching from a calorimeter quadrant to the level offered by the L1CAL upgrade offers at least a factor of 2 to 3 in additional rejection of high-occupancy events for a medium- p_T electron trigger.

There are also significant benefits from the point of view of the tracker, where track matching is used to verify track triggers rather than calorimeter triggers. Strong (factors of 10-70) rejection of fake tracks is possible by matching them to calorimeter towers of modest energy.

Segmenting the EM trigger towers to 0.1 in phi might provide a potential factor of three further improvement in rejection for fake electron triggers.

Our conclusion is to support the implementation of a track-matching algorithm that can take full advantage of the calorimeter position resolution provided by the new L1CAL trigger, although the precise details of the algorithm will require further study. The question of the EM trigger tower segmentation should be deferred until more studies are completed.

There are also significant benefits from the point of view of the tracker, where track matching is used to verify track triggers rather than calorimeter triggers.

The further improvements contemplated by further segmenting the EM trigger towers in 0.1 in ϕ might provide a potential factor of three further improvement. Also, if one tightens the track p_T requirement beyond 1.5 GeV, then the rejection improves substantially again.

Our conclusion is to support the implementation of a track matching algorithm, although the precise details of the algorithm will require further study, and the question of the EM trigger tower segmentation should be deferred until more studies are completed.

4.9 Improving Missing E_T Triggering using ICR Energy at Level 1

The region around $0.8 < |\eta| < 1.5$, known as the inter cryostat region (ICR) encompasses the transition from showers contained within the CC and showers contained within the EC. There is a gap in EM coverage and a major thinning of FH coverage in this area. Since these are the layers which comprise standard trigger towers, there is a major degradation in Level 1 calorimeter response and resolution in this region. This is exacerbated by the presence of significant dead material in the solenoid in Run2. To aid in recovering the energy losses in the ICR region, we use the intercryostat detectors (ICD), which consists of scintillators located in the gap between the calorimeter cryostats, and the “massless gaps” (MG) which consist of the front sections of the endcap calorimeter that have no absorber in front. In this section we study ways to improve the energy measurement at the trigger level.

4.9.1 Concept & performance

Global tower E_T sums such as missing E_T or scalar E_T , while very useful, suffer from several significant problems at the L1 trigger. There are two significant issues: first is that the ICR sampling layers are not available in the calculation at Level 1; second is that the imprecision of the tower E_T 's gets compounded for global sums, resulting in significantly degraded effectiveness. This is particularly true in a multiple interaction environment. There are two possible solutions to these problems. First we can take advantage of work done for Run2a to make the ICR layers available at Level 2 and add these towers back into the global sums at Level 1 in Run2b. Second, we can develop a scheme which discriminates towers which are from multiple interactions and avoids adding them into the sum.

Simulations of single pions and jets in this region indicate that the energy scale in this region goes as low as 40% of the CC/EC scale (as shown in Figure 35), and the resolution is as bad as 6 times worse than in the CC or EC (as shown in Figure 36). These results are very consistent with findings from Run1 Level 1 missing E_T analyses (see Figure 37). One of the major results of this deficiency is that the efficiency and rejection of a Level 1 missing E_T selection are noticeably degraded. These simulations also indicate that adding ICD and MG cells into trigger towers can improve the scale by a factor of 2, while optimizing the resolution by a factor of 3.

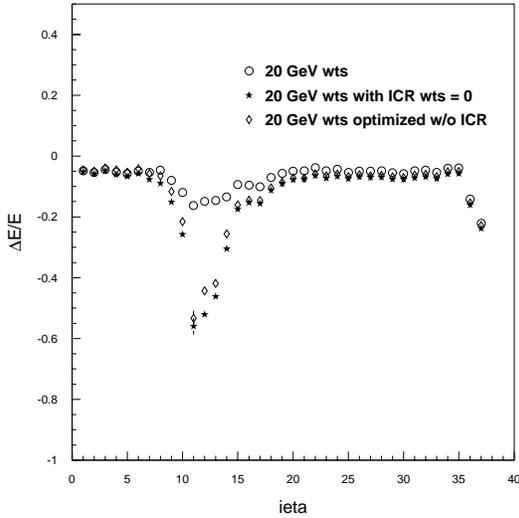


Figure 35. The relative calorimeter energy response in the ICR region for incident 20 GeV pions as a function of $\eta \times 10$. The stars are the response if the ICR weights are set to zero, the open diamonds are the response if the ICR energies are ignored and the remaining calorimeter weights are re-optimized, and the open circles are the response when the ICR region is included and the weights are optimized.

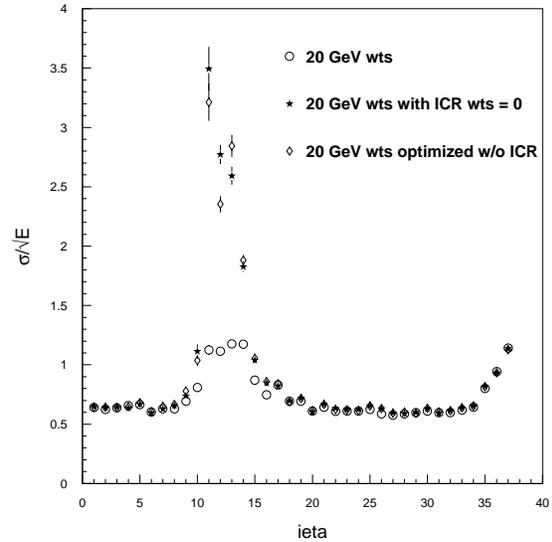


Figure 36. The calorimeter energy resolution in the ICR region for incident 20 GeV pions as a function of $\eta \times 10$. The stars are the response if the ICR weights are set to zero, the open diamonds are the response if the ICR energies are ignored and the remaining calorimeter weights are re-optimized, and the open circles are the response when the ICR region is included and the weights are optimized.

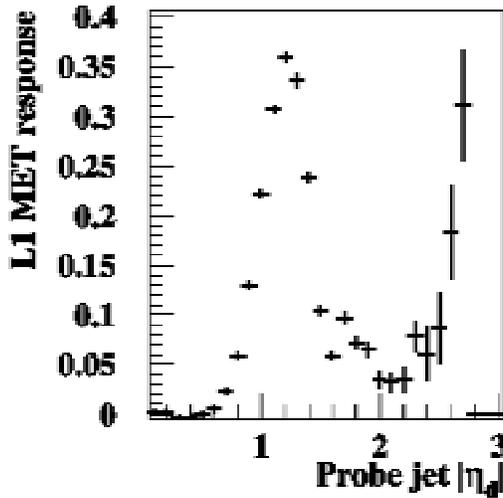


Figure 37. The L1 missing E_T response as a function of η for 85 GeV jets using the Run 1 DØ detector simulation.

4.9.2 Simulation results

In principle, it is straightforward to estimate the effect of the ICD and MG to the missing E_T calculation. However our present simulations do not yet fully address a number of issues (including a proper treatment of trigger tower sampling weights, the verification of the modeling and calibration for the ICR, and the proper mapping of calorimeter cells in the MC). The last of these problems is easily solved, but the first two present a larger problem, and so until such time as we have resolved these problems, we will estimate the expected improvement based on other studies.

To estimate the effect of adding the ICR detectors into the missing E_T , we consider the fact that in the region of $1.0 < |\eta| < 1.4$, the sampling weight simulations indicate approximately half of the energy will be deposited in the EM+FH, and the other half in the ICD+MG. As a crude estimate of the magnitude of the effect of adding the ICR layers, we will merely consider the missing E_T measurement with and without the EM+FH layers in this region and assume the ICR improvement will be similar. Although the sample used for this calculation is a QCD sample with jet $p_T > 20$ GeV and 0 minimum bias events overlaid, for historical reasons it is a different sample than that mentioned in the rest of this document with the same specifications. The missing E_T mean and rms in this sample behave as follows:

if remove all ICR TTs: $\mu/\text{rms} = 6.7 \text{ GeV} / 4.8 \text{ GeV}$

if only use EM+FH TTs: $\mu/\text{rms} = 5.5 \text{ GeV} / 3.9 \text{ GeV}$

The number of events passing various Level 1 missing E_T cuts in this sample are shown in Table 20.

Table 20. Events passing L1 missing E_T cuts when the ICR energy is included and when it is removed from the trigger towers.

L1 ME_T	Without ICR	With ICR
> 5GeV	948	766
> 10 GeV	337	185
>15 GeV	95	40
> 20 GeV	37	11
> 25 GeV	9	4

Thus, the region is important to the missing E_T calculation and the rates of passing 15 or 20 GeV selection can change by factors of around 2.5-3. A proper treatment of the gains from adding in the ICD and MG, however, will have to await a satisfactory treatment of the relative weights of various layers.

4.9.3 Improving Missing E_T for Multiple interaction Events

Our experience in Run1 indicated the Level 1 missing E_T to be very sensitive to the number of multiple interactions. This results from several factors, including the fact that the fundamental trigger tower fractional energy resolution is poor, especially for very low E_T towers, and the numbers of these towers increases substantially with the number of multiple interactions. As a result, we have explored three ways in which we might improve the missing E_T resolution to reduce this problem in Run2b.

First, we varied the low threshold on the E_T of towers going into the global sum. In Run1, this threshold was 0.5 GeV and was not studied in detail in the light of multiple interactions. Again, we have used the QCD $p_T > 2$ GeV and $p_T > 20$ GeV samples with 0 minimum bias (mb) events overlaid, a 5mb overlay, and a 10mb overlay. We have used the $t\bar{t}$ sample with 2.5 mb overlays for the signal. If we calculate the missing E_T mean and the rms in these samples for various E_T thresholds, we find the results shown in Table 21.

Table 21. Change in the means and rms for the missing E_T for background (QCD) and signal ($t\bar{t}$) samples as a function of the trigger tower (TT) threshold. A selection of 1.5 GeV on trigger towers removes most of the multiple interaction variation for the QCD samples, while having little effect on the signal top sample.

ME_T calc	2 GeV QCD (μ /rms) in GeV	20 GeV QCD 0mb (μ /rms) in GeV	2 GeV QCD 10 mb (μ /rms) in GeV	20 GeV QCD 5mb (μ /rms) in GeV	ttbar (μ /rms) in GeV
TT>0.5GeV	1.0/1.0	5.1/3.8	3.1/2.2	6.5/4.2	35.9/25.4
TT>1GeV	0.6/0.9	5.2/3.9	2.3/1.9	5.8/4.0	35.4/24.7
TT>1.5GeV	0.3/0.7	5.3/4.1	1.6/1.9	5.6/4.0	35.0/24.1
TT>2GeV	0.1/0.6	5.2/4.2	1.0/1.7	5.4/4.2	34.6/23.6

The error on the mean and RMS for the QCD samples is approximately 0.1 GeV. The cut of 2GeV reduces the mean of the QCD sample noticeably. If we consider the 20 GeV sample, the trigger tower cut of 1.5 GeV provides a 20% to 30% lower pass rate for moderate missing E_T selections. Although scalar E_T is generally considered a poor variable at Level 1 because of its sensitivity to multiple interactions, we have studied its mean and rms (see Table 22) for the same thresholds to see what is happening:

Table 22. Change in the means and rms for the E_T scalar sum for background (QCD) and signal (ttbar) samples as a function of the trigger tower (TT) threshold.

Sum E_T calc	2 GeV QCD 0.7 mb(μ /rms) in GeV	QCD 0 mb (μ /rms) in GeV	2GeV QCD 0.7 mb(μ /rms) in GeV	QCD 5mb (μ /rms) in GeV	ttbar (μ /rms) in GeV
TT>0.5GeV	2.9/3.3	23.5/13.0	21.2/18.1	57.7/39.3	179.7/68.8
TT>1GeV	0.8/1.5	17.9/11.9	6.5/7.1	26.6/15.8	161.1/66.4
TT>1.5GeV	0.3/1.1	14.7/11.4	2.8/4.2	18.0/12.5	151/64.9
TT>2GeV	0.2/0.8	12.5/11.1	1.5/3.1	14.2/11.6	143.6/63.8

Comparison of the two QCD samples indicates that low thresholds let in an enormous amount of energy which has nothing to do with the hard scatter interaction.

Because the typical low p_T QCD event E_T is distributed flat in η , we might not expect a degradation in the global sum behavior from including forward trigger towers in the calculation of these quantities. In fact, when looking in simulated events even with large numbers of multiple interactions, one finds very little transverse energy in this region. However, our experience in Run1 indicated strongly that use of forward towers (ie. those around $|\eta| \sim 3$ or more) substantially degraded the missing E_T behavior. This was especially true in a multiple interaction environment. As a result, we suspect strongly that there is a benefit from being able to easily select what the range is for the calculation, or perhaps include the η parameter into a weighting scheme with the trigger tower E_T . This requires further study only possible once data is available.

Another concern for the missing E_T measurement involves the truncation of trigger tower E_T 's into 0.5 GeV bins. Since one to two hundred towers are typically added into the Missing E_T , this resolution loss can start to be noticeable. Taking the QCD $p_T > 20$ GeV sample with minimum bias overlay of 0 and 1648 events, we can use the simulator described above in the ICR discussion and toggle truncation on and off. The results are shown in Table 23.

Table 23. Comparison of the effect of TT truncation on the missing E_T . The table lists the number of events (out of a sample of 1648, QCD with $p_T > 20\text{GeV}$ and no minimum bias overlaid events) that pass the listed missing E_T thresholds.

Missing E_T	no truncation	no truncation, $TT > 0.5\text{GeV}$	with truncation
$>5\text{ GeV}$	947	868	766
$>10\text{ GeV}$	309	261	185
$>15\text{ GeV}$	76	51	40
$>20\text{ GeV}$	22	17	11
$>25\text{ GeV}$	7	5	4

The first column indicates truncation turned off and no threshold applied to trigger towers. The second column also has no truncation and zeros out all towers with $E_T < 0.5$. The third column employs the normal 0.5 GeV truncation. Since truncation lowers tower E_T 's only to the next lowest 0.5 GeV increment, it effectively deweights all of the poorly measured E_T in low E_T towers. In fact, if we consider the QCD $P_t > 20\text{ GeV}$ sample with 5mb already discussed, the missing E_T mean and rms are mildly improved over the straight 1.5GeV threshold by a simple weighting scheme. If we choose weights of 5%, 25%, and 75% for $E_T = 0.5, 1.0, \text{ and } 1.5\text{ GeV}$, respectively, we find the results shown in Table 24.

Table 24. Comparison of simple TT threshold vs. weighting scheme for 20GeV QCD jet sample.

Scheme	μ (GeV)	rms
TT $E_T > 1.5\text{ GeV}$:	5.41	4.20
Weighted TT:	5.41	3.96

If the capability exists in an FPGA to enforce a weighting scheme, then one might devise a scheme which does better than this.

Because the trigger tower threshold seems to be the simplest solution that shows progress, and the weighting also seems to help, one might ask whether rejecting low E_T towers unless they are near significant neighbors might help. Looking again in the 5mb QCD sample at missing E_T means and sigmas, we find the results shown in Table 25. These results point to a significant degradation in missing the E_T mean and resolution.

Table 25. Comparison of effect of rejection low ET towers unless they are near trigger towers (NN) with significant energy deposits.

Cut	μ (GeV)	rms (GeV)
None :	6.45	4.17
NN $E_T > 0.5$ GeV:	6.45	4.37
NN $E_T > 1.5$ GeV:	6.56	4.37
NN $E_T > 3.0$ GeV:	6.72	4.86
NN $E_T > 10$ GeV:	5.62	4.57
NN $E_T > 1k$ GeV:	5.41	4.20

4.9.4 Conclusions

In this section, we have explored several different ways to improve the calorimeter missing E_T measurement at Level 1. Studies leading to the optimization of the Run2a trigger have indicated a large improvement in the scale and resolution of jets in this region if the ICD and MG are used. Although our current simulation samples do not have a proper treatment of this region, a crude estimate indicates that this amount of energy should have a noticeable improvement on the missing E_T resolution.

Several attempts were also made to improve the behavior of missing E_T in a multiple interaction environment. The most promising appears to be a simple tightening of the E_T threshold on a trigger tower to around 1.5 GeV which would reduce the background by around 20% in our QCD sample. The actual degradation in the real data may be larger than we see here, however, and the corresponding gain may also increase. We will be in a better position to evaluate this when we have reliable data at various luminosities. There is some evidence that a weighting scheme would provide further benefits.

4.10 Finer EM Tower Segmentation for electrons

4.10.1 Concept

The gains from larger trigger towers and the sliding window algorithm is apparent for jets. Given the much smaller extent of electromagnetic showers we were led to explore the possible gains from smaller EM towers with or without a sliding window algorithm.

4.10.2 Simulation

Monte Carlo single electrons have been used to compare the performances of the various options:

1. Fixed trigger towers of 0.2×0.2 (the current system)
2. Fixed trigger towers of 0.2×0.1 in $\Delta\eta \times \Delta\phi$

3. Trigger towers of size 0.2×0.2 which slide in either the η or ϕ direction by steps of 0.1 .

The direction of the generated electron is extrapolated to the calorimeter surface and trigger regions are looked for in the neighborhood of the intersection point.

Figure 38 shows the transverse energy seen in the trigger region for cases (2) and (3), normalized to that seen by the current trigger. It can be seen that fixed trigger towers of size 0.2×0.1 will see $\sim 5\%$ less E_T than the current TTs. A slightly larger energy is deposited in windows which are sliding in the η rather than in the ϕ direction. This is due to the fact that when the Z_{vertex} is not zero, the calorimeter geometry is not projective in η (while it is always projective in ϕ). Figure 39 shows that indeed, when electrons are emitted at $Z_{\text{vertex}} \approx 0$, overlaps in η and overlaps in ϕ yield similar energy deposits in the trigger regions.

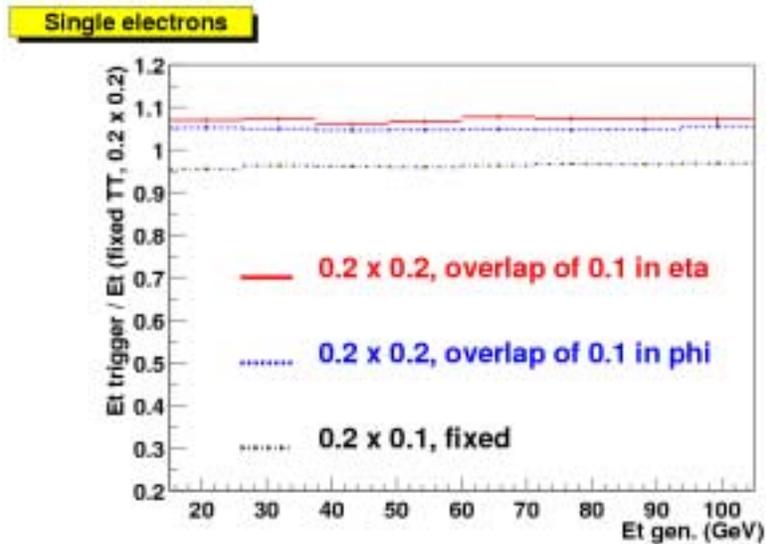


Figure 38. Ratio of the E_T measured in various possible trigger regions to the E_T seen by the trigger when using fixed 0.2×0.2 TTs.

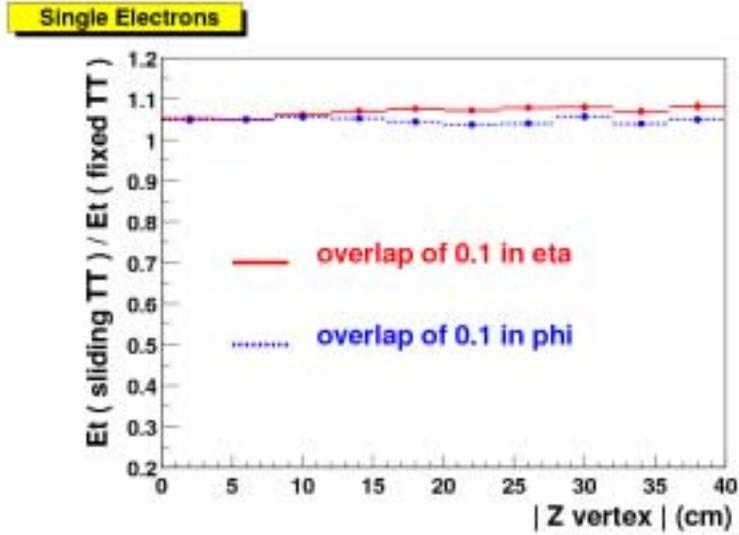


Figure 39. Ratio of the trigger E_T seen by using sliding windows of 0.1 in η or in ϕ to the E_T seen in the current trigger towers, as a function of the Z_{vertex} .

4.10.3 Efficiency

The efficiencies on single electron events are summarized in Table 26.

Table 26. Efficiencies for single electron events.

$E_{T,e}$ (GeV)	Trigger threshold (GeV)	0.2 x 0.2 (fixed)	0.2 x 0.2 sliding in η	0.2 x 0.2 sliding in ϕ	0.1 x 0.2	0.2 x 0.1
10	5	91.1%	94.5%	94.5%	86.1%	89.0%
10	7	69.6%	78.0%	76.4%	57.4%	59.1%
20	10	90.5%	93.4%	93.9%	86.9%	88.6%

The single electron efficiency vs. the inclusive QCD rate has also been studied. In these studies the three algorithms have been compared using a trigger requirement that demanded at least one EM TT above a given threshold (with no hadronic fraction veto). The rate is calculated assuming a luminosity of $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ with an average of 2.5 overlaid minimum bias events. The efficiency for the central region, $|\eta| < 1.2$, is shown in Figure 40. The three algorithms perform similarly at the smaller thresholds, but the 0.2x0.1 fixed window algorithm is somewhat more efficient at large trigger thresholds. There are no indications of dramatic performance gains from either the finer segmentation or the overlapping windows.

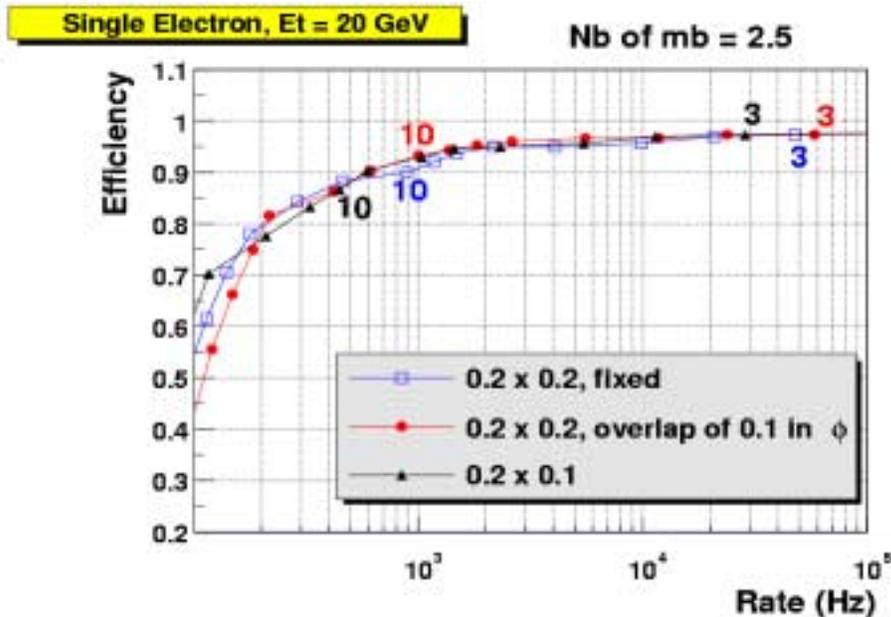


Figure 40. The single electron efficiency for $|\eta| < 1.2$ vs. the QCD inclusive rate for a luminosity of $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ for three different algorithms. The algorithms are 0.2x0.2 fixed window (open squares), 0.2x0.2 sliding window with a 0.1 overlap (solid circles), and a fixed window of 0.2x0.1 (solid triangles). The points represent different trigger thresholds (in steps of 1 GeV) with 3 and 10 GeV indicated for reference.

4.10.4 Comments

The implementation of finer EM segmentation has considerable impact on the complexity, size and cost of the L1 calorimeter trigger. The required changes start with the BLS trigger sum driver hybrid and propagate through essentially a doubling of numbers of boards in the L1 calorimeter trigger. The full hardware implications of implementing this finer granularity have not yet been fully studied.

We do not yet have a complete understanding of the gains that a finer EM segmentation would offer, although these first looks suggest that the improvement is not significant. Since the cost (in complexity, funds and manpower) of implementing this option is quite high, we conclude that more studies must be done before making a final decision on the granularity. In addition, these studies must be completed soon because of the large impact on the system design.

4.11 Topological Considerations

4.11.1 Concept & physics implications (acoplanar jets)

The search for Higgs boson is the central element of the Run 2b physics program. The Run II Higgs workshop report¹ concluded that the channel $p\bar{p} \rightarrow HZ \rightarrow b\bar{b} \nu\bar{\nu}$ was critical. This final state poses a difficult topology, two relatively soft jets ($p_T < M_{H/2}$) with modest missing E_T . For a Run 1 style di-jet plus missing E_T trigger, the nominal calorimeter trigger tower and missing E_T

thresholds are such that the efficiency for the $b\bar{b}\nu\bar{\nu}$ channel is compromised. The trigger efficiency is driven by the allowable Level 1 rate. While b-tagging can be used at Level2 to control the rate, it is important to note that b tagging will not be possible at Level 1. Thus, it is clear that this channel relies on alternative triggering techniques at Level 1.

4.11.2 Efficiency

To efficiently trigger on the HZ channel one can exploit the unique topology: the Higgs boson recoils from a massive particle decaying invisibly, thereby leading to an acoplanar jet topology. From Monte Carlo based studies, it has been demonstrated that the L1 central track trigger (L1CTT) can be used to identify acoplanar topologies using the fiber tracker. The algorithm is based on identifying the 4.5° wide sector having the highest track p_T sum within the two 45° wide octants having the highest track p_T sum. In Figure 41, the opening angle between the leading partons is shown; the binning reflects the central fiber tracker (CFT) azimuthal segmentation. The red histogram represents the true opening angle and the blue is the corresponding angle reconstructed from charged tracks in the CFT using the above algorithm. Note the QCD background is predominately back-to-back (i.e. the most probable opening angle is 40 sectors or 180°) whereas the Higgs boson signal has a substantial acoplanar component. Figure 42 shows the correlation between $\Delta\phi$ and the missing E_T of the event for signal and representative QCD backgrounds. The figures demonstrate that combining an acoplanar topology cut ($N_{\text{sector}} < 35$) with a looser missing E_T requirement can maintain good signal efficiency while still suppressing most of the QCD background.

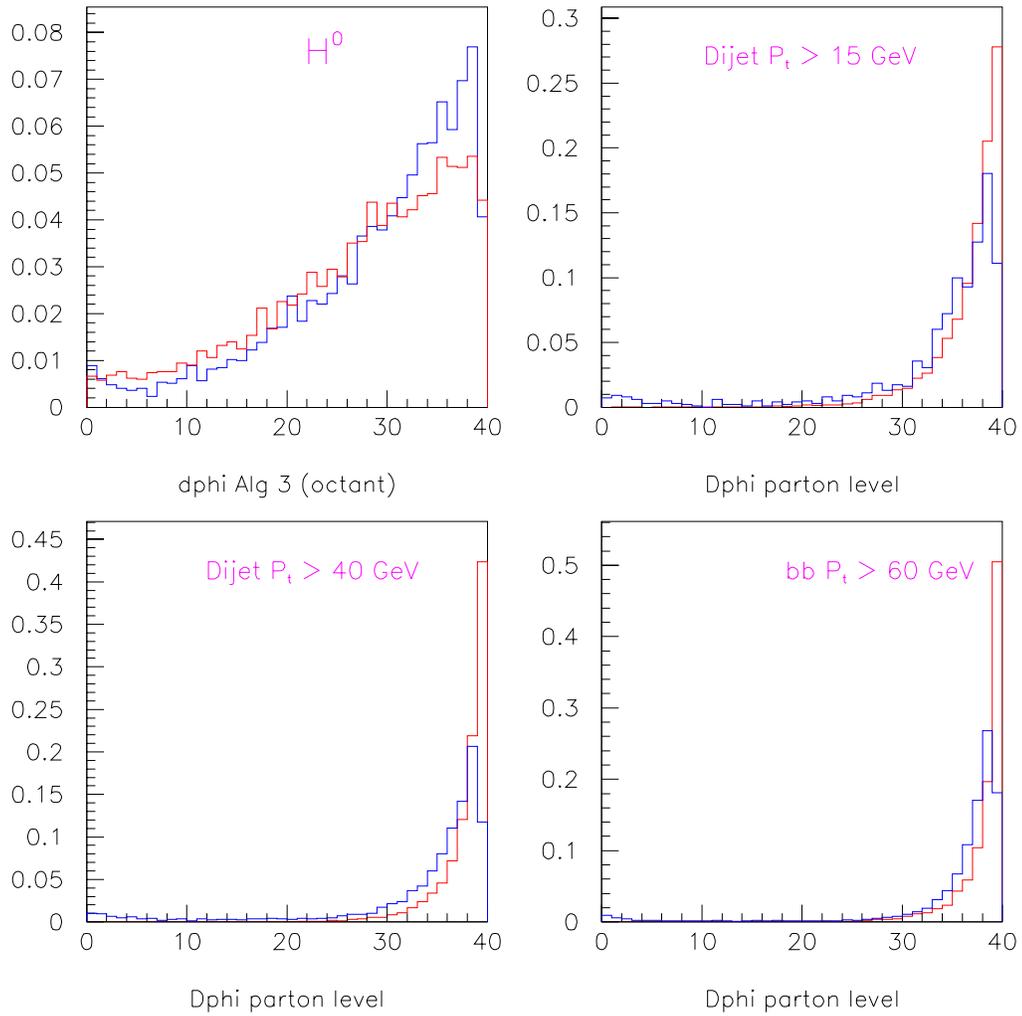


Figure 41. The opening angle between the leading partons.

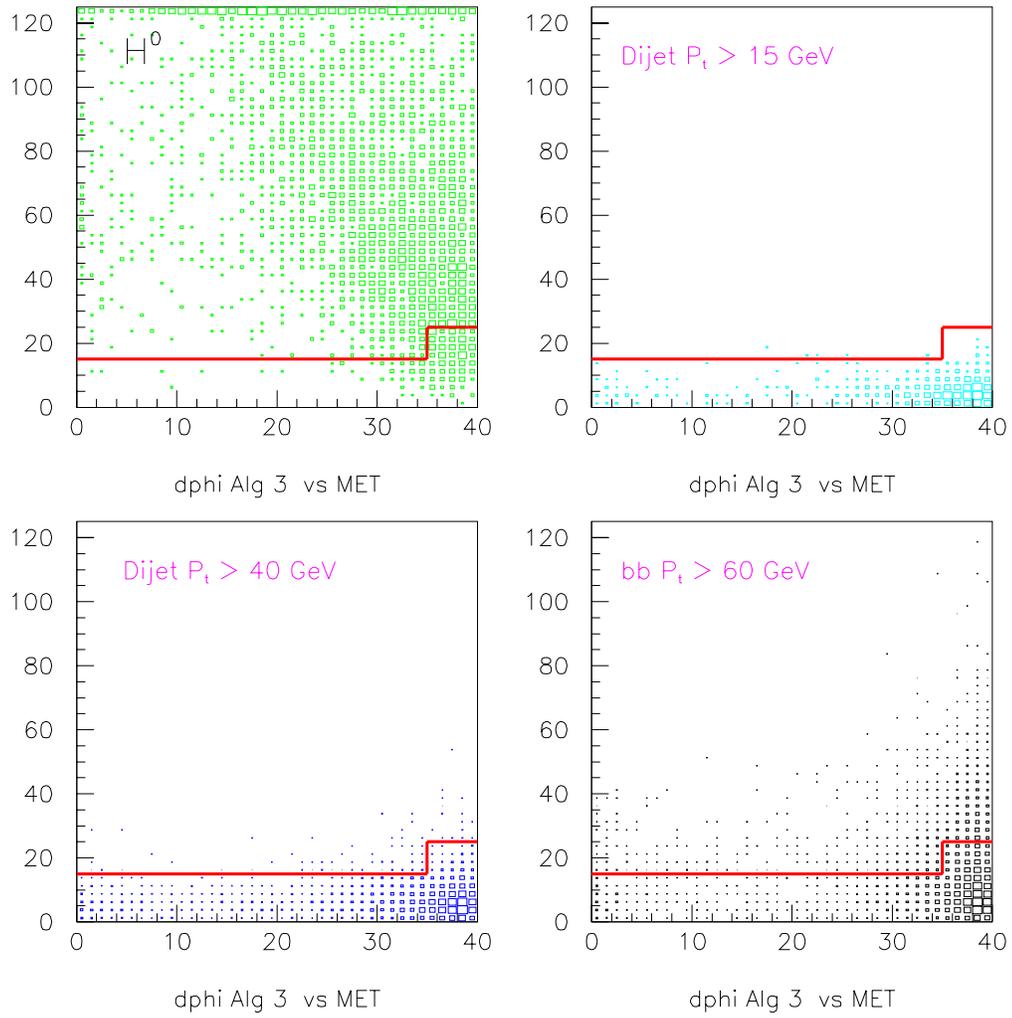


Figure 42. The correlation between delta phi and the missing E_T of the event for signal and representative QCD backgrounds

4.11.3 Rates and rejection improvements

The use of the CFT ϕ correlations becomes compromised at high instantaneous luminosity, as shown in Figure 43. Only for relatively high p_T jets does the correlation remain. At high luminosity one would benefit from the use of the calorimeter to confirm the CFT jets. Modest trigger thresholds are able to reduce the rate from low p_T scatters.

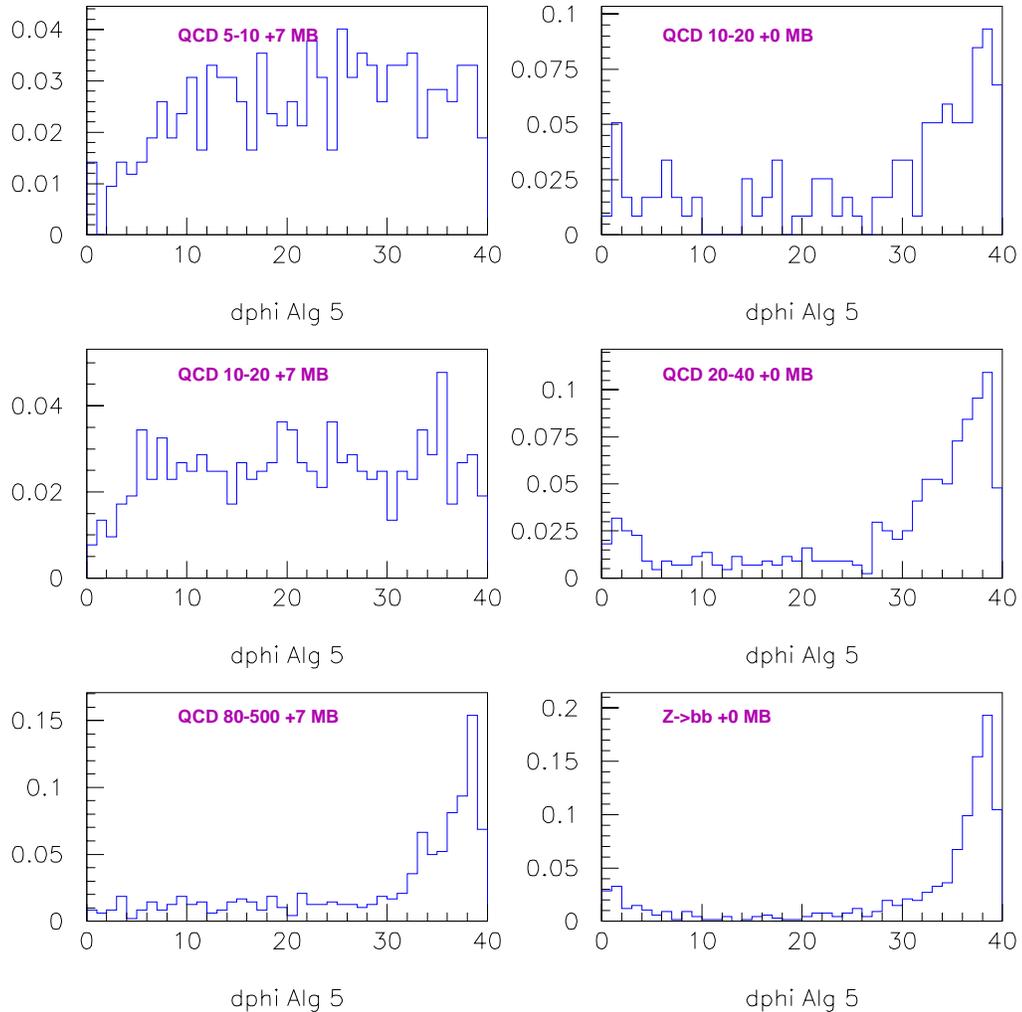


Figure 43. Correlation of $\Delta\phi$ in high luminosity conditions (left hand plots with 7 minimum bias events) and low luminosity conditions (right hand plots with zero additional minimum bias events).

With an improved Level 1 calorimeter trigger that allows correlating CFT and calorimeter based jets these backgrounds can be further suppressed.

4.11.4 Comments

Substantial gain in trigger efficiency for channels such as $Z(\nu\bar{\nu})H$ through imposing cuts on topological correlations between jets. The calorimeter correlations are important extensions of the existing CFT correlations at high luminosity. These calorimeter correlations should be straightforward in the implementation described below using FPGA's in the upgrade calorimeter detector.

4.12 L1 Calorimeter Trigger Implementation

The physics imperatives that drive the need to build a new L1 calorimeter trigger raise a number of implementation issues that will need to be resolved before construction can begin. In this section we discuss the issues that have been raised to date regarding implementation choices that need to be made. Among the important considerations and constraints are ways to minimize the disturbance to the running system as the new system is integrated into the experiment and commissioned.

4.12.1 Constraints

Because the L1 calorimeter system needs to be integrated into the existing DØ DAQ system it needs to obey the following constraints.

4.12.1.1 Existing interfaces

The interfaces of the new system to the existing hardware should be compatible. In particular the new system must interface to the input pickoff signals, the L1 framework, the L2 and L3 data, the clock, and the timing and control systems. Depending on the physics requirements, some of the interfaces may be changed because the existing systems will be modified. An example of this is the possibility that the present differential trigger sum driver signals from the calorimeter will be further subdivided to provide finer granularity EM towers. The change would mean that the present differential coax signals would be used as single ended coax cables (thereby doubling the granularity from 0.2×0.2 to 0.1×0.2 in $\phi \times \eta$)

4.12.1.2 L1 Latency

The L1 latency is $4.2 \mu\text{sec}$. The new system should be compatible with this value. So, the maximum time remaining for complete signal processing which includes digitization, filtering and the processing of the cluster algorithms is less than $2.7 \mu\text{sec}$ after accounting for all the transit times and front end processing. While we do not believe that this should be a concern using modern FADCs and FPGAs, the execution of the cluster algorithms should be optimized in order to be as efficient as possible.

4.12.1.3 Adiabatic integration

The installation and integration of the new system should be designed and built in such a way as to minimize the effect on the data taking. For example, in the absence of a long shut down between Run 2a and b, we are considering the

use of single ended signals from the trigger pickoff as a means to split off the signals for parasitic running – the full implications of such a choice are not yet understood, but are under study. In addition, a testing phase of a part of the trigger with real data would be a great help to debug and validate the algorithms and associated monitoring.

4.12.2 L1 Calorimeter trigger hardware conceptual design

A block diagram of the new L1 calorimeter trigger system is shown in Figure 44. The main change would be to remove the present ADC and logic cards located in 13 racks and to replace them by a 2 to 3 racks of new electronics that will perform the Analog to Digital Conversion, (ADC) the digital filtering (FIR) and the cluster algorithm processing (TAP) for jets and electrons. An output to track matching logic is also foreseen. The functionality of the main functional blocks are discussed in the following sections.

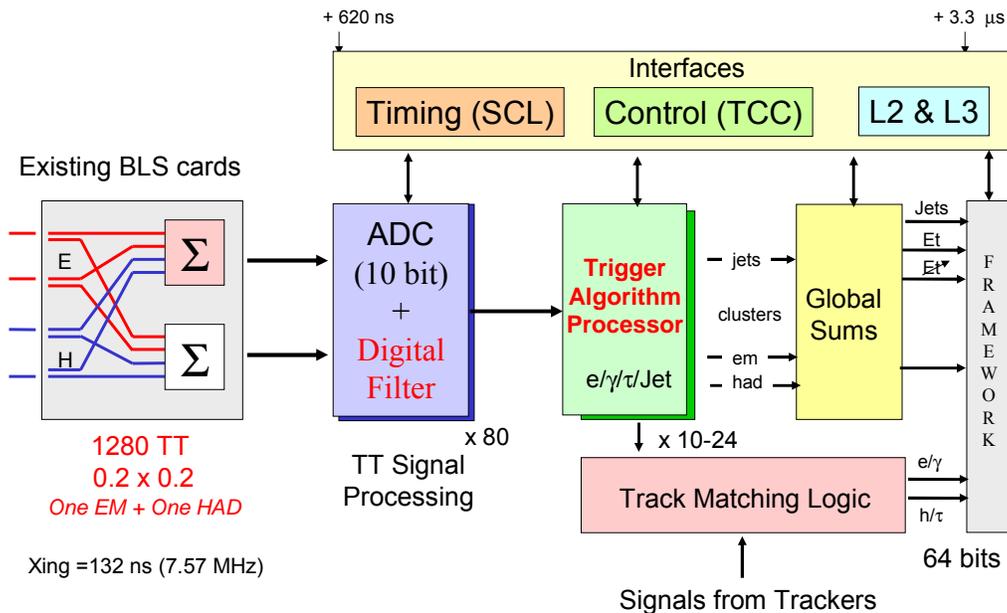


Figure 44. Block diagram of L1 calorimeter trigger, with the baseline subtractor (BLS) cards shown at left.

4.12.3 ADC/TAP Split

In the previous sections we have discussed the various functions that are needed for the L1 calorimeter trigger. One natural split in the system could occur between the ADC section that handles analog signals and a TAP (Trigger Algorithm Processor) section that is a purely digital processor. These two sections would then be linked by LVDS connections. The location of the digital filter leaves us with two options that we consider below.

4.12.3.1 Option 1: “Dumb” ADC

In this option, the ADC section would contain only the analog to digital converter, and no digital filter. The reason to consider this is that the TAP should have enough processing power to perform both the digital filtering and the physics algorithms. The ADC part would produce output samples with 10 bit accuracy. The expected advantages are that in this case the ADC would not need slow controls. Thus it is viewed as inexpensive, simple and very easy (that is to say relatively fast) to implement. However the disadvantage is that this implementation would likely be incompatible with a sampling rate that is faster than the beam crossing rate, because of output bandwidth required to transport all the signals from the ADC to the TAP.

4.12.3.2 Option 2: Filter in the ADC

For this option we place the digital filtering on the in the ADC section. The advantages of this option are:

- The output of the ADC can be limited to 8 bits words. Thereby reducing the link bandwidth to the TAP by 20%.
- There are several towers (at the boundary between central and end caps) that need special handling. While this special treatment is required regardless of the design, it would allow at least the TAP card to use a single uniform design (thus reducing design time).
- The data at the output of the ADC is transferred to the Level 2 trigger and the read-out. Applying the filtering in the ADC section would eliminate the need to repeat the filtering calculation in level 2 and in the off-line processing.

It is also possible that given the somewhat complex designs of the digital filter and the trigger algorithm sections, having these functions physically separated would lead to more expeditious development and testing, particularly if these two sections were developed and built by different collaborators. Although such a division would impose a further management burden on the project in order to preserve excellent communications between groups.

4.12.4 Granularity

The current granularity of the trigger towers is 0.2×0.2 in $\phi \times \eta$. It is possible with a replacement of the trigger sum driver hybrid in the BLS to provide a granularity of 0.1×0.2 in $\phi \times \eta$ in while preserving the current cable plant. There are two options to this increase of granularity:

1. Increasing the trigger granularity of only the EM towers to 0.1×0.2 and leaving the hadronic towers at their present granularity of 0.2×0.2 (which we refer to as mixed granularity)
2. Increasing the segmentation of both the EM and Hadronic towers to 0.1×0.2 .

The additional complexity associated with finer trigger tower segmentation would likely increase the numbers of additional ADC cards by a factor of 1.5 to 2 for options 1 and 2 respectively (compared to leaving the segmentation at the present value). Similarly, the number of TAP's would increase by a factor of 2 to 4 for options 1 and 2 respectively. The increased costs would be a substantial part of the total cost.

The mixed granularity solution has a particular difficulty. The 0.2x0.2 region of interest consists of two adjacent TTs. This region of interest may have two different positions relative to the hadronic towers behind it. It is either exactly on top of one hadronic tower or partially above two hadronic towers. The threshold for the cuts on hadronic fraction or isolation should clearly be different for the two cases. In order to implement those different thresholds we would need additional hardware, and that in turn may end up lessening the effectiveness of the cuts.

4.12.5 Overlap

The amount of data produced by the ADC cards is too large to be processed by a single TAP. The volume of data would be about 20 Gbytes/s (for 0.2 x 0.2 and twice that for 0.1x0.2). Therefore the digital processing must be done by tens of TAP cards, each one processing the data corresponding to a rectangular area of the calorimeter. The number and speed of the LVDS links supplying data to one TAP card determine the number of TAP cards needed. Each DFE card is responsible for the recognition of electrons and jets in its section of the calorimeter.

It is necessary for the data to be shared across neighboring TAP cards in order to implement the algorithms. The amount of sharing depends on the details of the algorithms; the jet algorithm is the most demanding (because jets are larger than electrons). In order to have a reasonable system size, the overlap must be kept to a maximum of two cells in all. This limits the choice of the jet algorithm. The first limitation comes from the need to avoid double counting: the same jet should not be found in two adjacent TAPs. The second requirement is to avoid splitting a single jet at the boundary of two TAPs. Both limitations can be addressed in the subsequent processing stage, but we would to avoid that if possible. That leads to two options for the overlap:

- 2 TT overlap in all directions: This allows for jet algorithms up to 1.0x1.0. It is also needed in the 0.8x0.8 algorithm if one requests separated jets. This symmetrical arrangement makes the cabling easier.
- Alternating 2 TT and 1 TT: This is the minimum for the 0.8x0.8 algorithm. This reduces the bandwidth between the ADC and the TAP by 8%.

4.12.6 TAP implementation

Since the detailed designs for the L1 calorimeter trigger system do not yet exist, we have explored two possible options for the TAP card implementation. In the first case we consider reusing existing designs of processor cards from other DØ systems. In the second case we imagine a completely new design.

4.12.6.1 Option 1: Reuse existing designs

We have considered the possibility of reusing the tracking electronics (CTT) digital front end cards (DFE) to perform the trigger processing functions of the TAP. Initial studies on the logical mapping of the DFEs to calorimeter sectors, the physical cabling and the required capacity of the links show that such an option appears viable. More detailed studies are needed before a firm conclusion could be drawn on the ultimate viability of this option, especially concerning the implementation of trigger algorithms in FPGAs. We estimate that this solution would roughly divide by two the design effort required, leading to several months of savings in manpower.

If this solution is adopted, then the digital filter must be implemented on the ADC cards because of:

- The link capacity. Carrying 10 bit samples over DFE links requires 25% more bandwidth than dealing with 8 bit E_T calibrated samples.
- The available processing power. Incorporating a series of digital filters and the trigger algorithm logic may not fit in the FPGA of DFEs.
- The existing slow controls system. The limitation of bandwidth for slow controls on the DFEs could make the loading and update of filter coefficients unacceptably slow.

Although the potential savings in manpower and the reduction of further complex boards that will need to be maintained are attractive, there are, however, a number of concerns for a DFE based solution. They include:

- The possible unavailability of some components of the DFE, especially connectors on the motherboard. It may not be possible to build a sufficient number of DFEs and spare cards from presently available parts.
- FPGAs on the daughter card of a DFE are mature devices and may not be cost-effective when Run 2b starts. Although a new daughter card with a more modern FPGA could be designed, the fact that the serial to parallel conversion for the input links is implemented on the motherboard of a DFE places a tight upper limit on link speeds and imposes a worrisome constraints on FPGA pin counts, printed circuit board design, etc.
- The bandwidth of DFE links which is marginally acceptable, even if these links could be clocked at 61 MHz instead of the current 53 MHz. This limitation could exclude the possibility to run algorithms that operate on a 1.0×1.0 window in $\phi \times \eta$ space, though using 0.8×0.8 windows would probably fit.
- There are no serial command link (SCL) links in the DFE system (the SCL is a high speed serial bus that links front end systems with the trigger framework). The SCL link must thus be implemented in the ADC sub-system. This will obviously complicate the design of the

ADC cards, offsetting the expected savings in manpower on the DFE side.

- Because DFEs do not receive timing information and are purely data driven, the necessary timing signals must be embedded in the dataflow by the ADC cards. This places additional constraints on the ADC cards and consumes a small fraction of the (precious) link bandwidth.
- The logic capacity of the FPGA in the current DFE may not be sufficient. This point has not been studied yet. The FPGA manufacturer does not foresee much (>2) larger devices because it has switched to a new footprint, which could introduce a maintenance and/or procurement problem.
- The bandwidth of the slow control is insufficient to keep all the functionalities of the current trigger software.
- The present DFE design is not as robust as one would like because of some rather delicate front panel connectors.

4.12.6.2 Option 2: New TAP design

While the possibility of reusing existing designs is attractive, it may not prove possible. Thus we have considered a completely new design for the trigger logic processors (the TAP cards) which allows for superior performance because the compromises imposed by using an already existing design can be avoided (at the cost of design manpower of course). In this study of a new, dedicated TAP module the following guidelines were proposed:

- Use faster LVDS links. This is obtained by feeding the links directly into the FPGA, bypassing the (relatively) slow serializer/deserializer used in the CTT DFE.
- Use SCL data from the back plane for synchronization.
- Use a modern serial bus (such as USB2) for slow control.
- Use 12 input links and 6 output links.
- Use the latest generation FPGA. Use smaller footprint FPGAs because of the reduced number of IO pins obtained by serial IO instead of parallel.
- Place all IO cables at the rear of the module.

Additional compatibility issues could also be addressed in this new design specification, to conserve the current CTT DFE environment:

- Use the same LVDS cables.
- Accept the slow control of the DFE crate as an alternate to the normal one.

- Use software compatible FPGAs.
- Such a design would provide ample improvement margin for possible CTT upgrades.

4.12.7 Milestones and cost estimate

Since a detailed design has not yet been made, the details of the schedule, resources and cost estimate are necessarily sketchy. They will require more work to develop a fully resource loaded schedule. However given the extreme time pressures that are imposed on any Run 2b upgrades, we have made an attempt to understand the dates for some major project milestones, as shown in Table 27.

Table 27. Major milestones for L1 calorimeter trigger project.

Milestone date	Task
03/02	Performance specification defined, major design choices made
08/02	Prototype design complete
12/02	Prototyping complete (ADC, TAP,...)
06/03	Prototype testing complete
09/03	Preproduction complete
12/03	Preproduction testing complete
06/04	Production complete, testing begins
07/04	Installation & commissioning starts
01/05	Commissioning complete

4.12.8 Cost estimate

A preliminary cost estimate for the Level 1 calorimeter trigger upgrade is presented in Table 28 below. Manpower is not included. Most of these M&S funds will be needed in FY03 and FY04.

As described in the above sections, much progress has been made in defining the technical approach that the Level 1 calorimeter trigger upgrade is expected to pursue. Nevertheless, there are a number of outstanding issues that remain: among them, for example, is the final trigger tower granularity that is adopted, which introduces a factor of two uncertainty in the number of boards that would have to be fabricated. (The boards for both the ADC/digital filtering system and the digital processing system will be the M&S cost driver for this project.) In an effort to accommodate this broad option in project scope, as well as other sources of uncertainty at this early stage in the design, we include a contingency of 100%. The base cost for most of the items below has been estimated from previous projects in Run 2a that required similar boards, power supplies, backplanes, and other elements.

We note that this cost estimate does not include any funds for possible track to calorimeter cluster matching.

Table 28. Preliminary cost estimate for the Level 1 calorimeter trigger only. A contingency of 100% has been applied. Manpower is not included, and track-calorimeter matching hardware is not included.

Item/process	Unit Cost (\$)	# Required	Total Cost (\$k)	Total Cost + 100% Contingency (\$k)
ADC/digital filter system				
ADC/filter cards	3500	105	368	
Crates & power supplies	7100	8	57	
Controller cards	2000	8	16	
VME masters	2300	10	23	
<i>Subtotal</i>			<i>464</i>	<i>928</i>
Digital Trigger Algorithm System				
Trigger algorithm cards	7500	30	225	
Crates & power supplies	3000	3	9	
Controller cards	500	4	2	
<i>Subtotal</i>			<i>236</i>	<i>472</i>
LVDS cables	75	350	26	52
TOTAL			\$726	\$1,452

4.13 L1 Calorimeter Summary & Conclusions

The high luminosity of Run 2b presents a significant challenge to the L1 calorimeter trigger. The L1 calorimeter trigger upgrade proposed in this section addresses these challenges.

We will need to be able to effectively deal with pileup in the trigger pickoff signal from nearby bunch crossings – this is addressed by digital filtering techniques. Since almost 80% of the L1 rate is calorimeter based, the importance of sharpening the p_T cut (and thus reducing background rates) as well as the possibility of triggering on real objects such electromagnetic clusters and jets is clear, and being addressed by a “sliding window” technique. The hardware implementation of this technique has been explored, leading to a preliminary understanding of the system scope and costs.

The system can also be expanded with the addition of track-calorimeter cluster matching hardware (which has not been costed). Our studies indicate that we can achieve considerable rate reductions for calorimeter triggers and also for tracking triggers. The effect of a doubling of the ϕ segmentation (which is achievable) was evaluated for the track matching and could lead to further rate

reductions by factors of two to three, although further study of this somewhat costly addition is required. The benefit of finer segmentation for electron energy clustering is apparently marginal.

The improvement in global variables such as missing E_T can also be improved with the addition of the energy from the ICR region at L1. The ability to do that has been provided in the present front-end electronics.

Finally, the additional power provided by current FPGA's will allow the migration to L1 of more sophisticated algorithms and topological cuts presently available at L2.

This set of tools provided by the proposed L1 calorimeter trigger will allow us to make the optimal use of the Run 2b luminosity.

5 L1 Muon Trigger

5.1 Goals

The primary goal of the L1 Muon Trigger (L1MU) system for Run2b of the DØ experiment is to provide an unprescaled high P_T ($P_T > 10$ GeV/c) single muon trigger with a rate of 1-2 kHz. Other L1 physics triggers may combine the L1 muon trigger with other L1 object triggers such as jets or electrons. Some physics triggers may utilize lower P_T threshold L1 muon triggers combined with other L1 object triggers. The L1 trigger rates of these other triggers will either be lower than the single muon trigger or prescaled because of their lower physics priority. For purposes of this document, the high P_T single muon trigger seems the best benchmark. In Run 2a, an additional goal is to provide an unprescaled 1-2 kHz low P_T dimuon trigger ($P_T > 1.5$ GeV/c). That goal is not presently extended to Run 2b.

5.2 Description of the Current L1 Muon Trigger

5.2.1 Overview

Information on the Run 2a L1MU trigger hardware including the technical design report can be found at <http://hound.physics.arizona.edu/l1mu/l1mu.htm>. Only a brief summary is provided here.

The muon detectors are organized into three regions corresponding to the solid iron toroids CF (central), EFN (north end), and EFS (south end). The detectors in the CF region are the A-phi scintillation counters just outside the central calorimeter. These are followed by the four-cell A-layer proportional drift chambers (PDTs), the magnetized iron, two separated three-cell PDT B and C layers, and finally, a plane of 'Cosmic cap' scintillation counters. A similar pattern is followed for the EF regions, with A-layer planes of pixel scintillation counters and multicell drift chambers (MDTs) followed by the magnetized toroids and separated B and C layer pixel counters and MDTs. Both PDTs and MDTs provide local track vectors for trigger purposes. The various scintillator elements give good timing and moderate granularity space points.

The L1MU trigger identifies muon candidates by using combinatorial logic that makes use of tracks from the L1 Central Fiber Tracker (L1CFT) trigger⁸ **and** hits from **all** muon detector elements. The muon detector elements include both drift chambers and scintillation counters.

A block diagram of the L1MU Trigger is shown in Figure 45. There are three custom VME crates of L1MU Trigger Cards (MTCxx's) corresponding to the central (CF), north (EFN), and south (EFS) geographic regions of the DØ detector. There is one custom VME crate that serves as a Muon Trigger Manager (MTM). There are also four custom VME crates of Muon Centroid Finder (MCEN) cards and one custom VME crate of Muon Concentrator (MCON)

⁸ The six highest- p_T tracks in each CFT trigger sector are sent from the first layer of track-finding trigger electronics before combination and collation by L1CTT.

cards. All VME crates reside on the detector platform and are thus inaccessible during data taking.

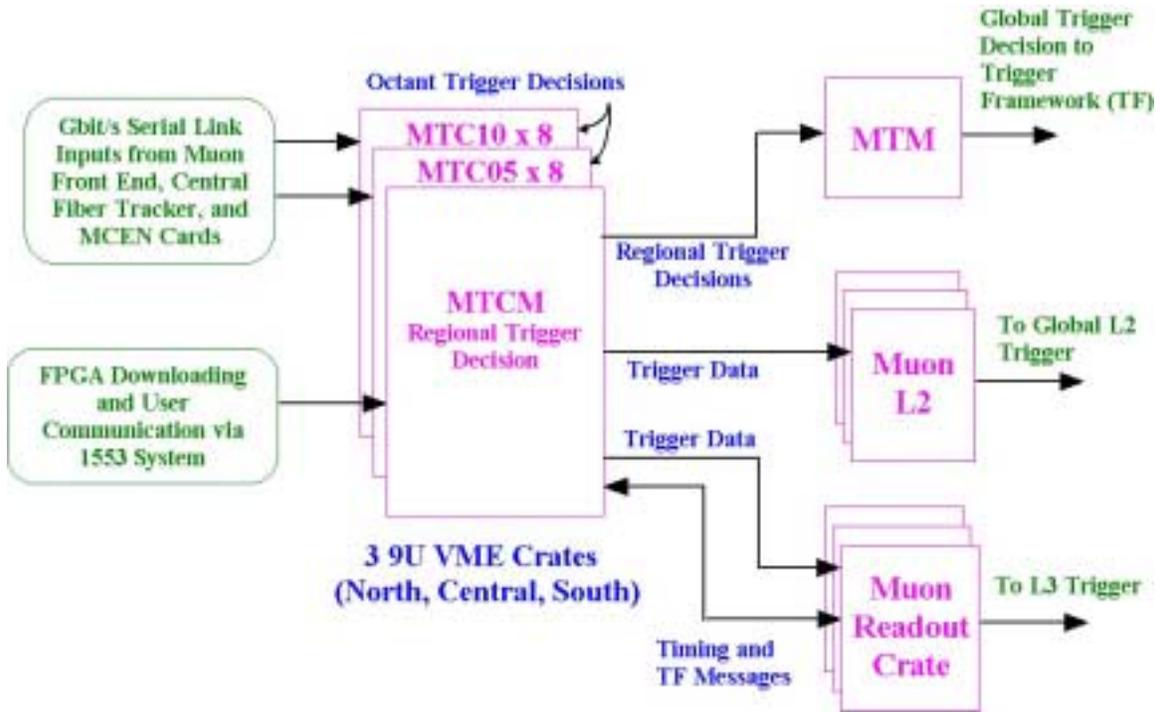


Figure 45. Block diagram of the L1MU trigger system.

Within each L1MU crate there are eight muon trigger “05” cards (MTC05 cards) and eight corresponding muon trigger “10” cards (MTC10 cards). Each geographic region is divided into octants and each MTC05 and MTC10 card makes local trigger decisions for one octant. The names “05” and “10” do not represent different levels of triggering but rather distinguish between those trigger decisions made primarily using L1CFT tracks combined with muon scintillator hits and those made primarily with muon wire chamber hits combined with muon scintillator hits. The muon trigger uses both “05” and “10” trigger decisions in a flexible, user-defined manner to determine whether a good L1 muon trigger has occurred.

A Muon Trigger Crate Manager (MTCM) card for each region collects the MTC05 and MTC10 trigger decisions for each octant to form several regional trigger decisions. These regional trigger decisions are collected by a Muon Trigger Manager (MTM) card that forms the 32 user-defined global L1MU trigger decisions sent to the trigger framework.

5.2.2 Central Muon Trigger Algorithm (CF MTC05)

For the central (CF) MTC05 cards, tracks from the L1CFT Trigger are received on twelve cables with up to six tracks per cable. Ten of the cables are from L1CFT Trigger sectors corresponding to a muon detector octant plus one

each from a sector in adjacent octants. Tracks from different cables are processed in parallel.

Each L1CFT Trigger track is currently described by its position in the outer layer of the CFT and its signed offset in the inner layer with respect to an infinite momentum track passing through the position in the outer layer of the CFT. This information can be used to determine the signed p_T of the L1CFT track. Currently only four groups of such inner layer offsets are possible corresponding to four P_T thresholds of 1.5, 3, 5, and 10 GeV/c. We (L1MU) call these thresholds PT1 to PT4 respectively. Tracks from the twelve cables are input simultaneously with subsequent tracks following every 18.8 ns. In the MTC05 FPGA logic, the p_T 's of the tracks are decoded and the outer layer positions are used to form "wedges" of CFT tracks that will be matched to ϕ slices defined by the A-layer A-Phi counters.

Scintillator hit information from the A-Phi and Cosmic Cap scintillator counters is carried by the four remaining cables. Combinatorial logic is then used to find η and ϕ correlations in AC and AB scintillation counter hits. (Note the present B-layer scintillator coverage is modest and only fills in C-layer gaps.) A valid muon trigger is denoted by the corresponding ϕ slice of the A-layer A-Phi counter. The trigger conditions (correlations) are found separately for each of the four P_T thresholds. Finally, the L1CFT wedges are matched to the ϕ slices of the A-Phi triggers to form the CF MTC05 triggers. The results are output in two-bit counters that give the number (A # B # C) scintillation counters and (AC # AB) correlated counter patterns that have been matched to L1CFT wedges. There are separate two-bit counters for each p_T threshold. These counters are subsequently sent to the MTCM card for use in forming the central regional trigger decision.

5.2.3 Central Muon Trigger Algorithm (CF MTC10)

For the central (CF) MTC10 logic three layers of proportional drift tube (PDT) **hits** are received on thirteen input cables. The hits in each layer are used to find centroids (track stubs) in each layer using combinatorial logic. Scintillator hit information from the A-Phi and Cosmic Cap counters are input on the remaining three cables. The scintillator hit information is used to confirm that the PDT centroids came from this specific crossing. This step is necessary because the maximum drift time of the PDT's spans four or five 132 ns bunch crossings.

Next, using only scintillator-confirmed centroids, combinatorial logic is used to find good trigger conditions that are defined by correlations between centroids in different layers. The results are output in two-bit counters which give the number of (A # B # C) centroids and (AB # AC) correlated centroid patterns. (BC patterns could also be used if needed.) These counters are subsequently sent to the MTCM card for use in forming the central regional trigger decision.

5.2.4 Forward Muon Trigger Algorithms (EF MTC05)

For the forward (EF) MTC05 cards, tracks from the L1CFT Trigger are received on twelve cables with up to six tracks per cable. Ten of the cables are

from L1CFT Trigger sectors corresponding to a muon detector octant plus one each from a sector in adjacent octants. Tracks from different cables are processed in parallel.

Each L1CFT Trigger track is currently described by its position in the outer layer of the CFT and its signed offset in the inner layer with respect to an infinite momentum track passing through the position in the outer layer of the CFT. This information can be used to determine the signed p_T of the L1CFT track. Currently only four groups of such inner layer offsets are possible corresponding to four P_T thresholds of 2, 4, 7, and 11 GeV/c. We (L1MU) call these thresholds PT1 to PT4 respectively. Tracks from the twelve cables are input simultaneously with subsequent tracks following every 18.8 ns. In the MTC05 FPGA logic, the p_T 's of the tracks are decoded and the outer layer positions are used to form "wedges" of CFT tracks that will be matched to ϕ slices defined by the A-layer Pixel counters.

Scintillator hit information from the A-, B-, and C-layer scintillator pixel counters is carried by the four remaining cables. Combinatorial logic is then used to find a good muon "track" defined by η and ϕ correlations in the AB and AC-layer Pixel counter hits. (BC-layer combinations could be used if needed.) A valid L1MU trigger is described by the corresponding ϕ slice of the A-layer Pixel counter. The trigger conditions (correlations) are found separately for each of the four P_T thresholds. Finally, the L1CFT wedges are matched to the ϕ slices defined by the A-layer Pixel triggers to form the EF MTC05 triggers. The results are output in two-bit counters which give the number of (A # B) Pixels and (AB # AC) correlated Pixel patterns that have been matched to L1CFT wedges. There are separate counters for each P_T threshold. These counters are subsequently sent to the MTCM card for use in forming the forward regional trigger decision.

5.2.5 Forward Muon Trigger Algorithms (EF MTC10)

For the forward (EF) MTC10 logic three layers of mini-drift tube (MDT) **centroids** are received on twelve input cables. The MCEN cards use MDT hits to first find the MDT centroids. Scintillator hit information from the A-, B-, and C-layer Pixel counters input on the remaining four cables. The scintillator hit information is used to confirm the MDT centroids.

Next, using only scintillator-confirmed centroids, combinatorial logic is used to find good trigger conditions that are defined as correlations between centroids in different layers. The results are output in two-bit counters which give the number (A # B) centroids and (AB # AC) correlated centroid patterns. These two-bit counters are subsequently sent to the MTCM card for use in forming the forward regional trigger decision.

5.3 Performance of the Current Muon Detector

Only one relevant aspect is reported here. The occupancies of the Pixel counters in the A, B, and C-layer per minimum bias event per octant are 3%, 0.7%, and 1.4% respectively. The occupancies of the MDT chambers in the A, B, and C-layers per minimum bias event per octant per number of planes (decks)

are 2.3%, 0.6%, and 1.3 % respectively. These numbers are quite low and in agreement with our expectations based on old Monte Carlo simulation. We need to re-check these numbers with current Monte Carlo samples. We must also study the occupancy as a function of luminosity. However, we feel that the substantial beamline shielding installed for Run 2a appears to be doing its job.

5.4 Performance of the Current L1Muon Trigger

Some elements of the L1MU trigger have been operational since the start of Run 2a. Other elements are not yet operational. Presently, the L1MU trigger consists of two-layer scintillator coincidences in the central and forward muon detector regions. The two-layer requirement imposes a $\sim 3\text{-}4$ GeV/c momentum threshold on the muons. Single muon triggers using reasonably tight "roads" are operational in both regions. Dimuon triggers are operational in both regions as well. Muon plus jet triggers are defined in the central muon detector region only as no calorimeter triggers currently exist in the calorimeter EC region. Trigger rates for existing L1MU triggers at $L=5 \times 10^{30}$ /cm²/s are given in Table 29.

Table 29. Trigger rates for existing L1MU triggers at $L=5 \times 10^{30}$ /cm²/s.

Trigger	Description	Rate (Hz)
mu1cmisc_fz	Single muon trigger -central region	135
mu2cmisc_fz	Dimuon muon trigger -central region	2
mu1pix_fz	Single muon trigger - north or south region	76
mu2pix_fz	Dimuon trigger - north or south region	<1
mu1cmisc_j5_fz	Single muon + jet trigger - central region	<1
mu1cmisc_j10_fz	Single muon + jet trigger - central region	<1

Elements currently missing from the L1MU trigger are the MTC10 triggers using the PDT's and MDT's and the MTC05 triggers using the L1CFT trigger. The MTC10 triggers using PDT's exist but problems with PDT front-end board timing have prevented us from fully commissioning this trigger. MTC10 triggers from the MDT's await the installation of the MCEN system that finds MDT centroids. The MCEN system is being installed during the October 2001 accelerator shutdown. Information from the L1CFT trigger awaits installation of the L1CFT and other CFT electronics. The L1CFT and other CFT electronics will also be installed during the October 2001 accelerator shutdown.

Data analysis of the purity and efficiency of L1MU triggers is just beginning. Using the d0ve event display we find that approximately 20% of the L1MU triggers in the forward region have good tracks by eye. Good here is defined as three layers of pixel scintillation counters and three layers of MDT track stubs. (Recall the L1MU trigger just requires two layers of pixel counters.) An analysis using reconstructed muon tracks (with muon detector elements only) gives a somewhat smaller number but also includes unknown reconstruction efficiency.

Results on the purity of the L1MU trigger in the central region are poorer and studies are underway to understand this.

5.5 Estimating the Run 2b Performance of the L1 Muon Trigger

We are presently missing **the** key element of the L1MU trigger, namely the L1CFT trigger. Hence estimating the Run 2b performance of the L1MU trigger is very difficult. We have three pieces of information: current data rates, L1MU simulator rates performed 1997, and current L1MU simulator rates.

Figure 46 and Figure 47 show the measured single muon L1MU Trigger rates in the central and forward regions. As described above, these triggers do not include the L1CFT or the PDT and MDT triggers. The fast z (minimum bias) requirement is presently part of the trigger definition. The central region data use an 88ns (wide) timing window for good scintillator hits on the scintillator front-end cards. The forward region data use a 40ns (narrow) timing window for good scintillator hits.

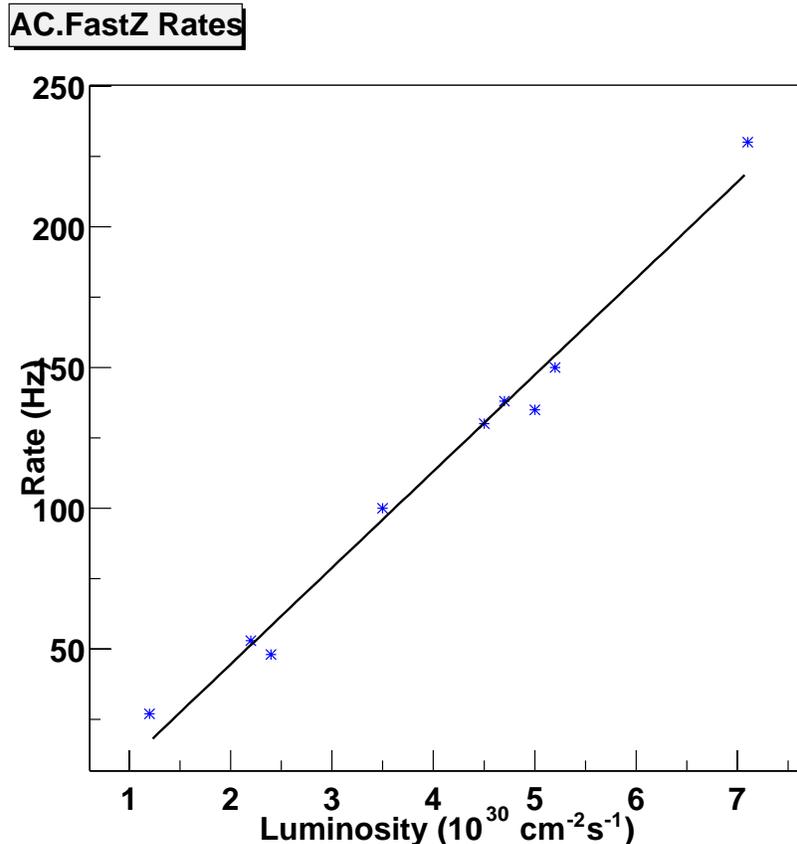


Figure 46. Measured single muon L1MU trigger rate in the central region.

Table 30 contains measured rates for $L = 2 \times 10^{30} / \text{cm}^2 / \text{s}$ and estimated rates for 2×10^{32} and $5 \times 10^{32} / \text{cm}^2 / \text{s}$.

AB Rates

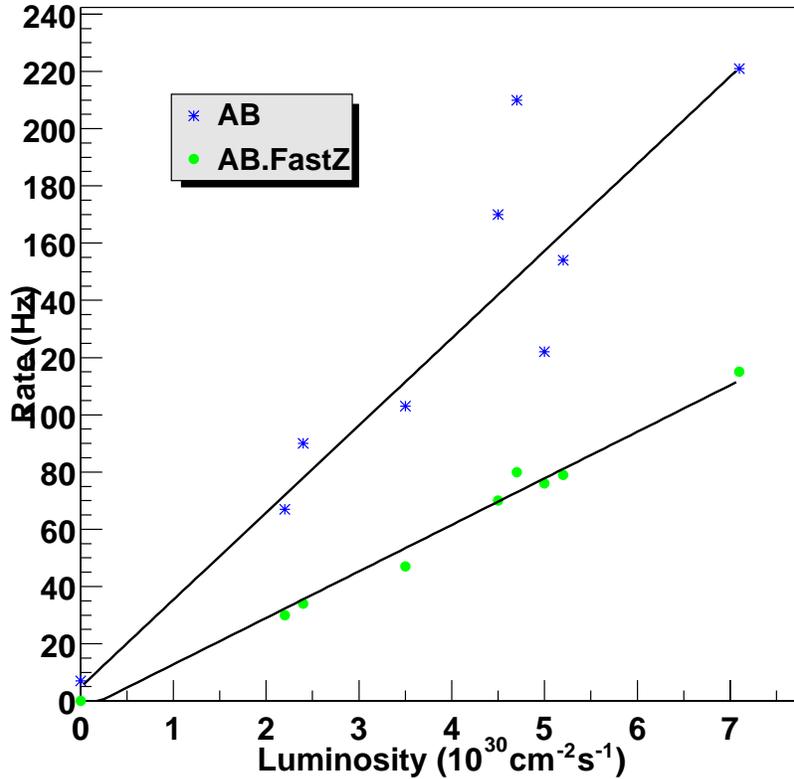


Figure 47. Measured single muon L1MU trigger rate in the forward region.

Table 30. Measured rates for $L = 2 \times 10^{30} / \text{cm}^2 / \text{s}$ and estimated rates for 2×10^{32} and $5 \times 10^{32} / \text{cm}^2 / \text{s}$.

Trigger	Measured Rate (Hz) at $L = 2 \times 10^{30} / \text{cm}^2 / \text{s}$	Estimated Rate (Hz) at $L = 2 \times 10^{32} / \text{cm}^2 / \text{s}$	Estimated Rate (Hz) at $L = 5 \times 10^{32} / \text{cm}^2 / \text{s}$
Single muon - central region	40	6800	17000
Single muon - forward region	30	3000	7500

Tightening the timing window from 88 to 40 ns for good hits on the scintillator front-end cards reduces the rates by roughly a factor of 2. This was recently implemented in the forward region scintillator front-end cards and is included in the forward region rate estimates above. On the other hand, removing the fast z (minimum bias) requirement increases the rates by roughly the same factor. (Since we don't know the efficiency of the fast z requirement for muons it might be removed at some later date.)

These rates are encouraging. We have yet to include the PDT and MDT L1MU triggers. We have yet to include the L1CFT tracks. The timing window for good hits on the scintillator front-end cards might possibly be narrowed even further. Assuming the L1MU triggers can take ~2kHz of the ~6kHz L1 trigger

bandwidth at the highest luminosity, a reduction of $\sim x7$ is needed which we believe possible with the above mentioned elements.

On the other hand, these numbers can be used to estimate the L1MU trigger rates if the L1CFT fails to provide any rejection at high luminosity. Achieving the $x5$ reduction with the PDT and MDT triggers alone is probably difficult but factors of $x2-3$ may not be.

A Fortran-based L1MU trigger simulator was used in 1996-1997 to help design the L1MU trigger algorithms. A selection of rates from that era is given in Table 31.

Table 31. Selection of rates from the Fortran-based L1MU trigger simulator.

Trigger	Description	Rate (Hz) for QCD + 1 Min Bias	Rate (Hz) for QCD + 4 Min Bias	Rate (Hz) for QCD + 6 Min Bias
L1CFT only – PT4	L1CFT only for $P_T > 11$ GeV/c	3395	51364	440929
L1MU(1,PT1, Loose, Central)	L1CFT & One-Layer Scintillator, $P_T > 2$ GeV/c, $ \eta < 1.0$	13546	96365	117114
L1MU(1,PT4, Loose, Central)	L1CFT & One-Layer Scintillator, $P_T > 11$ GeV/c, $ \eta < 1.0$	92	617	81
A-layer PDT	PDT A centroid only	65356	278012	364892
AB & AC-layer PDT	MTC10	950	5632	9636
L1MU(1,PT1, Loose, Forward)	L1CFT & One-Layer Scintillator, $P_T > 2$ GeV/c, $1.0 < \eta < 2.0$	30123 x 2	148251 x 2	252096 x 2
L1MU(1,PT4, Loose, Forward)	L1CFT & One-Layer Scintillator, $P_T > 11$ GeV/c, $1.0 < \eta < 2.0$	13 x 2	4 x 2	4 x 2
A-layer MDT	MDT A centroid only	28292 x 2	70509 x 2	124490 x 2
AB-layer MDT	MTC10	26 x 2	24 x 2	75 x 2

A few comments on Table 31:

- The L1CFT trigger with the highest p_T threshold (PT4) has a 1% firing rate with 4 minimum bias interactions and a 10% firing rate with 6 minimum bias interactions.

- The x 2 in Table 31 is given because the rates were estimated for the North region only.
- Note the dramatic fall-off of rates once a muon detector layer outside the toroid iron is included in the trigger. Compare the PDT or MDT triggers for example.
- One of the easiest methods to reduce the L1MU trigger rates is to include muon detectors outside the toroid. However one must be equally concerned about loss of efficiency.

The L1MU Trigger rates of the L1CFT Trigger coupled with muon detector elements appear to be survivable at the highest luminosities. The rates in this case, however, are based on very few background events passing the trigger requirements. The trigger rates could be higher if more Monte Carlo had been available at that time because one event carrying a large weight could significantly increase the estimated rate.

Finally, we also have some relative rate estimates using the current DØ C++ trigger simulator. We do not quote an absolute rate but rather simply compare numbers of events with 0.7 and 5.0 minimum bias events with p_T (hard scatter) > 2 GeV/c. Results are included in Table 32. Note that timing window cuts on the scintillator hits have **not** been applied here. Including them would likely reduce the number of events passing the various trigger conditions. The study to determine this rejection factor in the simulator is in progress.

Table 32. Muon trigger rates estimated using Run 2 trigger simulator.

Trigger	Description	Number Passed per 16k events QCD + 0.7 minimum bias events	Number Passed per 16k events QCD + 5.0 minimum bias events
L1MU(1,PT1, Loose,Central)	L1CFT & One-Layer Scintillator, $P_T > 2 \text{ GeV}/c$, $ \eta < 1.0$	38 (2.3×10^{-3})	958 (5.9×10^{-2})
L1MU(1,PT4, Loose,Central)	L1CFT & One-Layer Scintillator, $P_T > 11 \text{ GeV}/c$, $ \eta < 1.0$	1 (6.2×10^{-5})	113 (7.0×10^{-3})
L1MU(1,PT4, Tight,Central)	L1CFT & Two-layers Scintillator, $P_T > 11 \text{ GeV}/c$, $ \eta < 1.0$	0 (0)	1 (6.2×10^{-5})
L1MU(1,PT4, Loose, Central+Forward)	L1CFT & One-Layer Scintillator, $P_T > 11 \text{ GeV}/c$, $ \eta < 1.5$	1 (6.2×10^{-5})	149 (9.3×10^{-3})
L1MU(1,PT4, Tight, Central+Forward)	L1CFT & Two-Layers Scintillator, $P_T > 11 \text{ GeV}/c$, $ \eta < 1.5$	0 (0)	1 (6.2×10^{-5})

As a crude consistency check, we can compare the trigger rates from the old and new simulators. In the current C++ simulator if one assumes that 16k events corresponds to the maximum trigger rate of 5 MHz, then the trigger rates of L1MU(1,PT1, Loose, Central) and L1MU(1,PT4, Tight, Central) are 12kHz and 300 Hz respectively. These rates compare reasonably well with the corresponding numbers from the older Fortran simulator of 14kHz and 100 Hz.

The points to note from Table 32 are:

- The Loose (L1CFT plus one-layer of scintillator counters) L1MU Trigger rates significantly increase as more minimum bias events are added to the event. Again note however that timing cuts have **not** been applied in this particular analysis.
- The Tight (L1CFT plus two-layers of scintillator counters) L1MU Trigger rates are small even at high luminosities. Again, the iron toroids serve as an effective shield of background of particles coming from the calorimeter and hence keep the L1MU Trigger rate low. There is loss of signal efficiency though as discussed below.

Finally, we do not have a comparison of data versus simulator rates since non-L1CFT triggers were never implemented in the simulator. Work is underway to add the current L1MU triggers used in data-taking to the simulator so that this comparison can be made.

5.6 Run 2b Issues

Given the present lack of an L1CFT trigger in the experiment, it is difficult to argue that the L1MU trigger (which relies heavily on the L1CFT trigger) will not function in Run 2b. On the other hand, it is clear that the muon detector systems themselves are likely to work. The weak spot in the muon triggering scheme will be the CFT, as was described earlier. Better estimates must wait until early in 2002 when the L1CFT trigger is operational. We note that the proposed improvement of the L1CFT using singlet fiber roads discussed in Chapter 3 will probably be necessary for control of Run2b muon rates.

There are several other L1MU issues related to Run 2b. These include PDT aging, central muon detector acceptance, central C-layer scintillator shielding, and the trigger decision time.

Aging of the PDT's in Run 1 was a major problem and a main motivation for replacing the PDT's in the forward region with MDT's. A number of steps were taken to reduce the effect of aging for the PDT's remaining in the central region for Run 2a. The A-layer PDT's are the most susceptible to aging and the most difficult to clean. In their case, the source of aging was removed by replacing the "glasteel" cathode pads with G10. It is expected that the aging of the A-layer PDT's will be greatly reduced although the actual rate from Run 2a collider running is unknown.

Most of the B and C-layer PDT's retain their glasteel pads for Run 2a and aging is a real concern. The absence of the Main Ring will certainly reduce the aging rate. To further minimize the effects of outgassing from the glasteel, the gas flow rate was increased for Run 2a. Nonetheless, the chambers *will* age and require periodic cleaning. Again, the actual aging rate due to Run 2a collider running is not yet known for the B and C-layers. It will be measured by tracking the pad gains. It is reasonable to assume that the B and C-layer PDT's will require cleaning several times during Run 2b. One could contemplate replacing the PDT's with MDT's or replacing the glasteel in the remaining PDT's. Both are large, manpower intensive jobs and the former is likely prohibitively expensive.

Except in the bottom two octants, the acceptance of the A-Phi scintillator is above ~90%. There is some loss of efficiency for $0.8 < |\eta| < 1.0$. The Cosmic Cap efficiency is ~80%. There is more loss in the $0.8 < |\eta| < 1.0$ region. The Tight (two-layer) L1MU Trigger efficiency in the central region is shown in Figure 48. The trigger efficiency in the bottom can be improved to 80% by requiring only a single layer of counters.

Because the L1MU trigger rates drop dramatically when scintillator outside the iron toroid is included, it is important to keep the efficiency of the B- and C-layer scintillator high (see Figure 49).

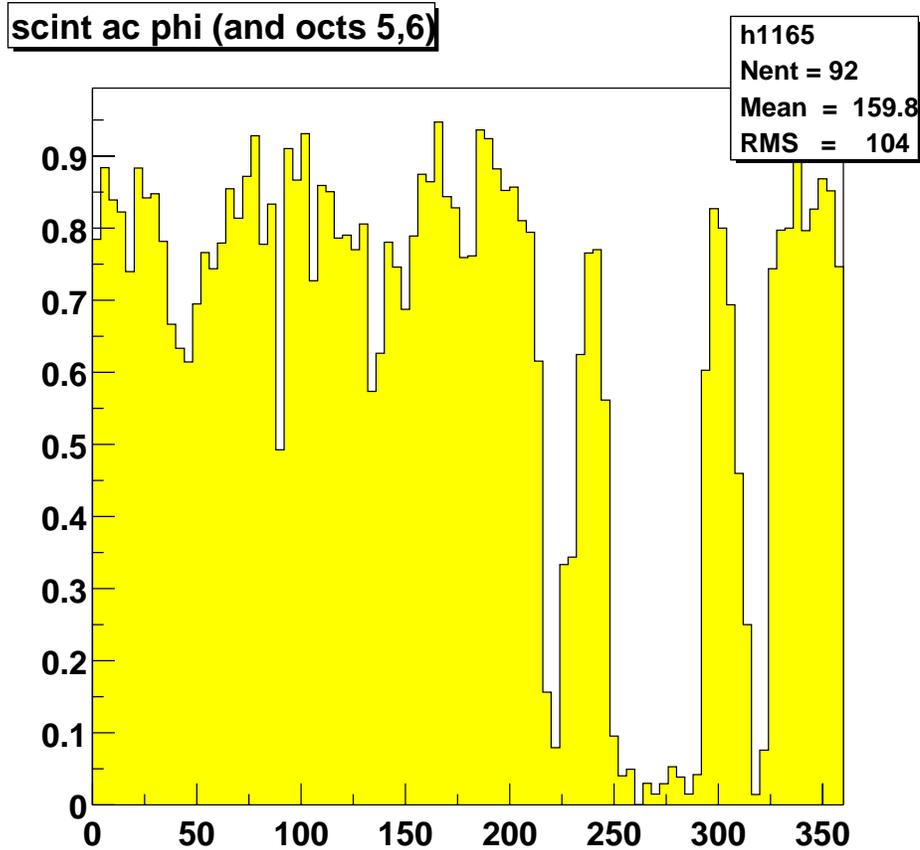


Figure 48. Acceptance of the AB- and AC-layer scintillator in the central region.

Increasing the outside scintillator efficiency might be achieved by the addition of some amount of B-layer scintillator. We will investigate available space in the B-layer during the October 2001 accelerator shutdown when we have access to the collision hall. Alternatively, more complicated trigger algorithms that allow A-layer only triggers at large $|\eta|$ and AC layer coincidences elsewhere could possibly be employed. Neither improvement has yet been studied in detail.

Hits in the C-layer Cosmic Cap counters are dominated by radioactivity in the collision hall ceiling and walls. The main source is ^{22}Na that produces 1.3 MeV photons with a half-life of 2.6 years. The present C-layer singles rate with $L = 2.5\text{-}3 \times 10^{30} / \text{cm}^2/\text{s}$ and without beam are 1.15 MHz and 1.07 MHz respectively. Thus at a threshold of $V_T = 10$ mV and a wide (88 ns) time window, the singles rates are dominated by these low energy photons. While ~ 1 MeV photons are notoriously difficult to shield, work is underway to measure the reduction in singles rate using a thin sheet of Pb for shielding.

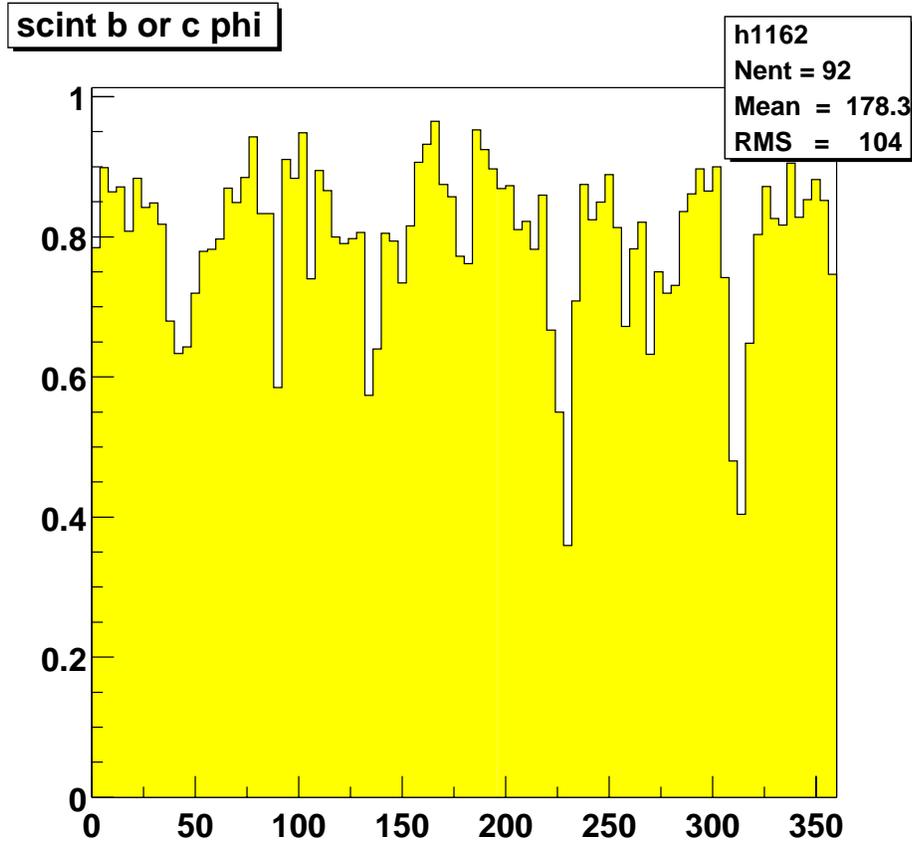


Figure 49. Acceptance of the B- and C-layer scintillators in the central region.

5.7 Summary

It is essential that the L1MU trigger will allow unprescaled single muon triggers in Run 2b. The weakest part of the L1MU trigger is its reliance on the CFT, which was discussed earlier. Important information will be gained once the L1CFT trigger becomes operational. At the moment we do not foresee major Run 2b upgrades for the L1MU trigger. There are items however that can increase the effectiveness of the L1MU trigger. These include additional scintillator in the central region to increase the acceptance of two-layer L1MU triggers in the central region and Pb shielding for the C-layer Cosmic Cap counters. We did not investigate the replacement of the PDT chambers at this time.

6 Level 2 Triggers

6.1 Goals

An overview of the Level 1 and Level 2 trigger system is given in Section 2.1. In Level 2, preprocessors analyze output from the Level 1 trigger of each detector system in parallel. The L2 Muon and L2 Silicon Tracking Trigger (L2STT) preprocessors also receive fully digitized detector data. Event selection takes place based on the high level (physics object) information available in the Global stage. The preprocessors developed for the start of Run2 are for the calorimeter, preshower system, tracking system, and muon system; the L2STT will be added during Run 2a, allowing reconstruction of displaced vertices.

All L2 preprocessors (except the specialized L2STT), and the L2Global processor, occupy a standard L2 crate. The 9U VME64 for physics crates provide dual backplanes: a standard VME bus, and a custom-built 128-bit "Magic Bus" or MBus (a handshaking bus capable of data transfer rates up to 320 MB/s). Each crate contains a number of devices for communication with the experiment's front end and trigger systems and at least two L2Alpha processor cards for analysis of detector subsystem data. The processors are configured for Administrator or Worker functions. Where appropriate, additional specialized hardware for data conversion or processing can be added. A Worker node applies trigger algorithms to its input data. The Administrator does all event processing and local trigger control tasks that do not involve the application of the trigger algorithm. These include verifying data integrity, controlling communication with the trigger framework, controlling the output of monitoring data, and controlling the readout of events to the higher trigger levels.

The input rate to L2 is limited by the SMT digitization deadtime, and the output rate is limited by the calorimeter precision readout deadtime. Since the digitization time of the readout does not change from Run 2a to Run 2b, the primary charge for Level 2 will be to maintain the current rejection, with the same time budget, despite some of the algorithms used in Run 2a Level 2 trigger being moved upstream to Level 1 for Run 2b.

To accomplish this goal, Level 2 must make better use of the time budget by using more powerful processors. This project is already under way and was begun to deal with manufacturing problems in the Run 2a Alpha processors. In addition, the Level 2 trigger preprocessor which uses SMT data, the L2STT (Silicon Tracking Trigger), must also be upgraded to match the new physical configuration of the Run 2b SMT.

6.2 L2 β Upgrade

6.2.1 Concept & physics implications

The University of Michigan CDF group developed the L2Alpha processor card for Run 2. L2Alphas are used by both the CDF and DØ experiments. The PC164 500MHz Alpha motherboard by Compaq Computer is the basis for the L2Alpha design. Custom elements added to the base PC164 design include: a

64-bit PCI-to-VME interface; a block transfer (DMA) controller connecting to the 128-bit MBus; a fast I/O port for registers for control or monitoring, and a bi-directional 64-bit programmed I/O interface between the PCI local bus and MBus. DØ uses L2Alpha processors throughout the L2 trigger, except for L2STT.

The motivation for upgrading from Alpha processors to L2β processors is twofold. Firstly, the existing complement of available Alpha processors is insufficient to implement the baseline L2 trigger. The first production run of alphas yielded 2 stable alpha boards, and 7 more boards operating with varying degrees of reliability. A second production run of 12 alphas is in progress, with a maximum yield of 12 boards, limited by component availability. The baseline system required 16 processors in the trigger crates, and another 6 or so in test and algorithm development facilities. We will adapt our plans to the resources available, combining Administrator nodes (one per crate) and Worker nodes whenever possible. The current commissioning efforts are proceeding with a single Alpha processor per crate. Eventually, as luminosity increases, we will likely have problems accomplishing all processing within the time budget. Thus the first purpose of L2β processors is to replace unreliable processors and to increase the number of processors up to the amount required for smooth running in Run 2a. For this reason, the L2 project is already underway: the boards have been designed and layout and firmware are in progress.

6.2.2 Implementation

Rather than attempt a complete redesign of the Alpha processor board, we use a more modular approach, taking full advantage of industry-standard components and upgrade paths. We follow the same conceptual design for the function of the board in our Level 2 system. Moreover, we **require** both hardware and software compatibility between both Alphas and L2β⁹. This not only facilitates more seamless integration into the experiment, but also offers a great economy in the manpower required to commission the new system.

The L2β implementation replaces the CPU and assorted computer peripheral functions with a commercially produced single board computer (SBC). This SBC will reside on a 6U CompactPCI (CPCI) card providing access to a 64-bit, 66 MHz PCI bus via its rear edge connectors. Such cards are currently available “off the shelf” from several vendors including Advantech¹⁰, Diversified Technology Inc.¹¹, and Teknor¹². The remaining functionality of the board will be implemented in a large FPGA and Universe II¹³ VME interface mounted on a 6U-to-9U VME adapter card as shown in Figure 50.

⁹Extensive documentation on L2βeta can be found at the project's website: <http://galileo.phys.virginia.edu/~rjh2j/l2beta>

¹⁰ <http://www.Advantech-nc.com>.

¹¹ <http://www.dtims.com>.

¹² <http://www.teknor.com>

¹³ Tundra Semiconductor Corp., <http://www.tundra.com>.

The adapter card will contain all DØ-specific hardware for Magic Bus and trigger framework connections. The SBC, in the adapter, will have its front panel at the face of the crate and will be easily removable. This implementation offers several clear advantages:

- The modular design, incorporating existing CPU cards, greatly reduces the engineering, debugging, and prototyping required for the system.
- The modular design provides a clear path for CPU performance upgrades by simple swapping of SBC cards.
- Hardware compatibility allows for a phased-in replacement of the Alphas.

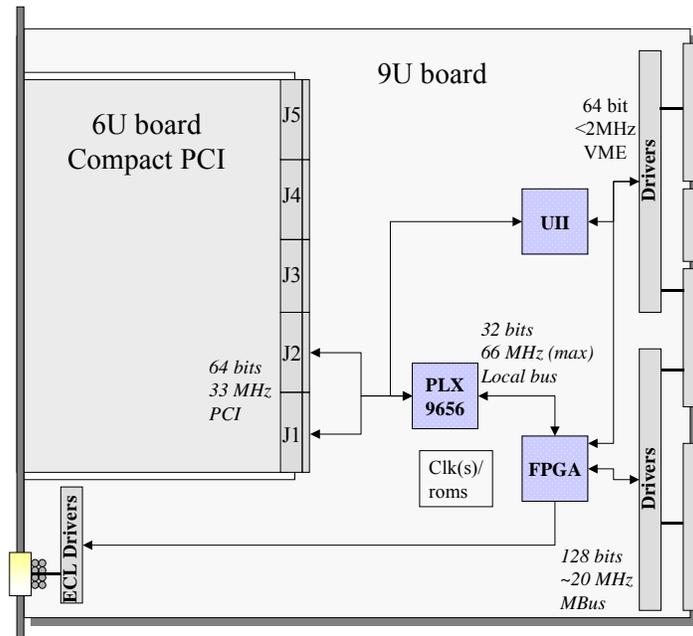


Figure 50. Physical model for the L2 β processor card. Connectors J1 and J2 provide the 64-bit CPCI connection to the CPU. The functions available on the J3-J5 connectors may be assigned arbitrarily by each board manufacturer.

- Higher or lower performance CPUs may be selected. For example, lower performance, less expensive CPUs may be used in Administrator-type processor cards, while more powerful CPUs can be used where physics algorithms are run.
- The use of a much smaller number of components to implement the DØ-specific functions of the board greatly reduces the parts count, increasing reliability and ease of hardware debugging.

As described above, the L2 β s will be composed of two separate devices: a commercial single board computer with a 64-bit CPCI interface and a custom 6U-to-9U adapter card. To minimize development time and to maximize chances of success for the L2 β s, our philosophy has been to use commercial devices where

custom devices can be replaced, to simplify the electrical design of the boards as much as possible, and to push as much of functionality as possible into firmware to reduce hardware prototype cycles.

Initially, we plan to use the MIC-3385 CPCI SBC^{10,14} as our processor in the L2βs. This board (and others in its class) can accept dual Pentium CPUs (up to 933 MHz). As shown in Table 33, these CPUs offer substantial performance gains over the 500MHz Alphas. The SBC supports a local 64-bit wide PCI bus that runs at 33 or 66MHz and, via a PCI-PCI bridge, it provides a 64-bit CPCI interface also supporting both 33 and 66 MHz bus speeds.

Table 33. Performance comparisons¹⁵ for several modern CPUs available on mass-produced VME single board computers. The current Level 2 Alpha CPU is shown at the top of this table. The integer performance of the CPUs is of primary importance for most of the operations in DØ's trigger.

CPU Type	SpecInt95	SpecFP95
Alpha 500 MHz	~15	~21
PIII 800 MHz	~38	~29
PIII 850 MHz	~41	~35
PIII 933 MHz	~45	~39
PIII 1000 MHz	~48	~41

All of the CPCI cards are supported under Linux. The KAI C++ compiler is readily available for this platform and OS. As the KAI compiler and Pentium Linux are fully supported in the DØ Experiment, this offers additional convenience for software support of the system as compared to the Level 2 Alphas using COMPAQ's Cxx compiler. Online code for the Alphas was developed under Linux, which facilitates our move to L2β hardware, and the similarity of byte-ordering in the Alpha and PIII processors simplifies the transition.

The 9U card will both adapt the 6U SBC card to the 9U crate form factor and provide hardware for all custom I/O required of the processor cards. This includes all Magic Bus (MBus) I/O, an interface to user-defined VMEbus J2 lines, the VME interface and outputs to trigger scalars.

Details of the 9U adapter card are shown in Figure 50. The adapter will contain a Universe II PCI-to-VME interface and all custom I/O functions on this card will be implemented in a single FPGA plus assorted logic converters and drivers. The FPGA of choice is the Xilinx XCV405E^{14,16}. This device is particularly suited to our application, because of its large amount of available Block RAM. 70KB of RAM (in addition to >10K logic cells) is available to

¹⁴ See documents at: <http://galileo.phys.virginia.edu/~rjh2j/l2beta/#components>.

¹⁵ Information on Spec measurements can be found at <http://www.specbench.org>.

¹⁶ Xilinx XCV405E, <http://www.xilinx.com>, go to VIRTEX-EM products.

implement internal data FIFOs and address translation tables for broadcasting data from the Magic bus to CPU memory, thus greatly reducing the complexity of the 9U PCB. A 64-bit, 33MHz PCI interface to the CPCI card will be implemented with a PLX 9656 PCI Master chip^{14,17}.

The following requirements will be satisfied in the design of the L2βs to meet or exceed the Alpha's capabilities:

- The 9U board/SBC will exceed the DMA performance of the Alphas. Although the theoretical bandwidth of the PC164's bus is 264 MB/s, the Alpha board typically realizes 80-100 MB/s due to internal buffer limitations. While the PCI front end of the PLX is capable of delivering data at the full 264MB/s, we expect the L2β's effective throughput to be 80-90% of this limit due to the need to broadcast data that is translated into non-contiguous DMA packets.
- On-board FIFOs must be able to receive bursts of data up to the full 320MB/s bandwidth of the Magic Bus. This is accomplished by implementation of fast FIFOs within the Xilinx FPGAs block RAM sections.
- It will be possible for the DMA to be preempted by pending Magic bus I/O requests. An advantage of the new design is that system performance may be fine tuned by configuration of PCI Latency timers and local bus DMA abort logic.
- DMA destinations will be configurable by the CPU for all MBus broadcast addresses. The full functionality of the DMA Mapper (responsible for converting MBus addresses to Memory target addresses) as used in the Alphas will be implemented in a functionally identical way inside the Xilinx.
- It will be possible to interrupt the PCI bus in accordance with events on the local bus (DMA complete, new event arrival, etc). The PLX explicitly supports generation of interrupts from the PLX local bus. The new hardware also supports the use of more convenient interrupt implementations (MSI) defined in the latest PCI specifications¹⁸.
- Magic Bus Programmed I/O (PIO) will be able to support a number of data modes: Master/Write, Master/Read, Slave/Write, Slave/Read. In our design this is a matter for firmware only. Bi-directional drivers are provided to send or receive MBus data.
- Fast MBus arbitration (~15ns). This is consistent with realizable gate delay times in the Xilinx FPGA.

In order to minimize the demand on the experiment's resources to bring the L2βs to completion it is vital that this project tread as lightly as possible on other trigger groups' projects. We have planned at the onset that the L2βs are to be both hardware and software compatible with the Alphas. Hardware compatibility

¹⁷ <http://www.plxtech.com>.

¹⁸ Shanley and Anderson, "PCI System Architecture", Mindshare, 1999.

will largely be a product of proper firmware design. By software compatibility we are referring to high-level software. It should be possible to recompile online code with little or no changes to run on the L2βs. This compatibility will be enforced either by the hardware interface layer, or device driver software and API.

The L2β processors will run Linux Redhat Version 7.1 (kernel version 2.4). The OS version will remain fixed indefinitely for the duration of Run 2, unless there are compelling reasons to upgrade. We will use the KAI compiler and all code will be built using the standard DØ software environment.

The coding tasks for this project can be displayed as in Figure 51. The device driver code will require a rewrite of the hardware interface layer, while the programmer interfaces for the device drivers will be unchanged from the present system. This is necessary for source code compatibility. A large fraction of this low-level software has already been tested. The UII driver will require the least amount of change. In fact, the current device drive code will function “as is” when the PCI base classes it depends on are fully replicated for the PIII boards. The remaining device driver code will have to be completely redesigned, since three former PCI devices will now live inside one FPGA. Different functions of this FPGA will be treated as pseudo-PCI devices to maintain a software interface compatible with the Alphas.

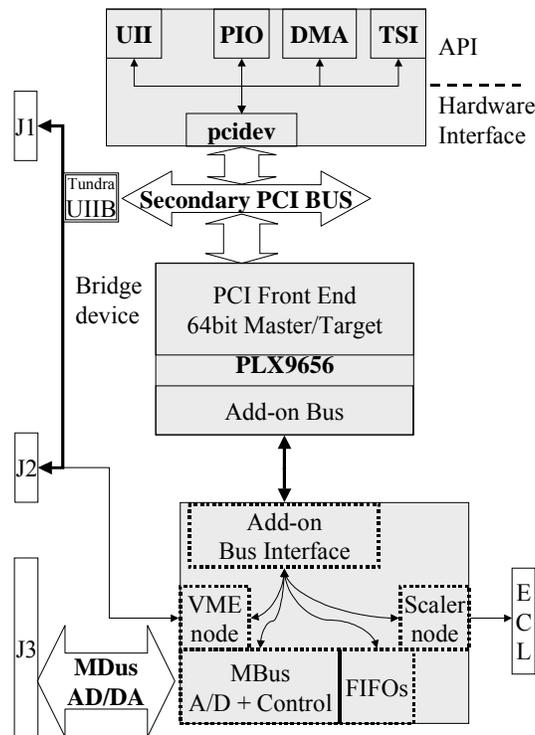


Figure 51. Block diagram of L2β software and firmware components.

The firmware will be composed in loosely coupled blocks similar to those shown in Figure 51. The most complex blocks will be the add-on bus interface and the MBus I/O block. A more detailed summary of the firmware blocks and FPGA resources required is shown in Figure 52. In addition to I/O resources for required functions, “utility pins” are allocated for configuration settings and logic analyzer ‘spy’ channels for assistance in hardware and firmware debugging.

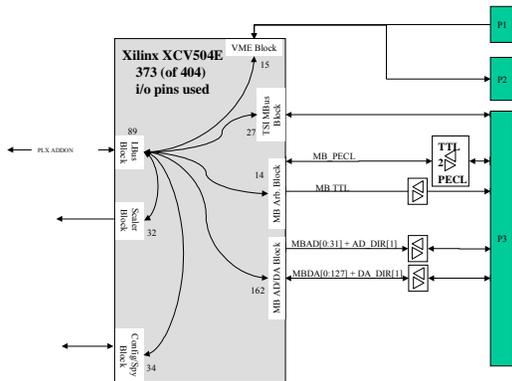


Figure 52. Overview of firmware blocks.

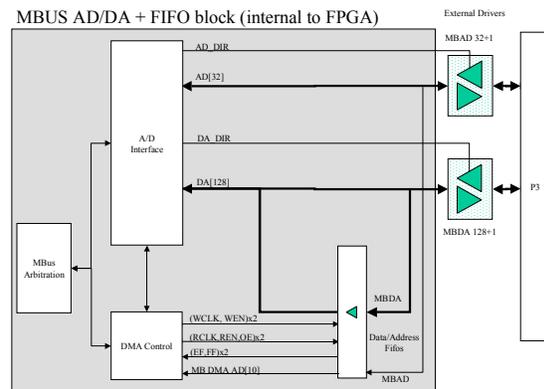


Figure 53. MBus I/O firmware blocks. I/O pin requirements are shown with each block.

Although we have sought to develop a system that is implemented in firmware to as large an extent as possible, we have, as mentioned above, chosen to use a hardware PCI interface rather than to overly complicate our firmware project with a PCI core implementation. We plan to take full advantage of the PLX's features to simplify the firmware design. The PLX 9656 provides a set of local configuration registers mapped to PCI Memory and I/O space and to a local bus address range. Additionally it provides four PCI memory windows for direct data transfers between PCI and local bus addresses. These memory windows will be configured to present interfaces similar to those used in the Alpha's devices. Perhaps the most interesting feature of the PLX 9656 is its ability to become a Master on both the PCI and add-on buses and to fully control DMA transactions. Thus we may simplify the DMA block of the firmware to a protocol that provides data words at the PLX's request. This removes all need for the Xilinx to directly support PCI timing, because the PLX completely decouples the two buses.

The MBus firmware (Figure 53) is responsible for controlling the MBus Data and Address drivers and the (internal) Data FIFOs. It must respond to a request from the PLX to send or fetch data (PIO Master), it must request that the PLX fetch or receive data (PIO Target), and it must provide data to the PLX for DMA transfers (FIFO readout).

The Trigger System Interface (TSI) is fully implemented in the Xilinx FPGA. This interface only functions as a PCI slave and is used to receive and send information to the rest of the trigger system. This includes the DØ trigger signals from the P2 backplane, as well as direct communication with the Trigger Control Computer (TCC) through a front panel connector. It is also used for monitoring the status lines of the Magic Bus.

6.2.3 Performance scaling

Given comparable I/O capabilities, the amount of time required to run complex algorithms should be inversely proportional to the processor speed; more complicated algorithms can be used to process the available data if the processors are faster. However, a factor of two increase of processing power is more useful when supplied in the form of a single processor than in the form of a second identical processor working in parallel. This is because load balancing among multiple nodes is difficult in the Level 2 system due to constraints imposed by the front-end digitization. The front-end digitization holds buffers for 16 events awaiting Level 2 trigger decisions. A critical restriction in the system is that L2 results (accept or reject) must be reported to the front ends in the order in which the triggers were taken at L1. While one processor works on an event with a long processing time, other events will arrive and fill the 16 front-end buffers. Other processors working on these events will go idle if they finish processing them quickly, since they cannot receive new events until the pending decision on the oldest event is taken. Faster processing for each event in turn is thus more desirable than adding additional processors, once a baseline level of parallelism is established.

As one possible path to processor upgrades, we note that the L2 β CPU card architecture allows equipping the cards with dual processors that share the card's memory and I/O. This upgrade is attractive because its incremental cost is low, but it would require a substantial software effort to turn it into increased throughput, even if it is possible to build code that takes advantage of the dual processors without writing thread-safe code. However, a dual-processor upgrade might be attractive for reasons other than performance. One processor could keep the Linux operating system active for debugging of problems in algorithms run in the second processor. Or one could run a production algorithm in one processor and a developmental version in the second processor. This second processor might even be operated in a "shadow" mode (as in Level 3), processing events parasitically, but skipping events if the developmental algorithm gets behind, or is being debugged.

6.2.4 Cost & schedule

The L2 β project is underway, and consists of a fruitful collaboration among Orsay, University of Virginia, and University of Maryland. Orsay is designing and building the 9u boards, and writing the firmware. Virginia is specifying the processor, writing software, and (with Maryland) specifying firmware functionality. Testing and commissioning will take place at Orsay, then Virginia/Maryland, then at Fermilab. Fermilab has provided \$50K of funds to get the project started.

Orsay has provided contributions of \$20K in cash and \$127K in-kind (engineering and travel), and Virginia and Maryland have provided another \$10K in-kind (travel). Manpower for testing, commissioning, and maintenance has also been committed. The baseline system provides for replacement of all alphas, including the 14 alphas originally reserved for upgrades to the Level 2 trigger during Run 2a.

We direct the reader to Appendix B, which contains a cost estimate for that portion of the Level 2 β project associated with completion of the Run 2a system. Our estimate of the engineering needed is included. The total M&S is \$411k, and the total sub-project cost after the addition of 37% contingency is \$562k. Identified sources of funding are shown in the spreadsheet as well – these come to a total of \$192k, leaving \$370k remaining to be identified in order to complete the project. We include in Table 34 below the current milestones for the Level 2 β project.

Table 34. Schedule milestones for the Level 2 β project

	One prototype round needed	Two prototype rounds needed
Final Prototype Delivery	Jan 1, 2001	Mar 1, 2002
Hardware Verification	Mar 8, 2002	May 8, 2002
Begin Production	Apr 8, 2002	Jun 8, 2002
Pre-production Verification	Jun 8, 2002	Aug 8, 2002
Begin Installation	Aug 8, 2002	Oct 8, 2002
Final System	Sep 1, 2002	Nov 1, 2002

For Run 2b, we are proposing a partial upgrade of the Level 2 β system by allocating sufficient funds to later replace the processors on 12 of the 24 boards. This is in anticipation of the potential increase in computing power that could at that time be used to implement more sophisticated tracking, STT, and calorimeter/track matching algorithms at Level 2 in response to the increased luminosity. Since this is an upgrade associated with Run 2b, we earmark this money for FY04 (see Table 46 in the Summary section at the end of this report). We base this estimate on our experience with the Run 2a Level 2 β system; the cost is estimated to be \$83k, including 34% contingency.

6.3 STT Upgrade

6.3.1 Concept & physics implications

The DØ Level 2 Silicon Track Trigger (L2STT) processes the data from the L1 Central Track Trigger (L1CTT) and the Silicon Microstrip Tracker (SMT) to associate hits in the SMT with tracks found by the L1CTT. These hits are then fit together with the L1CTT information, thus improving the resolution in momentum and impact parameter, and the rejection of fake tracks. The STT matched to the Run2a SMT detector is being constructed with NSF funds for delivery in the

summer of 2002. An upgrade for Run2b, however, will be necessary in order to match the new geometry of the Run2b Silicon Tracker.

Tracks with large impact parameter are indicative of long lived particles (such as b-quarks) which travel for several millimeters before they decay. The L2STT thus provides a tool to trigger on events with b-quarks in the level 2 trigger. Such events are of particular importance for the physics goals of Run 2. The Higgs boson decays predominantly to $b\bar{b}$ pairs if its mass is less than about $135 \text{ GeV}/c^2$. The most promising process for detection of a Higgs boson in this mass range at the Tevatron is associated production of Higgs bosons with W or Z bosons. If the Z boson decays to neutrino pairs, the b-quarks from the Higgs decay are the only detectable particles. In order to trigger on such events (which constitute a significant fraction of associated Higgs production) the L2STT is essential to detect jets that originate from b-quarks at the trigger level. The L2STT will also allow the collection of a large enough sample of inclusive $b\bar{b}$ events to see the decay $Z \rightarrow b\bar{b}$. Such a sample is important to understand the mass resolution and detection efficiency for $b\bar{b}$ resonances, and to calibrate the calorimeter response to b-quark jets. The latter will also help to drastically reduce the uncertainty in the top quark mass measurement, which is dominated by the jet energy scale uncertainty. Detailed descriptions of the physics benefits of STT are written up as DØ Notes^{19,20}.

6.3.2 STT Architecture

The L2STT consists of three types of electronics modules:

- The Fiber Road Card (FRC) receives the data from L1CTT and fans them out to the other modules. It also receives Serial Command Link (SCL) information from the Trigger Control Computer (TCC) and initiates appropriate action, and manages the buffers used for storing processed data for readout by the VME Buffer Driver (VBD).
- The Silicon Trigger Card (STC) receives the raw data from the SMT front ends. These are then processed to find clusters of hit strips and associate these clusters with the tracks found by L1CTT.
- The Track Fit Card (TFC) fits a trajectory to L1CTT tracks and the SMT clusters associated with it. The results are then relayed to the Level 2 Central Track Trigger.

Each of these modules is based on the same 9U by 400 mm VME motherboard. Logic daughter boards carry out the main function of the three modules. VME Transition Modules (VTM) receives the inputs from L1CTT and SMT. Serial Link Transmitter and Receiver Boards (LTB/LRB) transmit data between modules.

¹⁹ "A silicon track trigger for the DØ experiment in Run II – Technical Design Report", Evans, Heintz, Heuring, Hobbs, Johnson, Mani, Narain, Stichelbaut, and Wahl, DØ Note 3510.

²⁰ "A silicon track trigger for the DØ experiment in Run II – Proposal to Fermilab", DØ Collaboration, DØ Note 3516.

The STT modules are located in 6 VME crates, each serving two 30-degree azimuthal sectors. Each of these crates holds one FRC, nine STCs - one for eight silicon sensors, and two TFCs - one per 30-degree sector.

6.3.3 Reconfiguration of STT for Run 2b

The silicon tracker planned for Run 2b consists of more sensors than the present detector. The STT must be upgraded to process the data that these sensors provide. The Run 2b silicon tracker will include 552 readout units (one or more sensors read out through one HDI) arranged in 6 layers of sensors (see Figure 54). Since one STC accommodates eight such HDIs, 12 STCs are required in each of the six VME crates to process these data. Since we currently have nine STCs per crate, we will need a minimum of 18 additional STC modules.

The data must be channeled into TFCs such that all hits from a track are contained in one TFC. In layers 0, 1, and 2 the overlaps between adjacent sensors are large enough so that each sensor can be uniquely associated with one TFC. This divides the detector into 12 azimuthal sectors as indicated by the shaded regions in Figure 54. To maintain full acceptance for tracks with $p_T > 1.5$ GeV/c and impact parameter < 2 mm, the data from some sensors in layers 3, 4, and 5 must be channeled into two TFCs, which are in some cases located in different crates. This is not the case in the current configuration, but should not present any problems. We are limited to 8 STC inputs into each TFC, which is sufficient for the Run 2b detector geometry.

6.3.4 Cost and Schedule

The cost estimate for the additional hardware required for the L2STT in Run 2b are shown in the second spreadsheet in Appendix B. The estimate includes our current understanding of the engineering needs. Quantities include 10% spares. The most effective way to acquire this hardware would be at the time the production of STT modules for Run 2a takes place. Combining the 2a and 2b production runs, as well as purchasing many of the processors before they become obsolete, would save much time, manpower, and money. Since the Run 2a STT module manufacturing is scheduled for the beginning of CY02, we will need the funds for the Run 2b STT upgrade in FY02.

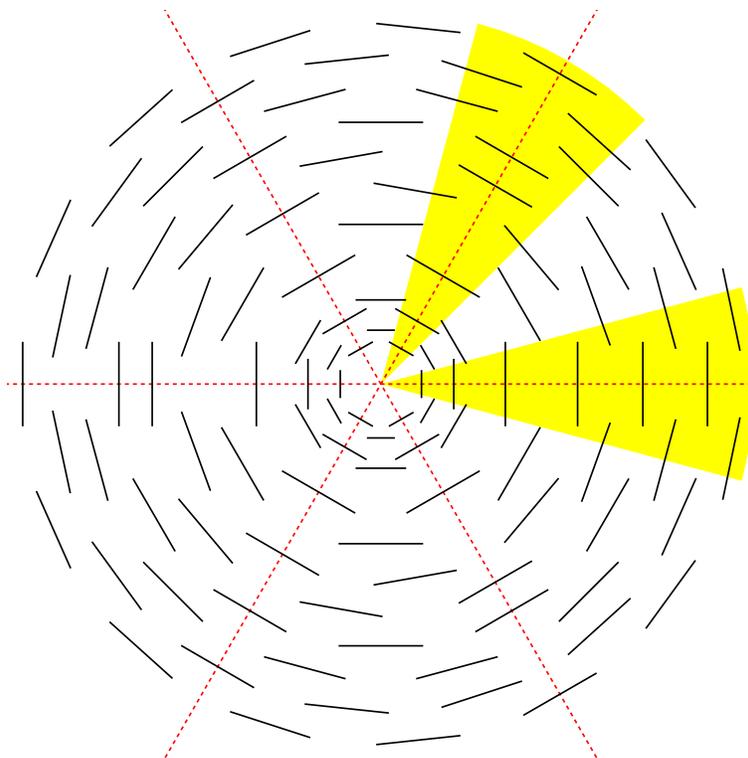


Figure 54. Geometry of DØ Silicon Tracker for Run 2b.

6.4 Other Level 2 Options

At this point there are several further options under study.

If it appears that bandwidth limitations will arise because of higher data volume per event in Run 2b, we could consider optimizing MBT firmware to raise DMA bandwidth to perhaps 150MB/s from the present estimate of 120MB/s. The main cost would be engineering time, perhaps \$10-15k. The Alphas will likely limit throughput to 80-100MB/s, but the L2 β processors are likely to be capable of larger bandwidth than the current Alpha processors. A further option is to increase the bandwidth of the individual Cypress Hotlinks connections. The transmitters and receivers are capable of upgrading from the current 16MB/s to perhaps 40MB/s. However, the implications of operating such a system need to be explored, given that the muon inputs will likely remain at lower frequency and that hardware is shared between the muon subsystem and other parts of the L2 system. Some hardware might actually have to be rebuilt if this is necessary, so this could be more costly if such a bandwidth upgrade is needed.

Another option under study is adding stereo information to either L1 or L2 triggering to help combat fake axial tracks due to pileup. If this were done in L1, any new outputs from would need to be sent to L2. Such outputs, probably only 4 at most, could require additional FIC-VTM²¹ card pairs costing some \$5k per additional 4-input card pair. If this option were pursued at Level 2, it would likely

²¹ For more details, see <http://www.pa.msu.edu/hep/d0/l2/fic.htm>.

result in some \$50k in new cards pairs, and another \$50k in engineering, backplane, crate, power, and other infrastructure. In the case of L2, this would have to be justified by an improvement in fake rates after the L2STT trigger confirmation of L1CTT axial tracks.

A third option is calculation of a longitudinal vertex for use in calculating E_T and sharpening L2 thresholds. This could be approached by adding post-processing of the L2STT tracks, based on the granularity of detectors, and would result in resolution of a centimeter or two, well-matched to the position precision of L2 data. This would probably require CPU power rather than new hardware. The gain of such improved E_T resolution would depend on the physics emphases of Run 2b. Precision physics which requires extremely high acceptance efficiency might actually not prefer such corrections, because erroneous assignments might result in longer acceptance tails than simply using $Z_V=0$. But search-oriented physics could use the improved acceptance due to an efficiency curve rising more rapidly to moderately high (80-90%) values.

Another possible upgrade would improvement of the DSP daughter boards of the SLIC²², particularly if we find we are I/O limited. Such an effort would be on the scale of \$50-100k for hardware and engineering. We will need operational experience with real data to determine whether this proves necessary.

6.5 Conclusions for Level 2 Trigger

- The Level 2 β upgrade needs the bulk of its funds approved for early 2002, because the initial phase is required for Run 2a.
- The Level 2 STT modifications for the Run 2b SMT also needs the bulk of its funds approved for early 2002, because the new components are most effectively acquired as part of the initial production run.
- Construction of additional VTM's for the Run 2b STT, for readout of the Run 2b SMT, or for providing stereo information to Level 2, should be pursued in a coordinated fashion, and the needs understood soon, because parts are becoming difficult to procure for this design.

²² For more details, see <http://www.nevis.columbia.edu/~evans/L2mu/slic/slic.htm> .

7 Level 3 Triggers

7.1 Status of the DØ Data Acquisition and Event Filtering

7.1.1 Description of Current Data Acquisition System

With an input event rate of 1000 Hz and an accept rate of about 20 Hz, the DØ data acquisition and filtering system will support the full Run 2 program of top, electro-weak, Higgs, and new phenomena physics. (At the nominal event size of 250 Kbytes, the input and output bandwidth are 250 Mbytes/sec and 5 Mbytes/sec, respectively). Event data is collected from the front-end crates with a system of custom-built hardware and transmitted to a filtering farm of 48 Linux nodes. Event rejection is achieved in the farm by partial reconstruction and filtering of each event.

The complete system is shown in Figure 55. Data is collected in a VME front-end crate by the VME Buffer Driver (VBD) boards using VME DMA transfers. The VBD interface board or (VBDI, not shown) collects data from one or two chains of VBD's. Each chain consists of as many as 16 VBDs connected by a 32-bit wide data cable. In addition a token loop connects the crates in a chain. Upon receipt of a token, a VBD places its data on the data cable. The token is then modified and passed to the next VBD in the chain which then acts on it. The VBDI board collects the data and sends it over optical link to a VBD readout controller (VRC).

The VRC is a PC with a custom optical link card called the serial interface board (SIB). The SIB is used throughout the system for high-speed data connections. Each VRC contains one input SIB and one output SIB. The system nominally includes eight VRCs.

The VRCs then pass the data to the four segment bridges (SB) via optical links. (Initially the system will be instrumented with three segment bridges but can be scaled to four.) Each VRC sits on a loop communicating with segment bridges. As the data blocks pass through the SB loops they are directed to available L3 nodes. Each SB has 12 SIBs, three each in four PCs. Eight of the SIBs communicate with the VRCs. The remaining four communicate with the Level 3 nodes via optical links.

The Level 3 nodes have four SIBs and a CPU that collects the data blocks. Once assembled in the L3 data acquisition nodes, the data is transmitted via ethernet to a Cisco switch, which, in turn, transmits the data to a farm of 48 Linux filtering nodes. The filtering nodes partially reconstruct the data and reject data based on event characteristics.

The flow and final L3 node destination of an event is directed by the event tag generator (ETG). The ETG uses L1 trigger information and look-up tables to form an "event tag". The tag is sent to each SB via LVDS links. To receive this information each SB has a fifth PC instrumented with an event tag interface (ETI). The ETIs determine if a SB can accept a tag if not, the ETI sends the tag to the next SB. This is a closed, recirculation loop. Tags are returned to the

ETG with a bit set for each SB. The ETG can decide to recirculate an event, timeout, or shut down the triggers. The ETG also has a special purpose interface to the L1 trigger called the VBDI-prime

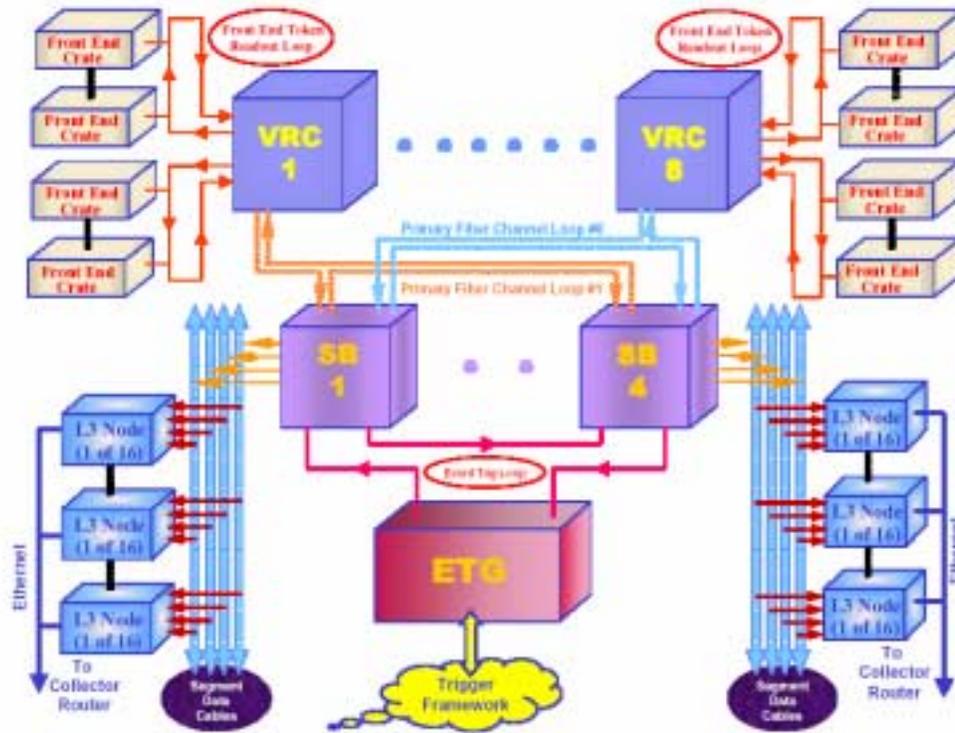


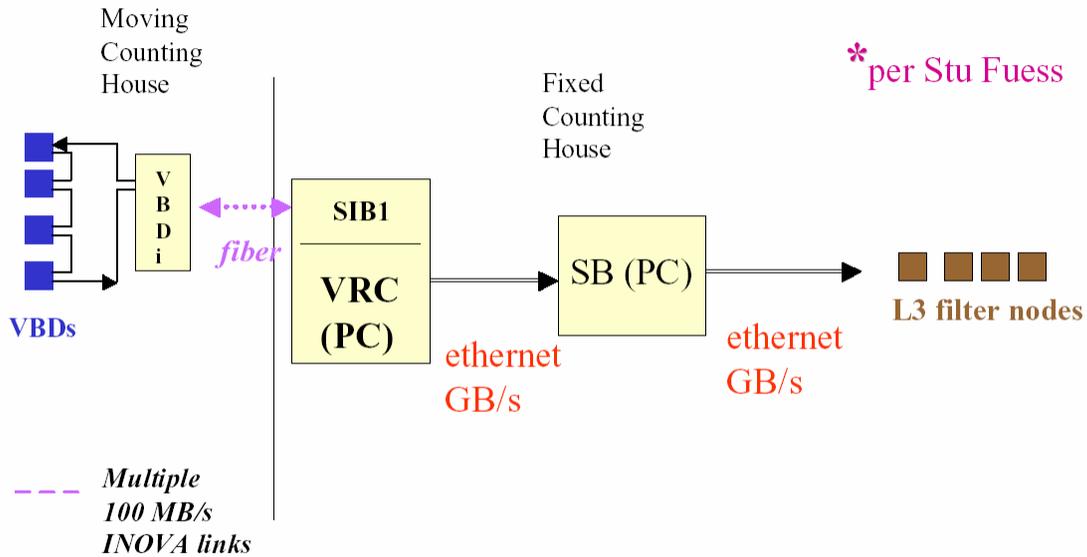
Figure 55. The full L3/DAQ data path.

To recapitulate, the system is composed of eight VBDIs, 8 VRCs, 3 SBs, 48 L3 nodes, 48 filtering nodes with event flow controlled by the ETG. There are four custom cards in the system including eight VBDIs, about 300 SIBs, three ETIs, and one VBDI-prime.

7.1.2 Status

Figure 56 shows the current implementation of the L3 data acquisition and filtering system, which supports commissioning at an 80 Hz event rate. (A typical event has a size of 250 Kbytes.) The VBDs are legacy hardware from Run I and are installed and functioning. Three prototype VBDIs and VRCs transmit data via ethernet to software emulated SBs and ETG. Presently, the events arrive and are filtered in ten or so L3 nodes.

L3DAQ Evolution: *Stage 1 Enhanced**



Event rate = 100's of Hz (at 250 KB/event)

Limitation: network I/O through Segment Bridge

Figure 56. Current scheme at DØ

By the end of the calendar year, numerous upgrades and additions will expand the capacity to 500 Hz and improve filtering capability. The installation of production VBDs and VRCs will occur. Similarly the emulated SBs will be upgraded and increased in number. These upgrades are scheduled for October and November. The ethernet switch between the L3 nodes and filter farm, as well as the 48 filtering nodes, are on hand and installed. The filtering farm is expected to be fully commissioned by mid-November.

Layout of the production VBDs and SIBs is currently underway. Production of sufficient numbers to populate eight VRCs and a prototype hardware SB is scheduled for mid-October. The overall hardware schedule has slipped several months because of technical difficulties with the fiber transceivers. ETI design and production will occur through November and December. The installation of hardware SBs at DØ will start in February and continue through March. Final commissioning of the system with all components will occur in April and May.

7.1.3 An Alternate System

The system described above is the baseline data acquisition system for DØ but has had schedule and technical difficulties. As a result DØ is aggressively developing a backup solution based upon commercial networking hardware. Preliminary analyses and tests show that such a system, shown in Figure 57, is feasible and can provide 1 kHz or more bandwidth. The system is composed of single-board computers (SBC) in each front-end crate, which communicate with the filtering farm through a series of ethernet switches. The SBCs transmit data

to a series of 4 Cisco 2948G switches, which, in turn, transmit data to a single Cisco 6509 switch. The large switch finally routes the data to L3 filtering nodes.

SBCs and switches have been ordered for a “slice” test in early November. Both the Fermilab Computing Division and DØ are participating in these tests and the system design. The full slice has ten SBCs to read out at least one VME crate of each type, 1 Cisco 2948G switch used to transfer the data from the 10 SBCs on 100 Mbit copper cables to 1 Gbit optical fibers, 1 Cisco 6509 switch to transfer the data from there to the Level 3 nodes, and the 48 Level 3 filter nodes.

Ten SBCs have been ordered from VMIC, and delivery is expected in late October. In the meantime, similar, older boards are used for software development. One Cisco 2948G switch has been ordered and should be delivered soon. Fermilab does have a spare, which could be used if necessary and not needed elsewhere. A spare Cisco 6509 switch has been installed at DAB, and cabling to a number of crates to be used in early tests is underway. All 48 Level 3 filter nodes are available part-time, since integration of the farm in the existing DAQ will also happen during the October shutdown.

On the software front, basic readout of a calorimeter crate has been achieved, and results are encouraging. Good progress has been made on the software design for the full system, and details of the interactions between the various systems are being ironed out. Effort assigned to the project has increased steadily and has reached the minimum required level.

The main tests proposed are: (1) establish that all types of crates used in DØ can be read out reliably using SBCs; (2) establish that events can be routed from multiple SBCs to individual Level 3 nodes based on Level 1 and 2 trigger decisions while keeping system latency low; (3) establish that the SBCs can handle simultaneous connections to 48 Level 3 nodes, sending event fragments to each of these; (4) establish that event building can be done in the level 3 nodes with reasonable CPU consumption; (5) establish that no congestion occurs at any point of the network when reading out 10 SBCs at high rate (in the full system, the signal from 10 SBCs is carried by 1 fiber link from the Cisco 2948G to the Cisco 6509 switch).

Further tests will involve tuning of communication parameters between the various system components. It should also be demonstrated that nodes receiving event fragments from 65 SBCs do not exhibit non-linear scaling effects leading to excessive CPU time consumption. While the 10 SBCs are not sufficient to establish this, the 48 nodes can be used instead, since the nature of the sending computer has no impact on this.

(draft) VME readout Controller System Diagram

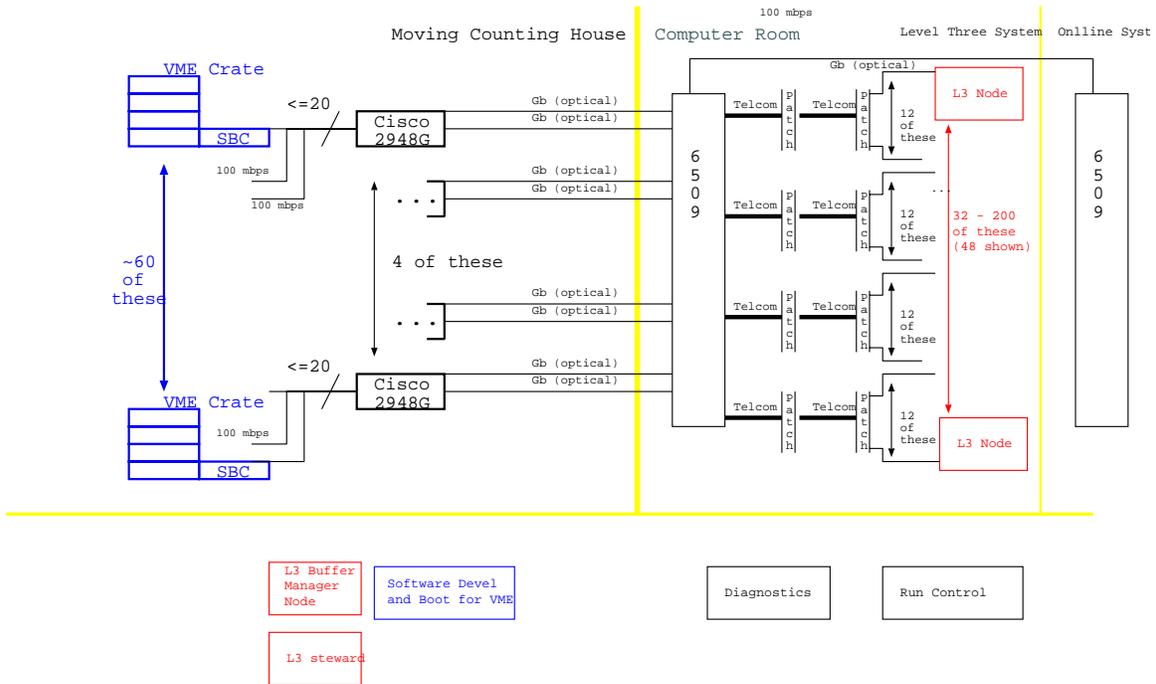


Figure 57. VME/Commodities Solution.

7.1.4 Comments on Current Status

The current Level 3 system as designed by the Brown/ZRL team remains the baseline system being pursued DØ. As has already been noted, the delivery of this system has been beset by serious schedule and technical difficulties. We are therefore pursuing the commercial alternative as a backup solution should the baseline system continue to encounter difficulties. DØ management is very carefully monitoring the development of both systems. Extensive discussions of the status of sub-project milestones, technical status, integration issues, and short- and long-term schedule development for both systems take place in weekly meetings with all of the principals. These discussions are overseen by a DAQ Technical Review Committee, appointed in July by the DØ Technical Manager, which consists of 10 scientists and technical personnel from both DØ and the Fermilab Computing Division.

The final configuration of the data acquisition system will depend on a number of factors including the performance of the baseline system, the results of the slice test, the need for sustained uninterrupted data flow, long term maintenance issues, time to completion for the systems, and cost. DØ Management, taking into consideration advice from the DAQ Technical Review Committee, will consider all of these issues in developing a plan for the final system. The time scale for these deliberations is set by the delivery of eight production VRCs and completion of the slice test, both of which are expected before the end of the calendar year.

The baseline solution was costed in equipment funds for the Run 2a upgrade, with more than 80% of the \$1,049k in total project cost having been obligated to date. What remains will be covered by what exists in the original Run 2a estimate, and there is therefore no additional cost associated with this system. Nevertheless, we consider the risk associated with completion of the baseline DAQ option to be sufficiently high that we have generated a preliminary cost estimate of the commercial DAQ solution (see Table 35 below). The major costs have been based on orders placed for the slice test and the LINUX filter farm development. A contingency of 50% has been applied.

Table 35 Preliminary cost estimate for commercial data acquisition system. A contingency of 50% has been applied. Manpower is not included.

Item	# Required	Unit cost (K\$)	M&S total (K\$)	Cost + 50% Contingency (K\$)
Single board computers	80	2.9	232	348
Digital I/O cards	80	0.7	56	84
CISCO 6509 switch (with blades)	1	80	80	120
CISCO 2948 switch (concentrators, w/blades)	5	4.2	21	32
Additional filter nodes	16	2.2	35	53
Cables & connectors	-	-	25	38
<i>TOTAL COST</i>			<i>\$449</i>	<i>\$675</i>

7.2 Run 2b Upgrades to Level 3

The Level 3 trigger consists of two principle elements: a high speed data acquisition system that provides readout of the entire detector at rates expected to exceed 1 kHz (described above), and a processor farm that utilizes software filters written to select events that will be permanently recorded. Since the required Run 2b data acquisition bandwidth is expected to be made available once the Run 2a Level 3 hardware is fully commissioned, the most likely need for Level 3 upgrades will be to provide increased processing power in the farm.

Given the increased selectivity of the Level 1 and Level 2 triggers, it is expected that there will be an increase in the complexity of the Level 3 filter algorithms. This will undoubtedly lead to the need for faster processors in the Level 3 nodes. However, the tremendous flexibility of Level 3 to implement complex trigger filters, combined with the lack of good experience in understanding the trade-off between CPU processing time and trigger rejection, make it very difficult to estimate the required increase in processing power.

Historically, DØ has equipped the Level 3 farm with the fastest processors on the market within the chosen processor family. It would seem reasonable to expect this approach to continue. At the time of the Run 2b upgrade, Moore's law would lead us to expect an approximately four-fold increase in processing speed over what is currently available. Thus, a significant increase in Level 3 processing power could be obtained by replacing the Run 2a Level 3 processors with the latest technology available in 2004.

7.3 Conclusions

We conclude that the Level 3 Linux filtering nodes should be replaced as part of the Run 2b upgrade. We have opted to pursue a series of partial upgrades to the filter farm, performed on a yearly basis as the luminosity increases. The responsibility for this sub-project falls under the online system, and is therefore discussed in more detail in the next section. We note here that the overall cost we anticipate for this upgrade is \$200k.

8 Online Computing

8.1 Introduction

8.1.1 Scope

For the purposes of this document, the DØ Online system will be defined to consist of the following components:

- Online network,
- Level 3 Linux software filter farm,
- Host data logging system,
- Control room computing systems,
- Data monitoring computing systems,
- Database servers,
- File servers,
- Slow control system,
- plus the associated software for each of these elements.

8.1.2 Software Architecture

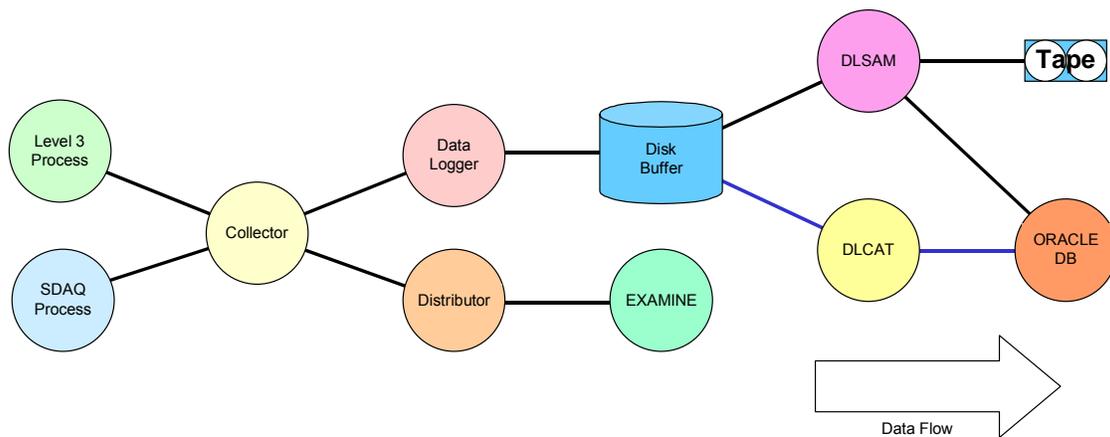


Figure 58. Online system software components.

The software architecture of the Run 2b Online system is unchanged from that of Run 2a. Some components will need replacing and/or updating, but there are no structural differences. The major software components of the current system are illustrated in Figure 58. The slow control system components are not illustrated in the figure.

8.1.3 Hardware Architecture

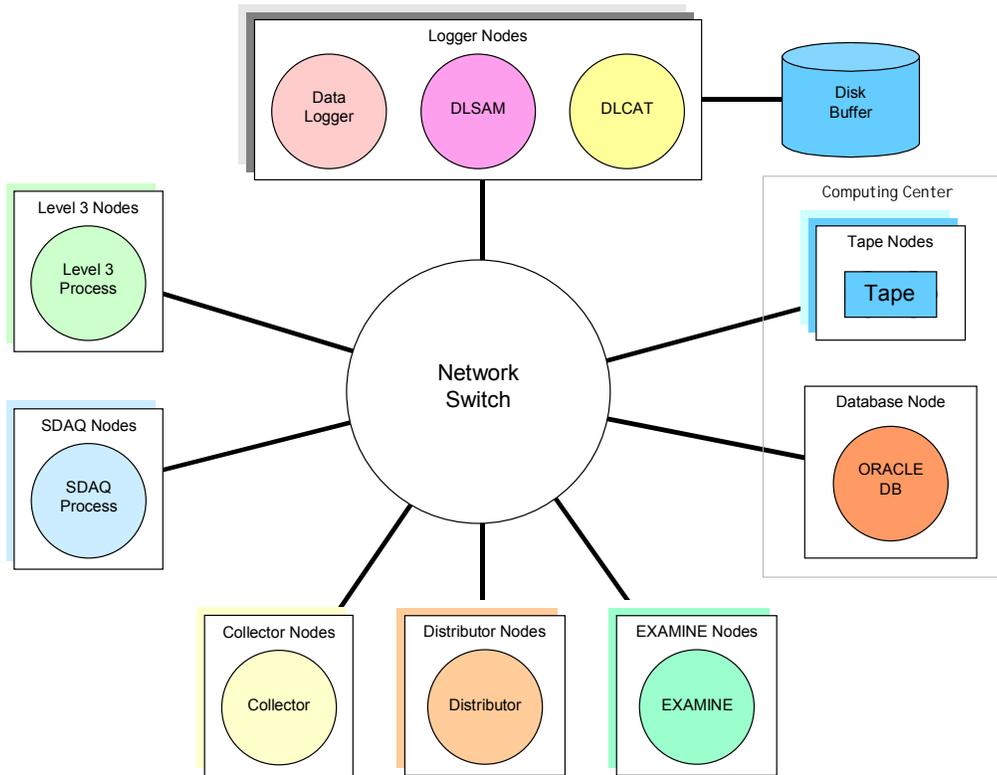


Figure 59. Online system hardware components.

The hardware architecture of the Run 2b Online system is also largely unchanged from that of Run 2a. The current architecture is illustrated in Figure 59. The center of the system is one or more high capacity network switches (Cisco 6509). The event data path includes the Level 3 Linux filter nodes, the Collector and Distributor nodes, the Data Logger nodes with large disk buffers, and the final data repository in the Feynman Computing Center. The EXAMINE nodes provide the real-time data monitoring functions. Some of the Slow Control system nodes also participate in the Secondary data acquisition (SDAQ) path. Not included in this figure are the Control Room, File Server, and most of the Slow Control system nodes.

For Run 2b many of these computer systems will need to be updated or replaced.

8.1.4 Motivations

The primary considerations governing the development of the DØ Online system for Run 2b are supplying the enhanced capabilities required for this running period, providing hardware and software maintenance for the (by then) five-year old hardware, and supplying the required software support. We expect the requirements for the Online data throughput to at least double, largely driven

by the ability of the Offline analysis systems to absorb and analyze the data. The Online computing systems will reach the end of their viable lifetime in capability, maintainability, and software support by the Run 2b era. The gradual replacement of many of the component systems will be essential.

8.1.4.1 Enhanced Capabilities

The factors limiting the rate at which DØ records data to tape have been the cost of storage media and the capability of the Offline systems to analyze the data. Assuming five years of improvements in computing capability, it is reasonable to expect the Offline capacity for absorbing and analyzing data to more than double. The Online system should be capable of providing equivalent increased data throughput.

After five years of experience in analyzing events, it can be expected that more sophisticated software filters will be run on the Level 3 trigger farm. These more complicated codes will likely increase execution time. The resulting increased computing demand in Level 3 will need to be met by either an increase in the number of processors, replacement of these units by more capable processors, or both.

It is also expected that data quality monitoring software will be vastly improved by the Run 2b era. These capabilities again are likely to come at the cost of increased execution time and/or higher statistical sampling requirements. In either case, more numerous and more powerful monitoring systems will be required.

8.1.4.2 Hardware and Software Maintenance

By the time of Run 2b, the computing systems purchased for Run 2a will be more than five years old. In the world of computing hardware, this is ancient. Hardware maintenance of such old equipment is likely to be either impossible or unreasonably expensive. Experience shows that replacement by new (and under warranty) equipment is more cost effective. Since replacement of obsolete equipment not only addresses the maintenance question, but also issues of increased capability, it is likely to be the most effective course of action.

The DØ Online system is composed of several subsystems that have differing hardware components and differing maintenance needs. Subsystem specific issues will be addressed in the following sections.

8.1.4.3 Software Support

Several different operating systems are present in the Online system, with numerous custom applications. We have tried, wherever possible, to develop software in as general a fashion as possible so that it can be migrated from machine to machine and from platform to platform. However, support of certain applications is closely tied to the operating system on which the applications run. In particular, ORACLE database operations require expertise that is often specialized to the host operating system. By the time of Run 2b, there is expected to be a consolidation in ORACLE support by the Laboratory that will not

include the existing Compaq DØ Online database platform. These platforms will thus need to be replaced.

8.1.5 Interaction with the Computing Division

The Run 2a Online system was developed through an active partnership with the Computing Division's Online and Database Systems (CD/ODS) group. It is essential that this relationship be maintained during the transition to the Run 2b system. While the level of effort expended by CD/ODS personnel has already decreased relative to what it was during the height of the software development phase of the Run 2a Online system, the continued participation of this group will be needed to maintain the system, and to migrate the existing software to new platforms as these are acquired. Computing Division assistance and expertise will be particularly critical in the area of database support since the Oracle consultant who led the design of the current system is not expected to be involved in maintaining the system. The continued involvement of the CD in the Online effort, which will presumably be described in a future MOU, will be left mostly implicit in later sections of this document, but will nevertheless continue to be crucial to the success of the effort.

8.2 Plan

A description of planned upgrades follows for each component noted in the Introduction. The philosophy and architecture of the Online system will not change, but components will be updated. Note that some changes are best achieved by a continuous, staged approach, while others involve large systems that will need to be replaced as units.

8.2.1 Online Network

The backbone of the DØ Online computing system is the switched Ethernet network through which all components are interconnected. The Run 2a network is based on a Cisco 6509 switch (a second Cisco 6509 switch is under consideration for a network-based DAQ readout system). The switch is composed of a chassis with an interconnecting backplane and various modules that supply ports for attaching the Online nodes. The total capacity of the switch is determined both by the chassis version and the number and versions of the component modules.

The existing Cisco 6509 switch will need to support an increased number of Level 3 nodes, a slight increase in the number of (high bandwidth) host system nodes, and more gigabit-capable modules. The switch chassis will need to be upgraded to support these newer modules. The cost of this upgrade and the new modules is indicated in Table 36.

Table 36. Network upgrade cost.

Item	Cost	Schedule
Upgrade existing Cisco 6509	\$80K	2 years @ \$40K per year

The upgrades of the existing switch will be purchased and installed as required.

8.2.2 Level 3 Linux Filter Farm

The final configuration of the Run 2a Level 3 filter farm is currently unknown. The expected configuration to be completed with Run 2a DAQ funds calls for 48 Windows NT nodes, connected to the readout system, to feed 48 Linux filter nodes. Existing funds do not allow for further expansion of this Linux filter farm.

We expect that the computing capacity of the Linux filter farm will be stressed at current Level 3 input rates with only the existing hardware. As Offline analysis software improves, some algorithms are likely to move into Level 3. As Level 2 filter algorithms are improved, the complexity of the Level 3 algorithms will increase in tandem. All of these efforts to enhance the capability of the Level 3 trigger will come at the expense of processing time. More and improved filter nodes will therefore be required. Table 37 gives a summary of the required hardware.

Table 37. Level 3 node upgrade cost.

Item	Cost	Schedule
Level 3 filter nodes	\$250K	5 years @ \$50K per year

Purchase and installation of the additional Level 3 filter nodes will be staged over the years leading up to Run 2B.

8.2.3 Host Data Logging Systems

The current DØ Online Host system comprises three Compaq/Digital AlphaServers in a cluster configuration. Two of the machines are AlphaServer 4000s (purchased in 1997 and 1998) and the third is an AlphaServer GS80 (purchased in 2000). These machines mount disks in the form of two RAID arrays, ~500 GB in a Compaq/Digital HSZ50 unit and ~800 GB in a Compaq/Digital HSG80 unit, and an additional 2.8 TB in Fibre Channel JBOD disk. This cluster supports data logging, the ORACLE databases, and general file serving for the remainder of the Online system.

The long-term maintenance of these systems is a serious concern. While they can be expected to still be operational in the Run 2b era, the high availability required for critical system components may be compromised by the inability to obtain the necessary maintenance support. Maintenance costs for these systems, particularly 7x24 coverage, will increase with age. By the time of Run 2b, maintenance costs are likely to rapidly exceed replacement costs.

These systems currently run Compaq Tru64 UNIX, previously known as Digital UNIX, or Digital OSF1. With the pending purchase of Compaq by Hewlett Packard, long term support for this operating system is problematic.

All applications developed for the data acquisition system that currently run on the Host systems were written with portability in mind. In particular, all will work under Linux. The proposed upgrade to the Host systems is therefore to replace them with Linux servers. Since the existing Host system provides data logging, database support, and file serving functions, each of these needs must be accommodated by the replacement system. These requirements will be addressed individually in this and following sections.

The data logging system must, with high (> 99%) availability, be capable of absorbing data from the Level 3 filter systems, distributing it to logging and monitoring applications, spooling it to disk, reading it from disk, and dispatching it to tape-writing nodes in FCC. The required data rate is an open issue—the minimum required is the current 50 Hz @ 0.25 Mbytes/event, but this may increase depending on the ability of the Offline computing systems to process the data. The high availability requirement, satisfied in the current system by using a cluster of three machines, precludes the use of a single machine. The amount of disk required to spool the data, and to act as a buffer if Offline transfers are disrupted, is currently ~2.8 Tbytes. Currently the disk buffers are shared by the cluster members, but this is not a strict requirement.

The proposed upgrade solution is for a set (two or three) of Linux servers (dual or quad processors) to act as the new data logging nodes. The data acquisition applications can run in parallel to distribute the load at full bandwidth, but a single node should be capable of handling nearly the entire bandwidth for running under special conditions. Each system will require gigabit connectivity to the Online switch, thereby raising the number of gigabit ports required.

Some R&D effort is needed to test such a configuration. The possibility of clustering the Linux nodes and the possibility of sharing the disk storage should be examined. A purchase of the complete data logging system can be staged, as not all members need to be identical (as noted above, the current Host system was purchased in three increments). The cost of these systems, which can be spread over several years, is noted in Table 38.

Table 38. Host data logging upgrade cost.

Item	Cost	Schedule
DAQ HOST system R&D	\$40K	2 years @ \$20K per year
DAQ HOST system	\$60K	2 years @ \$30K per year

8.2.4 Control Room Systems

The current DØ control room system is composed of 12 Linux nodes (single and dual processor) that manage 27 monitors. These systems range in age from one to five years. Many of the monitors are already showing the effects of age. It is expected that we should replace some fraction of the control room nodes

and monitors each year. The cost of these replacements, spread out over several years, is noted in Table 39.

Table 39. Control room systems upgrade cost.

Item	Cost	Schedule
Control room systems	\$100K	5 years @ \$20K per year

8.2.5 Data Monitoring Systems

Real-time monitoring of event data is accomplished by a scheme in which representative events are replicated and distributed to monitoring nodes as they are acquired. The monitoring ranges from examination of low-level quantities such as hit and pulse height distributions to complete event reconstruction. In the latter case, the environment and the code are similar to that of the Offline reconstruction farms. There are one or more monitoring applications for each detector subsystem, and for the trigger, luminosity, and global reconstruction tasks.

The rate at which the monitoring tasks can process events, as well as the complexity of monitoring, are limited by the processing capabilities of the monitoring nodes. The Control Room systems and several rack-mounted Linux nodes currently share this load. Much can potentially be gained by upgrading the experiment's monitoring capability. As more sophisticated analysis software becomes available, these improved codes can be run in the Online environment to provide immediate feedback on data quality.

The monitoring nodes, rack mounted Linux systems, should be continually updated. Such upgrades can occur gradually. The cost, including the infrastructure (racks, electrical distribution), is noted in Table 40.

Table 40. Data monitoring upgrade cost.

Item	Cost	Schedule
Monitoring systems	\$100K	5 years @ \$20K per year

8.2.6 Database Servers

The ORACLE databases currently run on the AlphaServer cluster, with the database files residing on the attached RAID arrays. As mentioned above, long-term support for this hardware is questionable. Additionally, ORACLE database and application support from the Computing Division no longer includes the Tru64 UNIX platform.

The principal requirement for the database server is high availability (> 99%). Support needs include maintaining the hardware, the operating system, and the application software (ORACLE). User application development also benefits from having independent production and development database instances.

The planned replacement of the database servers is by two redundant SUN or Linux systems with common access to RAID disk arrays. The Computing Division supports both of these systems. The combined cost of the systems, RAID arrays, and tape backup system is noted in Table 41. The purchase of these systems is best staged over two years, with early purchase of the development machine and later purchase of the production machine.

Table 41. Database server upgrade cost.

Item	Cost	Schedule
Development ORACLE system	\$40K	\$40K purchase
Production ORACLE system	\$60K	\$60K purchase

8.2.7 File Servers

The Host cluster currently provides general-purpose file serving. Linux nodes within the Online system access the Host file systems by NFS. Approximately 500 GB of RAID disk is currently available. Files stored include the DØ software library, Fermilab software products, DAQ configuration files, detector subsystem application data, and user home areas. Since the existing file servers are the AlphaServers, replacement is necessary, for reasons already delineated.

The requirement for the file server system is again high reliability (> 99%) of both system and disks. The proposed solution is a pair of redundant Linux servers with common access to both RAID and JBOD disk arrays, plus access to tape backup devices. Acquisition of these systems can be staged. Table 42 shows the costs.

Table 42. File server upgrade cost.

Item	Cost	Schedule
Primary File Server system	\$20K	\$20K purchase
Backup File Server system	\$20K	\$20K purchase

8.2.8 Slow Control Systems

The Input/Output Controller (IOC) processors for the DØ Online Slow Control system consists of Motorola 68K and PowerPC single-board computers. These nodes perform downloading, monitoring, and calibration functions critical to the operation of the detector. Both of these processor families have limited lifetimes. By the beginning of Run2b, repairs or replacements for the 68K processor boards will no longer be available and, by the end of the run, the same situation may exist for the PowerPC boards as well. Without a change in single-board computer architecture (for example, moving to Intel processors with a significant accompanying software effort) DØ must be able to sustain operation with the existing systems through Run 2b. At the least, a significant number of spare

PowerPC boards – the number based on operational experience – must be purchased and the existing 68K boards in the slow controls system must be replaced.

The functionality of the Muon system 68K processors in the read-out crates is limited by their available memory and memory upgrades are no longer available. Monitoring, control, and calibration functionality would be greatly improved by a complete replacement of these aging processors.

Associated front-end bus hardware, MIL1553 controllers, and rack monitors, are also dependent upon hardware that is no longer available. Spares for these components can no longer be acquired and, since several critical IC chip types are no longer being manufactured, they cannot be repaired. Some devices could be replaced by contemporary systems that employ an Ethernet connection in place of the MIL1553 bus. The existing rack monitors (a general purpose analog and digital signal interface) are prime candidates for such replacement. This would release a number of other MIL1553 components that would then be available for replacement spares. For the remaining MIL1553 devices on the detector platform, reliability would be improved by moving the IOC processors and MIL1553 bus controllers from the Moving Counting House to the platform, thereby eliminating the long runs of the MIL1553 bus cables that have been a significant source of reliability problems.

It is very likely that, by the beginning of Run2b, the operating system on the IOC processors, VxWorks, will no longer be supported at the current level by the Computing Division. The most likely replacement is some version of the Linux system, possibly RT Linux. Conversion of the existing IOC processors to the new operating system, while not requiring significant equipment costs, will involve substantial programming effort. The replacement system must, however, be capable of operating on the existing PowerPC processors.

The replacement of the Muon system processors should take place as soon as possible. The replacement of the 1553 hardware is likely to be spread over many years. The estimate of costs is given in Table 43.

Table 43. Slow control upgrade cost.

Item	Cost	Schedule
Muon processor replacements	\$45K	\$45K purchase
Controls M68K replacements	\$15K	3 years @ \$5K per year
PowerPC spares	\$20K	4 years @ \$5K per year
MIL1553 bus replacements	\$100K	4 years @ \$25K per year

8.3 Procurement Schedule

Table 44 provides a schedule for procurement of the items listed in the above Plan. The fiscal year immediately preceding Run 2b, FY04, will see the greatest

expenditures as the bulk of the production systems are purchased. Other purchases are spread out in time, with the philosophy that the Online components will be gradually updated.

Note that Table 44 does not include normal operational costs of the Run 2a and Run 2b Online computing system. Software and Hardware maintenance contracts, repairs, procurement of spares, hardware and software support of Online group personnel, and consumables will require an additional \$140K per year.

Table 44. Procurement schedule.

WBS	Item	Thousands of \$					Total
		FY02	FY03	FY04	FY05	FY06	
.1.1	Upgrade existing Cisco 6509	\$ 40	\$ 40				\$ 80
.2	Level 3 filter nodes	\$ 50	\$ 50	\$ 50	\$ 50	\$ 50	\$ 250
.3.1	DAQ HOST system R&D	\$ 20	\$ 20				\$ 40
.3.2	DAQ HOST system			\$ 30	\$ 30		\$ 60
.4	Control room systems	\$ 20	\$ 20	\$ 20	\$ 20	\$ 20	\$ 100
.5	Monitoring systems	\$ 20	\$ 20	\$ 20	\$ 20	\$ 20	\$ 100
.6.1	Development ORACLE system		\$ 40				\$ 40
.6.2	Production ORACLE system			\$ 60			\$ 60
.7.1	Primary File Server system				\$ 20		\$ 20
.7.2	Backup File Server system			\$ 20			\$ 20
.8.1	Muon processor replacements	\$ 45					\$ 45
.8.2	Controls M68K replacements		\$ 5	\$ 5	\$ 5		\$ 15
.8.3	PowerPC spares		\$ 5	\$ 5	\$ 5	\$ 5	\$ 20
.8.4	1553 Hardware replacements		\$ 25	\$ 25	\$ 25	\$ 25	\$ 100
Total		\$195	\$225	\$235	\$175	\$120	\$ 950

8.4 Summary

The need to update and replace DØ Online computing equipment is based mainly on the problems associated with the rapid aging and obsolescence of computing hardware. Maintenance costs, particularly 7x24 costs for high availability systems, rapidly approach replacement costs by systems with much greater functionality. Additionally, software support for operating systems and critical applications (ORACLE) is potentially problematic for the platforms currently in use. There is a possible need for higher bandwidth data logging if this can be accommodated by Offline throughput. There are very real benefits to be accrued from more complex trigger filters and data monitoring software. For these reasons, we plan to update and replace the Online systems.

Replacement systems, wherever possible, will be based on commodity Linux solutions. This is expected to provide the best performance at the lowest cost. The Fermilab Computing Division is expected to support Linux as a primary operating system, with full support of local products and commercial applications. We plan to follow a “one machine, one function” philosophy in organizing the structure of the Online system. In this way, less costly commodity processors can replace costly large machines.

9 Summary and Conclusions

The $D\bar{D}$ experiment has an extraordinary opportunity for discovering new physics, either through direct detection or precision measurement of SM parameters. An essential ingredient in exploiting this opportunity is a powerful and flexible trigger that will enable us to efficiently record the data samples required to perform this physics. Some of these samples, such as $p\bar{p} \rightarrow ZH \rightarrow b\bar{b} \nu\bar{\nu}$, are quite challenging to trigger on. Furthermore, the increased luminosity and higher occupancy expected in Run 2b require substantial increases in trigger rejection, since hardware constraints prevent us from increasing our L1 and L2 trigger rates. Upgrades to the present trigger are essential if we are to have confidence in our ability to meet the Run 2b physics goals.

To determine how best to meet our Run 2b trigger goals, a Run 2b Trigger Task Force was formed to study the performance of the current trigger and investigate options for upgrading the trigger. These studies are described in some detail in the previous sections, along with the status and plans for changes in the fiber readout electronics, development of the Level 2 β trigger system, DAQ, and online systems that are needed well before Run 2b. We summarize below the major conclusions of this report.

1. The Analog Front End (AFE) boards used to read out the fiber tracker and preshower detectors require modification to operate with 132 ns bunch spacing. The design of a new daughter board, which would replace the Multi-Chip Modules (MCMs) currently mounted on the AFE boards, is underway. Completion of the AFE modification is critical to our being able to operate with 132 ns bunch spacing.
2. The Level 1 Central Track Trigger (CTT) is very sensitive to occupancy in the fiber tracker, leading to a large increase in the rate for fake high- p_T tracks in the Run 2b environment. The most promising approach to increasing the selectivity of the CTT is to better exploit the existing axial fiber information available to the CTT. Preliminary studies show significant reductions in the rate of fake tracks are achievable by utilizing individual fiber “singlets” in the track trigger algorithm rather than the fiber doublets currently used. Another attractive feature of the fiber singlet upgrade is that the scope is limited to changing the DFEA daughter boards. While further study is needed to optimize and develop an FPGA implementation of the singlet tracking algorithm, the present studies indicate upgrading the current DFEA daughter boards is both feasible and needed to maintain an effective track trigger.
3. The Level 1 calorimeter trigger is an essential ingredient for the majority of $D\bar{D}$ triggers. Limitations in the current calorimeter trigger, which is essentially unchanged from the Run 1, pose a serious threat to the Run 2b physics program. The two most serious issues are the long pulse width of the trigger pickoff signals and the absence of clustering in the jet trigger. The trigger pickoff signals are significantly longer than 132 ns, jeopardizing our ability to

trigger on the correct beam crossing. The lack of clustering in the jet trigger makes it very sensitive to jet fluctuations, leading to a large loss in rejection for a given trigger efficiency and a very slow turn-on. Other limitations include exclusion of ICD energies, inability to impose isolation or HAD/EM requirements on EM triggers, and very limited capabilities for matching tracking and calorimeter information. The proposed upgrade of the L1 calorimeter trigger would allow these deficiencies to be addressed:

- A digital filter would utilize several samplings of the trigger pickoff signals to properly assign energy deposits to the correct beam crossing.
 - Jet triggers would utilize a sliding window to cluster calorimeter energies and significantly sharpen jet energy thresholds.
 - ICD energy would be included in the calorimeter energy measurement to increase the uniformity of calorimeter response.
 - Electron/photon triggers would allow the imposition of isolation and HAD/EM requirements to improve jet rejection.
 - Tracking information could optionally be utilized to improve the identification of electron and tau candidates. Significant improvements in rates for both EM and track-based τ triggers have been demonstrated, but further study is needed to better understand how tracking information could be incorporated into the L1 calorimeter trigger and the cost and resources required.
 - Topological triggers (for example, an acoplanar jet trigger), would be straight-forward to implement.
4. No major changes are foreseen for the Level 1 Muon trigger. Modest upgrades that provide additional scintillator counters in the central region and shielding upgrades may be required for Run 2b. The improvement in background rejection achieved with the fiber singlet track trigger upgrade is probably also needed for the Run 2b muon trigger.
 5. The Level 2 Alpha processor boards have suffered from low yield and poor reliability. The replacement of these processors with L2 β processors is needed to fully deploy the L2 trigger for Run 2a. In addition, we expect to need to upgrade some of the L2 processors for Run 2b. The L2 Silicon Track Trigger (STT) requires additional cards to accept the increased number of inputs coming from the Run 2b silicon tracker.
 6. The Level 3 trigger utilizes a high bandwidth Data Acquisition (DAQ) system to deliver complete event information to the Level 3 processor farm where the Level 3 trigger decision is made. For Run 2b, the DAQ must be able to read out the detector at a rate of 1 kHz with a high degree of reliability. DØ is in the process of commissioning its Run 2a DAQ system based on custom hardware that provides the high-speed data paths. We are also exploring an alternative approach based on commercial processors and network switches. Maintaining Level 3 trigger rejection as the luminosity increases will require

increasing the processing power of the L3 processor farm as part of the upgrade to the online system.

7. The online computing systems require upgrades in a number of different areas. These upgrades are largely needed to address the rapid aging and obsolescence of computing hardware. We anticipate upgrading our networking infrastructure, L3 farm processors, the online host system, control and monitoring systems, database and file servers, and the 1553 slow control system.

9.1 Cost Summary for Trigger Completion and Upgrades

In the two tables below, we present a summary of the preliminary cost of the trigger projects being proposed here. We segment the projects into two categories: those covering the completion of and upgrades to the detector for data taking prior to Run 2b, and those addressing the preparations for Run 2b and beyond. The estimates do not include manpower.

At Level 1, we propose option 2 for the SIFT replacement, as we believe there to be less technical risk associated with this option than with the version requiring removal of the MCMs from the existing AFEs boards. We are also proposing an upgrade to the calorimeter trigger for Run 2b, which is included in Table 46 below. As mentioned above, we believe that further study is needed before a specific proposal that track information be incorporated into the Level 1 calorimeter trigger can be made. We therefore exclude it from financial consideration here, pending completion of our studies later this calendar year. The studies performed here suggest that an upgrade to the track trigger in which fiber singlet information is integrated at Level 1 will offer significant gains in rejection. In light of what these initial studies have demonstrated, we include the projected cost of this improvement in Table 46. Because it offers more processing power, and does not require the invasive and technically risky process of removing FPGAs from the existing daughter boards, we have chosen the option in which the daughter boards are replaced. Both of these upgrades are being targeted for FY03 and FY04.

The dominant portion of the funds required for the Level 2 β system is earmarked for the Run 2a system, which will be completed within the next calendar year. These funds will therefore be needed in FY02. Taking into account the \$192k in funding that has already been identified, completion of the Run 2a Level 2 β project requires a total of \$370k. In anticipation of a partial upgrade of the Level 2 trigger system for Run 2b – in particular, the handling and processing of information from the track trigger and possibly the Silicon Track Trigger – we include in Table 46 a line item corresponding to a processor upgrade of 12 of the 24 Level 2 β boards. In addition, we note that the funds for the upgrade of the STT for Run 2b are requested in FY02. This is to allow us to exploit significant gains in time and money by piggybacking on the Run 2a STT production run in early CY02. Obsolescence of some of the processors over the next three years is also a concern; these will be purchased for both the baseline and upgraded STT in FY02 as well.

As noted in Section 7.1.4, our baseline data acquisition system is financially covered in the original Run 2a cost estimate, with most (more than 80%) of the money for the DAQ having already been obligated. We therefore do not include a cost for that system below. We consider the risk associated with the delivery of this system to be substantial enough that we include the estimated cost for the commercial DAQ option in Table 45 below. Should this option be pursued, we anticipate that the bulk of the money will be needed in FY02, with some limited complementary portion required in early FY03.

An estimated total of \$950k is needed to cover yearly project-related upgrades to the online system for the five year period spanning FY02 through FY06, inclusive. These upgrades include the LINUX filter farm for the Level 3 trigger, the slow controls system, etc. We assume here that this money will come out of the operating budget - pending final discussions with the Laboratory - and therefore do not include this sum in the tables below, which represent estimates for equipment expenditures. We note that this money for online upgrades is requested in addition to the yearly operating allocation for online support for DØ operations.

Table 45. Preliminary cost estimate to complete trigger sub-projects required prior to Run 2b. Total includes secondary (commercial) DAQ option. Manpower is not included. * Rows corresponding to Level 2β and TOTAL include the \$192k in funds already identified for the Level 2β sub-project.

Sub-Project	M&S (\$k)	Contingency (%)	Total (\$k)	Fiscal Year Needed
SIFT Replacement (Option 1)	688	46	1001	FY02-03
Level 2β*	411	37	562	FY02
Commercial DAQ system	449	50	675	FY02-03
<i>TOTAL</i> *	<i>\$1,455</i>		<i>\$2,238 (incl. DAQ option)</i>	

Table 46. Preliminary cost estimate for projects associated with detector upgrades for Run 2b. Manpower is not included.

Sub-Project	M&S (\$k)	Contingency (%)	Total (\$k)	Fiscal Year Needed
Level 1 Calorimeter Trigger	726	100	1,452	FY03-04
Level 1 Track Trigger	360	50	540	FY03-04
Level 2 β	62	34	83	FY03-04
Level 2 Silicon Track Trigger	392	40	549	FY02
<i>TOTAL</i>	<i>\$1,540</i>		<i>\$2,624</i>	

A DØ Run 2b Trigger Task Force

A.1 Task Force Charge

The Run 2b Trigger Task Force is charged with developing a plan for a Run 2b trigger system that allows DØ to run at 132 nsec, and a luminosity of 5×10^{32} , with the following output trigger rates:

L1: 5 kHz

L2: 1 kHz

L3: 50 Hz.

The upgraded trigger system will ideally allow DØ to run with a full complement of triggers, thereby spanning the space of physics topics available in Run 2b. It should be ready for installation at DØ by the summer of 2004, and must remain within reasonable bounds in terms of cost, technical resources, development and production time, and the impact on the existing detector. The addition of new tracking detectors, a greatly expanded cable plant, or significant additions to the number of crates in the Movable Counting House are examples of options that will in all probability not be feasible, given the time, manpower and hardware constraints that we are facing. The Task Force should take such constraints into consideration as it explores the various options.

The tight time constraints the Task Force is facing will in all probability not allow them to consider the full suite of possible Run 2b triggers. They should therefore consider focusing on the essential elements of the Run 2b high- p_T physics program, of which the Higgs search is of paramount importance. The bandwidth requirements and trigger efficiencies that result from the implementation of the available technical solutions, applied to provide the needed rejection, should be estimated.

To guide their work in the relatively short time that is available, the Task Force may assume that the most extensive upgrade is likely to be needed at Level 1. Feasibility arguments for upgrades to the higher trigger levels - which may be based on expected improvements in processing power, for example - might be sufficient, depending on what is learned during their studies. Should their investigations indicate that more extensive upgrades at Levels 2 or 3 (i.e., board replacements, etc.) will be needed, however, they should outline this in a more comprehensive manner in their report.

The Task Force should submit a Conceptual Design Proposal that lists the proposed upgrades to the Run 2b Project Manager by September 17, 2001. These recommendations should be supported by physics simulations, and include an estimate of the financial and technical resources required, an outline of the expected schedule for delivery, and the impact on the existing detector infrastructure.

A.2 Trigger Task Force Membership

Brad Abbott, Maris Abolins, Drew Alton, Levan Babukhadia, Drew Baden, Vipin Bhatnagar, Fred Borcharding, John Butler, Jiri Bystricky, Sailesh Chopra, Dan Edmunds, Frank Filthaut, Yuri Gershtein, George Ginther, Ulrich Heintz, Mike Hildreth (co-chair), Bob Hirosky, Ken Johns, Marvin Johnson, Bob Kehoe, Patrick Le Du, Jim Linnemann, Richard Partridge (co-chair), Pierre Petroff, Emmanuelle Perez, Dean Schamberger, Kyle Stevenson, Mike Tuts, Vishnu Zutshi

B Level 2β and Level 2 STT Cost Estimates

The cost estimates for that portion of the Level 2β project associated with the completion of the Run 2a detector, and the Run 2b upgrade to the L2 STT, are shown in the spreadsheets below. Our current estimates of the engineering needs for each are included.

Table 47: Cost estimate for the Run 2a Level 2β project. Engineering is included.

WBS	2.1	Title		MATERIALS & SERVICES (M&S)		CONTINGENCY		TOTAL Cost	Sources of Funds						
		ITEM		Unit	M&S Cost	%	Cost		Spent to date	EIC	Fermi Orsay	Fermi Prototype	Fermi 2a	Fermi 2b	Total
2.1.1		<i>Motherboard</i>			243,489	28	68,131	311,621	74,417	169,072	138,328	27,000	0	0	165,328
2.1.1.1		Engineering and Design			131,415	3	3,425	134,840	64,415	67,000	128,415	3,000	0	0	131,415
2.1.1.1.1		Exploratory Design (Maryland)	lot	1	3,000	0	0	3,000	3,000	0	0	3,000	0	0	3,000
2.1.1.1.2		Design and schematics (Orsay)	yr	0.7	100,000	0	0	70,000	50,000	20,000	70,000	0	0	0	70,000
2.1.1.1.3		PCB Layout (Orsay)	yr	0.17	100,000	0	0	17,000	17,000	0	17,000	0	0	0	17,000
2.1.1.1.4		Mechanical Engineering (Thales)	lot	1	11,415	30	3,425	14,840	11,415	0	11,415	0	0	0	11,415
2.1.1.1.5		Testing and Commissioning (Orsay)	yr	0.30	100,000	0	0	30,000	0	30,000	30,000	0	0	0	30,000
2.1.1.2		Setup Engineering by Assembler (Thales)			6,032	50	3,016	9,048	0	6,032	0	6,500	0	0	6,500
2.1.1.2.1		PC Board	lot	1	1,974	50	987	2,961	0	1,974	0	0	0	0	0
2.1.1.2.2		Assembly	lot	1	1,958	50	979	2,937	0	1,958	0	0	0	0	0
2.1.1.2.3		Testing	lot	1	2,100	50	1,050	3,150	0	2,100	0	0	0	0	0
2.1.1.3		Prototype Board			-4,335	100	17,339	34,679	10,002	7,337	9,913	17,500	0	0	27,413
2.1.1.3.1		PC Board	ea	4	1,245	100	4,981	9,416	0	4,435	0	0	0	0	0
2.1.1.3.2		Assembly	ea	4	168	100	672	5,653	0	4,981	0	0	0	0	0
2.1.1.3.3		Testing	ea	4	68	100	273	945	0	672	0	0	0	0	0
2.1.1.3.4		Mechanical parts	ea	4	1,109	100	4,435	4,708	4,435	-4,162	4,435	0	0	0	4,435
2.1.1.3.5		BGAs	ea	5	813	100	4,067	8,133	4,067	4,067	4,067	0	0	0	4,067
2.1.1.3.6		Other Components	ea	5	282	100	1,411	2,822	0	1,411	1,411	0	0	0	1,411
2.1.1.3.7		Connectors	ea	4	375	100	1,500	3,000	1,500	0	0	0	0	0	0
2.1.1.4		Production Board			2,334	50	88,703	133,054	0	88,703	0	0	0	0	0
2.1.1.4.1		PC Board	ea	38	672	50	12,760	24,447	0	11,687	0	0	0	0	0
2.1.1.4.2		Assembly	ea	38	170	50	3,232	28,752	0	25,520	0	0	0	0	0
2.1.1.4.3		Testing	ea	38	32	50	599	7,062	0	6,464	0	0	0	0	0
2.1.1.4.4		Mechanical parts	ea	42	278	50	5,843	7,040	0	1,197	0	0	0	0	0
2.1.1.4.5		BGAs	ea	42	809	50	16,979	50,936	0	33,957	0	0	0	0	0
2.1.1.4.6		Other Components	ea	42	235	50	4,939	14,818	0	9,878	0	0	0	0	0
2.1.1.4.7		Connectors	ea	42	0	50	0	0	0	0	0	0	0	0	0
2.1.2		<i>Processors</i>			129,523	49	63,050	192,573	14,389	115,134	3,513	23,000	0	0	26,513
2.1.2.1		Prototypes			23,651	43	10,114	33,765	14,389	9,262	3,513	23,000	0	0	26,513
2.1.2.1.1		VVIC processor	ea	1	3,423	0	0	3,423	0	3,423	0	0	0	0	0
2.1.2.1.2		CPCI Crate	ea	1	3,375	50	1,688	5,063	3,375	0	0	0	0	0	0
2.1.2.1.3		CPCI Crate Equipment	lot	1	565	50	283	848	565	0	0	0	0	0	0
2.1.2.1.4		Advantech SBC	ea	4	3,513	50	7,026	21,078	7,026	7,026	3,513	0	0	0	3,513
2.1.2.1.5		Heat Sink Modification	ea	4	125	50	250	750	0	500	0	0	0	0	0
2.1.2.1.6		Disk Drive	ea	4	200	50	400	1,200	0	800	0	0	0	0	0
2.1.2.1.7		2nd CPU Chip	ea	4	234	50	468	1,404	0	936	0	0	0	0	0
2.1.2.2		Production Boards			4,072	50	52,936	158,808	0	105,872	0	0	0	0	0
2.1.2.2.1		Advantech SBC	ea	26	3,513	50	45,669	137,007	0	91,338	0	0	0	0	0
2.1.2.2.2		Heat Sink Modification	ea	26	125	50	1,625	4,875	0	3,250	0	0	0	0	0
2.1.2.2.3		Disk Drive	ea	26	200	50	2,600	7,800	0	5,200	0	0	0	0	0
2.1.2.2.4		2nd CPU Chip	ea	26	234	50	3,042	9,126	0	6,084	0	0	0	0	0
2.1.3		<i>Maintenance Facilities</i>			38,400	50	19,200	57,600	0	38,400	0	0	0	0	0
2.1.3.1		VIPA Crate	ea	2	5,000	50	5,000	15,000	0	10,000	0	0	0	0	0
2.1.3.2		Mbus Backplane	ea	2	500	50	500	1,500	0	1,000	0	0	0	0	0
2.1.3.3		Mbus Terminators	ea	4	100	50	200	600	0	400	0	0	0	0	0
2.1.3.4		Power	ea	2	5,000	50	5,000	15,000	0	10,000	0	0	0	0	0
2.1.3.5		Bit3 Interface	ea	2	4,000	50	4,000	12,000	0	8,000	0	0	0	0	0
2.1.3.6		Control PC	ea	2	2,000	50	2,000	6,000	0	4,000	0	0	0	0	0
2.1.3.7		Test Equipment	ea	2	2,500	50	2,500	7,500	0	5,000	0	0	0	0	0
2.1		Level 2 Beta Processor 2a			411,412	37	150,381	561,794	88,806	322,606	141,841	50,000	0	0	191,841

Table 48: Cost estimate for the Run 2b Level 2 STT upgrade. Engineering is included.

WBS 2.2		Title						
WBS 2.2	ITEM Level 2 STT Upgrade	MATERIALS & SERVICES (M&S)				CONTINGENCY		TOTAL Cost
		Unit	#	Unit Cost	M&S TOTAL	%	Cost	
2.2.1	<i>Boards (more of existing types)</i>				275,755	37	103,288	379,043
2.2.1.1	Motherboard	ea	32	2,000	64,000	30	19,200	83,200
2.2.1.2	STC Logic Board	ea	20	2,500	50,000	30	15,000	65,000
2.2.1.3	Link Transmitter Board (LTB)	ea	52	200	10,400	30	3,120	13,520
2.2.1.4	Link Receiver Board (LRB)	ea	33	550	18,150	30	5,445	23,595
2.2.1.5	Buffer Controller Board (BC)	ea	32	950	30,400	30	9,120	39,520
2.2.1.6	VME Transition Module (VTM)	ea	20	2,500	50,000	50	25,000	75,000
2.2.1.7	Track Fit Card (TFC)	ea	8	5,000	40,000	50	20,000	60,000
2.2.1.8	Board Testing	ea	197	65	12,805	50	6,403	19,208
2.2.2	<i>Link Echo Board</i>				48,290	49	23,807	72,097
2.2.2.1	Design & Prototyping	hours	960	35	33,600	50	16,800	50,400
2.2.2.2	Production	ea	26	500	13,000	50	6,500	19,500
2.2.2.3	Testing	ea	26	65	1,690	30	507	2,197
2.2.3	<i>Software & Firmware changes</i>				33,600	50	16,800	50,400
2.2.3.1	STC	hours	960	35	33,600	50	16,800	50,400
2.2.4	<i>J3 Backplane</i>				15,131	41	6,266	21,397
2.2.4.1	Design & Layout	lot	1	5,000	5,000	50	2,500	7,500
2.2.4.2	Setup for production	lot	1	1,500	1,500	30	450	1,950
2.2.4.3	Backplanes	ea	10	500	5,000	30	1,500	6,500
2.2.4.4	Connectors	ea	10	363	3,631	50	1,816	5,447
2.2.5	<i>Cables</i>				18,950	35	6,675	25,625
2.2.5.1	LVDS	ea	165	30	4,950	50	2,475	7,425
2.2.5.2	Splitters	ea	80	125	10,000	30	3,000	13,000
2.2.5.3	Fibers	ea	160	25	4,000	30	1,200	5,200
2.2	Level 2 STT Upgrade				391,726	40	156,835	548,561