



Update on DØ Run 2b Plans

The DØ Collaboration

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Prepared for the June 2001 meeting of the Fermilab PAC

Introduction

We are pleased to provide the laboratory and PAC with an update on our Run 2b plans. Since the April PAC meeting, there has been progress on a number of fronts. We have begun to put in place the Run 2b project management team, have actively worked with the Run 2b task force and cost review committees to answer their questions, have explored various options for the silicon tracker design, and are working to better define our plans for trigger upgrades.

In the sections below, we describe the project management that is being put in place and update our upgrade plans for the Silicon Tracker and Trigger. In this document, we have focused on describing the changes and new developments since the April PAC meeting; documentation on the material previously presented can be found at:

http://d0server1.fnal.gov/projects/upgradeproject/run2b/pac_april2001/pac_april2001.html.

Project Management

Much of the upper tier of the DØ Run 2b project management has been put in place since the last PAC review. Jonathan Kotcher from Brookhaven National Laboratory has been chosen by the experiment to manage the project. His selection has been approved by the Fermilab Directorate. The Project Manager has chosen Richard Partridge from Brown University to serve as Deputy Project Manager for the upgrade, with a term of one year. Marcel Demarteau from Fermilab will serve as Sub-Project Manager for the silicon sub-project.

A proposal for the organizational sub-structure of the silicon sub-project has been developed, and internal discussions related to the specific personnel assignments are well underway. At the moment, we expect the silicon sub-project to be divided into five sub-areas: mechanical, sensors, electronics, production, and testing and quality assurance. Another task devoted to simulation efforts may be added. The DØ Run 2b Project Manager and the silicon Sub-Project Manager will also choose a Deputy Project Manager for the silicon who, like the Deputy Project Manager, will serve for a term of

one year. Specific individuals who have been chosen to oversee various sub-project tasks will be announced after their appointments have been discussed sufficiently within D0. We expect most of these appointments to be finalized within the next two weeks.

Besides the silicon tracker replacement, the other primary branch of the upgrade is the trigger improvements needed to handle the increase in luminosity for Run 2b. As is described elsewhere in this document, we are currently in the process of defining the specifics of this portion of the upgrade. The organizational sub-structure of the trigger sub-project, and the individuals who might be chosen to manage the various sub-tasks, is under active discussion within the collaboration. This will be finalized as the scope of this portion of the project is more clearly defined.

An understanding of the role, charge, and scope of responsibility of each of the principals chosen to lead the various portions of the upgrade project has been reached between the relevant parties. More detailed descriptions of these and other roles will be contained in writing in the Project Management Plan, which is being prepared.

Run 2b Silicon Tracker

Silicon Tracker Overview

The silicon tracker design has evolved since the April 2001 PAC meeting. Changes have been made in response to comments from the meeting, discussions with the silicon task force, and as a part of the natural development of the April design. Plan views of the tracker region illustrating some of the changes are shown in Figs. 1-2.

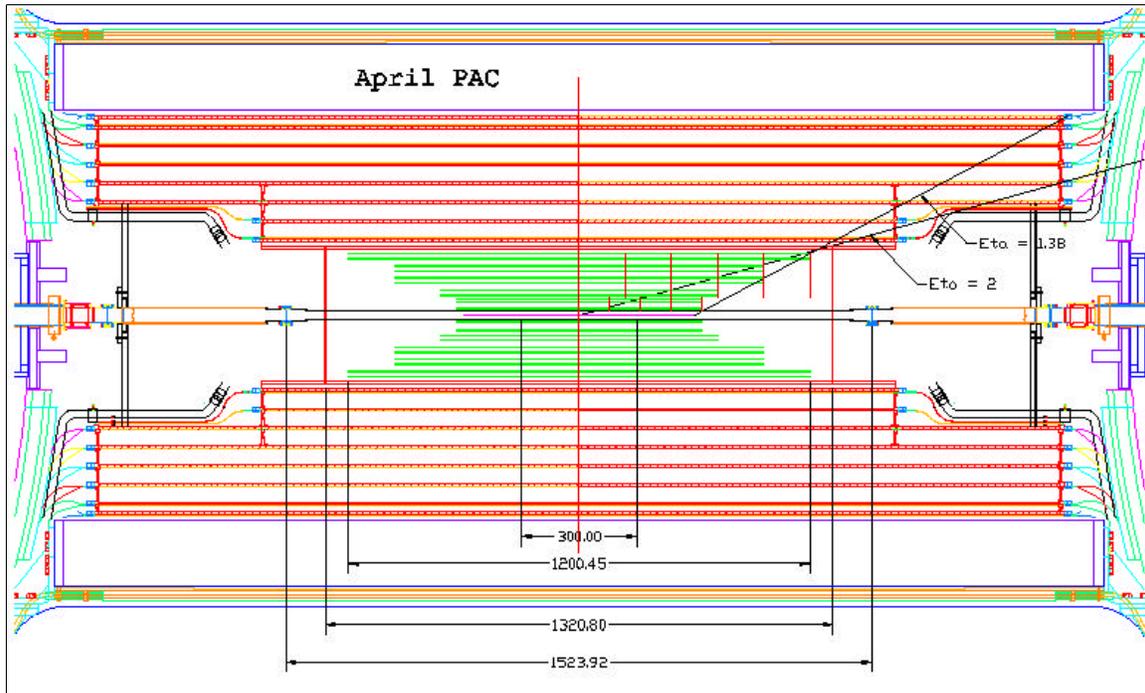


Figure 1: Plan view from the April PAC meeting. Red lines in the upper right quadrant indicate the ends of sensors.

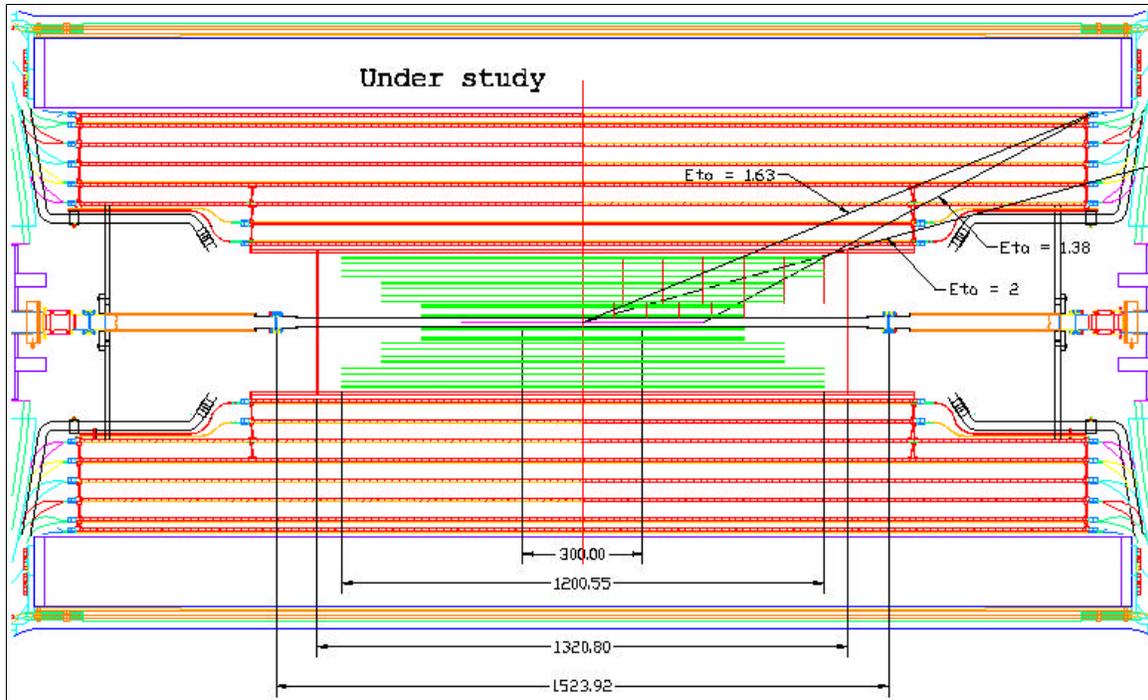


Figure 2: Plan view of the arrangement presently under study. Red lines in the upper right quadrant indicate the ends of sensors.

Tracker Geometry

The $r\text{-}\phi$ geometric arrangement of silicon sensors remains essentially unchanged from the design shown at the April 2001 PAC meeting, but several changes have been made in the $r\text{-}z$ arrangement. These changes are described below.

Sensor lengths in layers 2 through 5 have been reduced from 120 mm to 100 mm to take into account improved knowledge of the fabrication requirements of potential manufacturers. We now assume that the pair of sensors from a 150 mm wafer must fit within a circle of diameter 136 mm on the wafer. Sensor lengths in layers 0 and 1 remain unchanged at 80 mm.

We have increased the length of several layers to better match the expected luminous region based on information we received from the Beams Division¹ and the possibility that the Tevatron Electron Lens project would eliminate the need for a crossing angle. An effective luminous region of extent $\pm 2\sigma$ with $\sigma = 150$ mm is shown in Figs. 1-2. The geometric acceptance of the new tracker layout with (without) a crossing angle is shown in Fig. 3 (4).

To allow space between SVX4 chips for possible bypass capacitors and power/ground connections at the front of the chip, designs have been studied in which the sensor readout pitch has been increased from 55 μm to 60 μm in layers 2 through 5. We have concentrated our stave design efforts on Proposal B of the PAC document, that is, on the design with central, rather than edge, cooling. That design should allow a modest (15% to 20%) reduction in the number of radiation lengths represented by a stave. It also allows the sensors to be slightly wider, providing the space needed for 60 μm readout pitch. Studies of heat transfer, stave deflections, and thermal bowing are in progress.

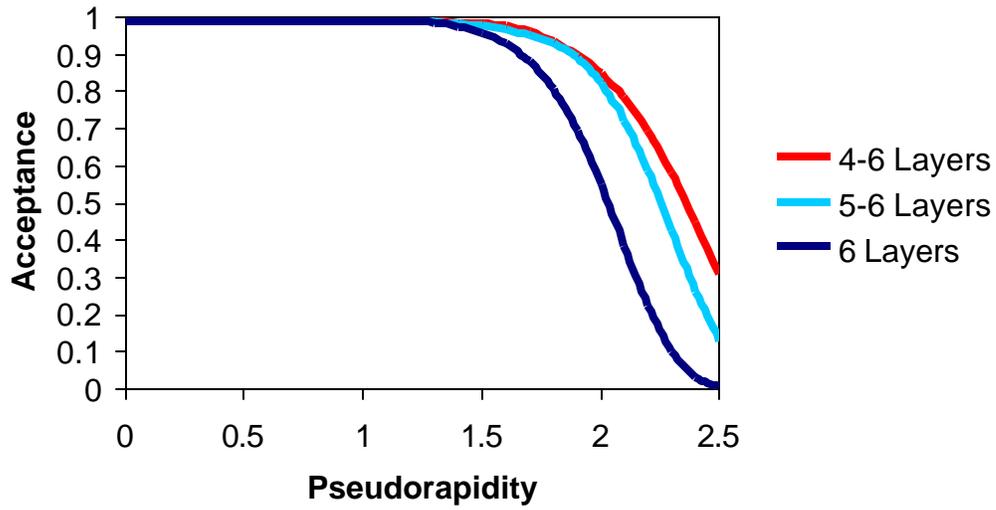


Figure 3: Silicon tracker acceptance for a 136 μrad crossing angle ($\sigma_z = 150$ mm).

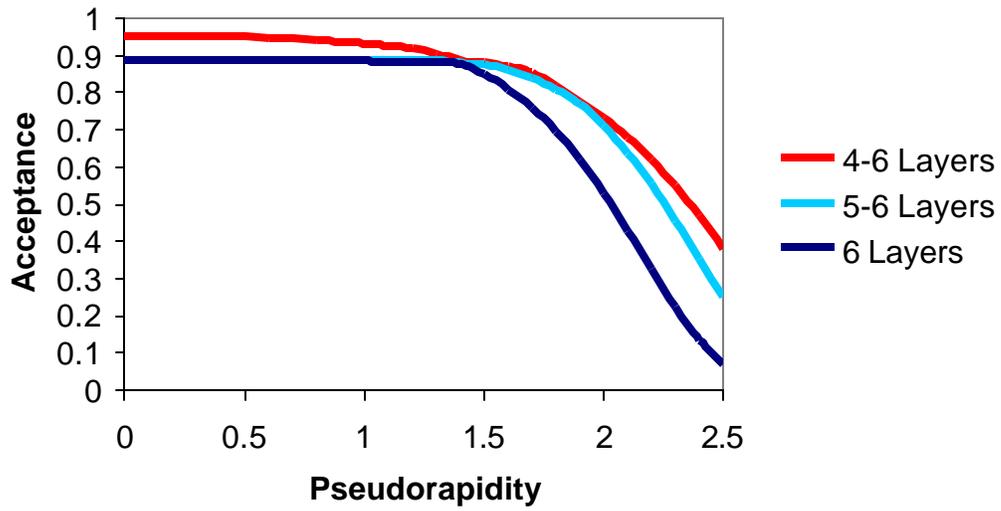


Figure 4: Silicon tracker acceptance for no crossing angle ($\sigma_z = 250$ mm).

The geometric arrangement of sensors considered in April and the arrangement presently under study are summarized in Tables 1-2 below.

Layer	Radius (mm) (approximate)	Axial/ stereo	Sensor W x L	# Phi	# Z	Readout pitch (mm)	Active surface (m ²)
0a	15	A	1 chip x 80 mm	6	8	.050	.024
0b	18	A	2 chips x 80 mm	6	8	.050	.047
1	34	A	2 chips x 80 mm	18	8	.050	.142
2	63	A+S	5 chips x 120 mm	12	6	.055	.593
3	97	A+S	5 chips x 120 mm	18	8	.055	1.186
4	129	A+S	5 chips x 120 mm	24	8	.055	1.581
5	160	A+S	5 chips x 120 mm	30	10	.055	2.471
						Total	6.045

Layer	Radius (mm) (approximate)	Axial/ stereo	Sensor W x L	# Phi	# Z	Readout pitch (mm)	Active surface (m ²)
0a	15	A	1 chip x 80 mm	6	10	.050	.030
0b	18	A	2 chips x 80 mm	6	10	.050	.059
1	34	A	2 chips x 80 mm	18	10	.050	.177
2	63	A+S	5 chips x 100 mm	12	10	.060	.896
3	97	A+S	5 chips x 100 mm	18	10	.060	1.344
4	129	A+S	5 chips x 100 mm	24	12	.060	2.151
5	160	A+S	5 chips x 100 mm	30	12	.060	2.689
						Total	7.346

While not evident in the figures and tables, we have investigated longitudinal ganging whereby two (or possibly three) sensors in the outer layers are wire-bonded together to increase the effective sensor length. Longitudinal ganging allows us to redistribute readout channels and decrease the number of readout cables and channels required. Ganging sensors longitudinally implies longer sensor modules and a decrease in the maximum achievable stereo angle for these sensors. We are actively investigating several different options for longitudinal ganging and hope to decide on a particular option in the near future.

Longitudinal ganging has several advantages over increased readout pitch as a means for reducing readout resources. Due to charge sharing, nearby tracks need to be separated by several readout strips to be cleanly reconstructed. Figure 5 shows that charged tracks from B hadron decays frequently have other charged tracks nearby, and that the probability of another hit on a nearby readout strip is a strong function of the strip pitch. These nearby tracks are predominantly from other tracks within the same jet as the B, with the probability of another nearby hit being a factor of 2-3 higher than would be predicted for random occupancy. These studies indicate that longitudinal ganging in the outer layers is preferable to a wider strip pitch for a given number of readout channels (a 10 cm long sensor in the outer layer covers a rapidity interval of ~ 0.6 , which is larger than the core of a jet). We also see from Fig. 5 that there is a substantial probability that hits in L0-1 will not be cleanly resolved. These layers play a dominant role in determining the impact parameter resolution. With 60 μm readout pitch in L2-5, we can measure these tracks in a relatively clean environment that will aid in the recovery of confused tracks in the inner layers.

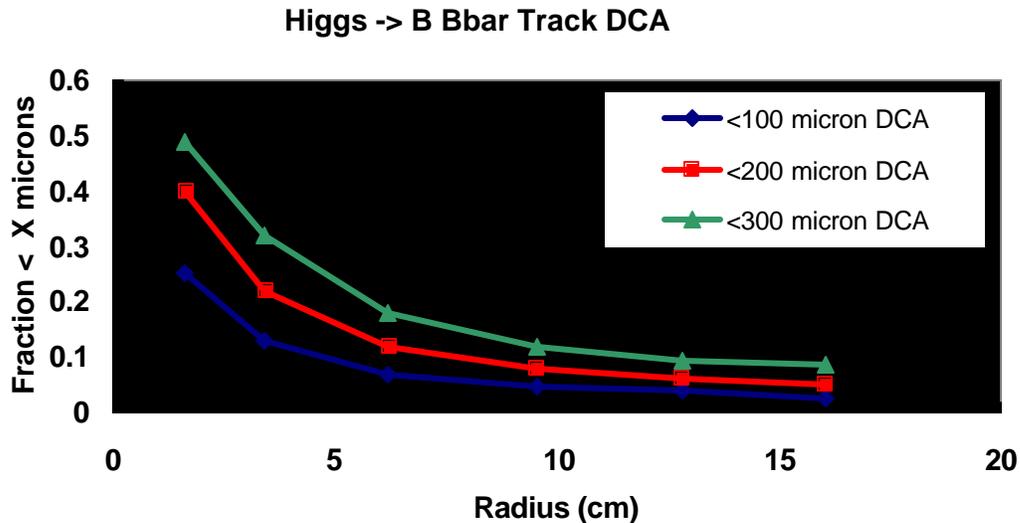


Figure 5: Fraction of time another track has a distance of closest approach (DCA) within 100, 200, or 300 μm of a track from B hadron decays in Higgs events.

We also note that space constraints appear to require mounting the hybrids for the outer layers directly on the sensors. Thus, we can bond the strips directly to the SVX4 chips provided the readout pitch is no more than $\sim 60 \mu\text{m}$. As a result, the incremental cost of reading out on a fine pitch is small; the SVX4 chips are relatively inexpensive,

while the number of hybrids, readout cables, and downstream electronics modules isn't affected. Finally, we find that keeping a narrow pitch and utilizing intermediate strips leads to significant improvements in momentum resolution for stand-alone silicon tracking (needed for $|\eta| > 1.6$) and r-z impact parameter measurements (see below).

Silicon Sensors

Our current designs feature three types of silicon sensors: 1 chip and 2 chip wide 80 mm long sensors with 50 μm readout pitch in L0-1 and 5 chip wide 100 mm long sensors with 55-60 μm readout pitch in L2-5. Our working assumption is that intermediate strips will be used in all layers, with the strip pitch half the readout pitch. The use of intermediate strips in L0-1 improves the expected impact parameter resolution in r ϕ , while their use in L2-5 improves the momentum resolution for silicon-only tracking in the forward region where we have a limited lever arm and the r -z impact parameter obtained from the stereo layers. To quantify these effects, we have calculated the effect of reducing the hit resolution from 10 μm to 6 μm : the r - ϕ impact parameter resolution for 2 GeV tracks decreases from 20 μm to 16 μm , the r -z impact parameter for 2 GeV $\eta=0$ tracks decreases from 367 μm to 264 μm for a 2° stereo angle, and the p_T where we can make a 3σ charge determination with silicon-only tracking increases from 55 GeV to 81 GeV.

Radiation studies of sensors from a variety of manufacturers are in progress. All devices are still working after 5 MRad, and we will continue to increase the dose these chips receive to understand how they would perform over the course of Run 2b. These studies are particularly focused on characterizing the performance of possible L0-1 devices, which must withstand ~ 1 MRad/fb⁻¹. Mask development for additional L0-1 prototypes is being done at Moscow State University for fabrication at ELMA, and discussions are underway with a variety of possible sensor vendors. We have also performed radiation tests of the various Run 2a sensors, and confirmed a probable lifetime of ~ 2 MRad.

Readout Electronics

The tracker readout electronics is based on using SVX4 chips to digitize signals from the silicon sensors, while maintaining compatibility with the current DAQ architecture. Since the SVX4 operates with 2.5V power rails, we must convert our present 5V plant for Run 2a so that it will function with the lower voltages. Aside from changes required to operate with 2.5V levels, our plan is to reuse as much of the current Run 2a cable and readout plant as possible.

We have been working with CDF and the SVX chip designers to develop SVX4 specifications and ensure that the chip will meet DØ's needs. We expect that this process will result in a single chip with a common pad ring that meets the needs of both CDF and DØ. The layout of the pad ring will be finalized in the near future, allowing us to begin hybrid design and plan for the entire readout chain. Submission of a complete prototype of the SVX4 chip is expected this fall.

The hybrids on layers 2-5 will have five SVX4 chips on each end, so that two sensor assemblies can be bonded to a single hybrid. In order to facilitate the 5V to 2.5V bi-directional conversions, we expect to include a radiation hard transceiver chip on each hybrid. These chips are already in hand and studies of their characteristics are underway. A single readout cable is used to connect the hybrid to the DAQ system.

Layers 0-1 are similar to layers 2-5 except that they use flex circuits to bring the sensor signals to the SVX4 chips and have fewer chips per hybrid. We have made a visit to a possible vendor for the flex cables, Dyconex in Zurich, and anticipate placing a prototype order with them in the near future.

We expect that the present adapter cards, which are mounted on the calorimeter and currently contain only passive components, will need to be replaced with new cards that have active power regulation components. While we expect to retain the cables connecting the adapter cards to the DAQ, we are working to better understand the required cable plant between the hybrids and adapter cards and determine if we can use the existing low-mass cables to connect the tracker to the adapter cards.

A strong constraint on the tracker design is imposed by the number of readout cables coming out of the tracker. Due to space limitations for feeding cables through the detector and crate space limitations on the detector, there is essentially no room for expansion beyond the ~900 cables currently in use.

Trigger Upgrades

Overview of trigger

The basic trigger philosophy from Run 2a will be maintained in Run 2b. The Run 2a trigger has three levels that progressively reduce the trigger rate to a manageable level. Level 1 is a detector specific trigger, which uses fast information from the Fiber Tracker, Central Preshower, Calorimeter, and Muon systems. The information from each of these systems is treated and used independently, except for the muon system, which uses the tracking results from the Fiber Tracker. Level 1 is a deadtime-less hardware trigger and a decision is reached after 4.2 μ sec. At Level 2, all Level 1 information is available and correlations between different detectors can be used to further reduce the trigger rate. The trigger data is collected and processed by an array of specialized processors and a decision is made in a global processor. An impact parameter trigger utilizing silicon tracker hits will be available in the summer of 2002. The time scale for a decision in Level 2 is 100 μ sec. Once an event is accepted at Level 2, all data are read out and made available to an array of PC's that run filters, similar to the offline code, but optimized for speed and efficiency. The time scale for a decision in Level 3 is 100 msec. The output rates of Levels 1, 2, and 3 are expected to be 5-10 kHz, 1 kHz, and 20-50 Hz, respectively.

Proposals for Run 2b

The Run 2b trigger must accommodate an increase of ~2.5 in instantaneous luminosity, as well as increased occupancy in the detectors. Our maximum Level 1 trigger rate will continue to be limited to 5-10 kHz by SVX deadtime, since we must run the SVX4 in SVX2 mode to maintain compatibility with our existing DAQ infrastructure. Thus, we must increase our Level 1 trigger rejection by at least a factor of 2.5 over what is planned for Run 2a.

There are currently several proposals for upgrades of the DØ trigger system under study. However, we have not yet considered these proposals in a comprehensive and integrated way that takes into account the need for a balanced trigger that is efficient in triggering on the key Run 2b physics processes while meeting our rate limitations in the high-occupancy Run 2b environment. We are in the process of establishing a Run 2b Trigger Task Force that will bring a strong focus to these issues, culminating in the

submission of a Run 2b Trigger Conceptual Design Report to the collaboration in mid-September.

The proposals for upgrading the trigger include:

- 1) The present fiber/preshower electronics boards that provide both signal digitization and trigger discriminators will not operate at 132 ns bunch crossing times. We have decided to replace the daughter cards that house the discriminator and digitizer chips with new cards based on an analog pipeline and flash ADC encoding of signals, controlled by new generation FPGAs. This redesign uses many of the elements of the SVX4 and other recent ASIC designs, and will ameliorate nonlinearities and clock noise inherent in the current digitizers. The new daughter cards will be pin-compatible with the old ones, so that the main front end analog boards and cable plant can be retained.
- 2) Since a large fraction of our triggers are based at least in part on calorimeter measurements, an upgrade of the Level 1 calorimeter trigger that was originally designed to meet Run 1 requirements is a particularly attractive option. We would then be able to replace our fixed jet tower size ($\Delta\eta \times \Delta\phi = 0.2 \times 0.2$) by a sliding window algorithm, which is similar to what is being proposed for the ATLAS calorimeter trigger. Such an algorithm is well established and results in sharper turn on curves for triggering on jets. We have started to simulate this trigger and the results are illustrated in Figs. 67 below. These preliminary results show that jet trigger rates can be reduced by a factor of 3-5 for high p_T jets, which is roughly in line with what is needed for Run 2b. A full simulation of trigger rates resulting from such a trigger has not yet been performed. However, given the steeply falling jet spectra as a function of transverse jet energy, it is clear that this trigger will greatly enhance triggering on jets, which is an important element in a wide variety of high- p_T triggers including $ZH \rightarrow \nu\nu b\bar{b}$. The upgrade would also improve triggering on electromagnetic objects by clustering neighboring towers and providing the option of imposing isolation, EM energy fraction, and tight track matching requirements. The Saclay group is trying to establish engineering support to build a first prototype. This is the most advanced of the trigger upgrade proposals.

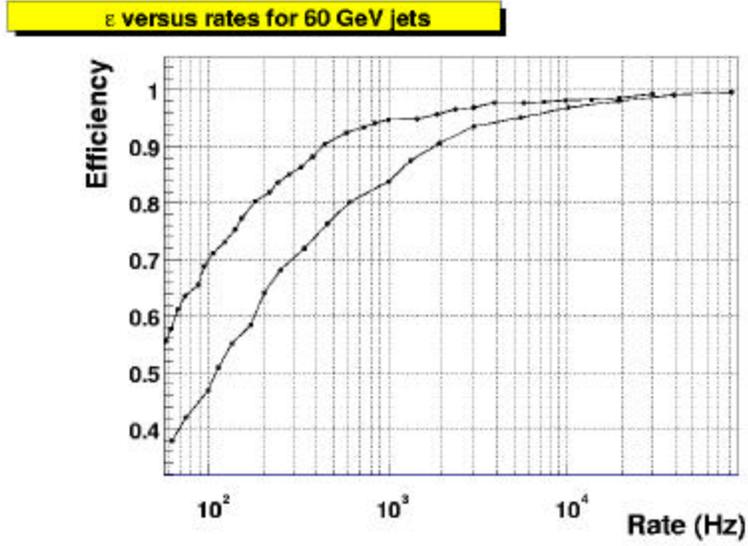


Figure 6: Efficiency for 60 GeV jets as a function of trigger rate. The upper curve is for the proposed new trigger, the lower one for the existing jet trigger at Level 1. For a given efficiency, trigger rates are reduced by a factor of ~3-5.

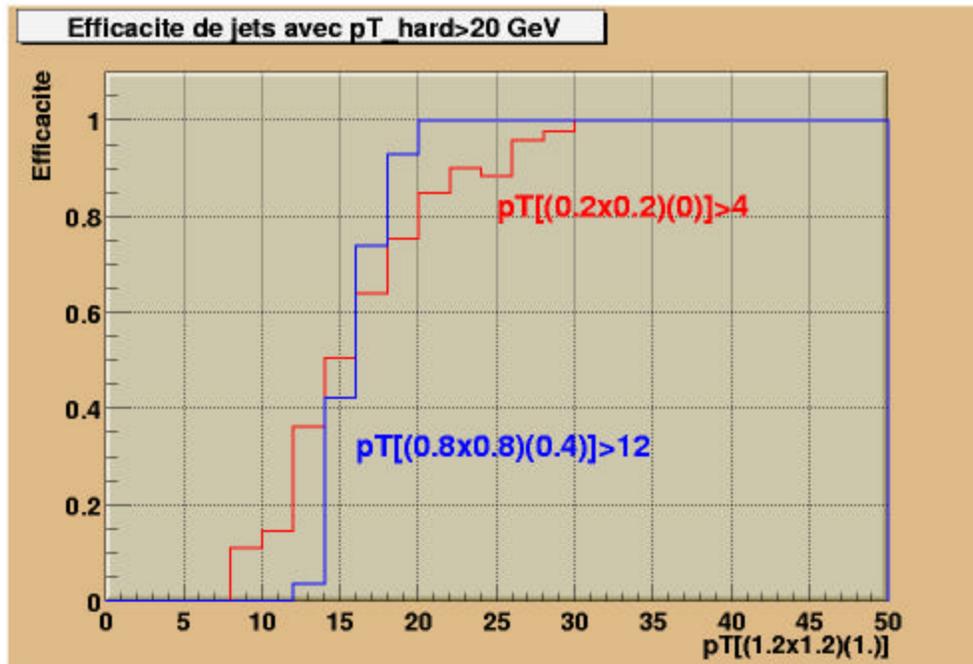


Figure 7: Comparison of efficiency curves for 20 GeV jets (red is current trigger; blue is proposed sliding window trigger).

- 3) There have been preliminary studies of including stereo layers or tightening axial roads in the Level 1 track trigger. Detailed simulations are being performed to better understand these options.
- 4) The Level 2 system contains 16 "L2Alpha" processor boards, based on a DEC/Compaq Alpha chip. These boards were developed together with CDF, and we have experienced great difficulties in manufacturing these complicated boards. The parts are now obsolete and it is not clear that we will have a completely functioning Level 2 system based on these boards. Furthermore, the L2Alpha's we do have are not sufficiently reliable and are very sensitive to external influences. We have decided to start a L2beta project to replace the L2Alpha boards in the future. We have begun development of a prototype, with engineering being done by the LAL Orsay electronics group. While the eventual production of a L2beta processor would be part of the Run 2b upgrade, we would hope to complete and install these processors during Run 2a.
- 5) Upgrading the processing power in the Level 3 farm is a straightforward way to increase the selectivity of the Level 3 trigger. Before a proposal can be made, however, we need the complete farm operational in Run 2a and tested with real data.

Conclusions

DØ is making considerable progress in developing Run 2b upgrade plans. The April PAC report stressed the importance of putting in place a strong project management team, and we are well on our way towards completing this critical task. The silicon tracker design continues to advance, with good progress being made in both high-level design and detailed technical issues. We plan to submit a full Technical Design Report to the laboratory by mid-October. Progress is also being made in understanding how to upgrade the trigger to meet the challenges presented by Run 2b. A major effort to review our trigger options and develop a detailed plan for trigger upgrades will take place this summer. We also plan to submit a detailed and comprehensive Run 2b trigger proposal, including cost and schedule documents, to the laboratory by mid-October.

References

¹M. Church, "*Integrated Luminosity vs. Detector Fiducial Length*", private communication,
http://d0server1.fnal.gov/projects/run2b/silicon/mechanical/luminous_region.doc.