

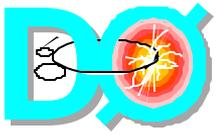
The DØ Run 2b Upgrade

Richard Partridge, Brown University
for the DØ collaboration

- ◆ Run 2b upgrade goals
- ◆ Silicon tracker upgrade
- ◆ Trigger upgrades

Fermilab PAC Meeting

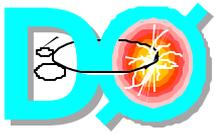
April 20, 2001



Run 2b Upgrade Goals

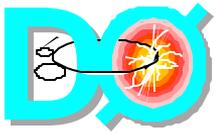
- ◆ Physics case for Run 2b has never been more compelling
 - » Indirect measurements point towards a light Higgs
 - » Possible direct evidence for a Higgs with $M_H \sim 115$ GeV
 - » Precision measurements may be hinting at new physics beyond the SM
- ◆ DØ focus is to maximize discovery potential
 - » Optimize detector for Higgs discovery
 - » Maintain DØ's strength in high- p_T physics (SUSY search, top, EW, etc.)
- ◆ Critical need to upgrade silicon tracker and trigger systems
 - » Silicon tracker must be able to withstand $15\text{-}30 \text{ fb}^{-1}$
 - » Optimize silicon tracker for Higgs discovery
 - » Increase trigger rejection to maintain existing rates with higher luminosity
 - » Ensure efficient triggering for full range of Higgs channels





Silicon Tracker Upgrade Strategy

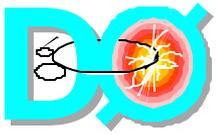
- ◆ DØ decided in January that our baseline solution is to build a new silicon tracker optimized for Run 2b
 - » Avoid long down-time and high risk associated with partial replacement
 - » Improve b-tagging performance for Higgs search
 - » Design for high luminosity, large radiation dose expected in Run 2b
- ◆ Maintain compatibility with existing DAQ
 - » Significant development time and cost for new DAQ electronics
 - » Requires new readout chip that emulates SVX2
- ◆ Minimize schedule risk
 - » Use established technologies, avoid long R&D cycles
 - » Simplify design, minimize number of different components
 - » Utilize elements that are common to other experiments (CDF, CMS, etc.)
- ◆ Benefit from experience in building Run 2a detector
 - » Collaboration has gained substantial expertise in building silicon trackers



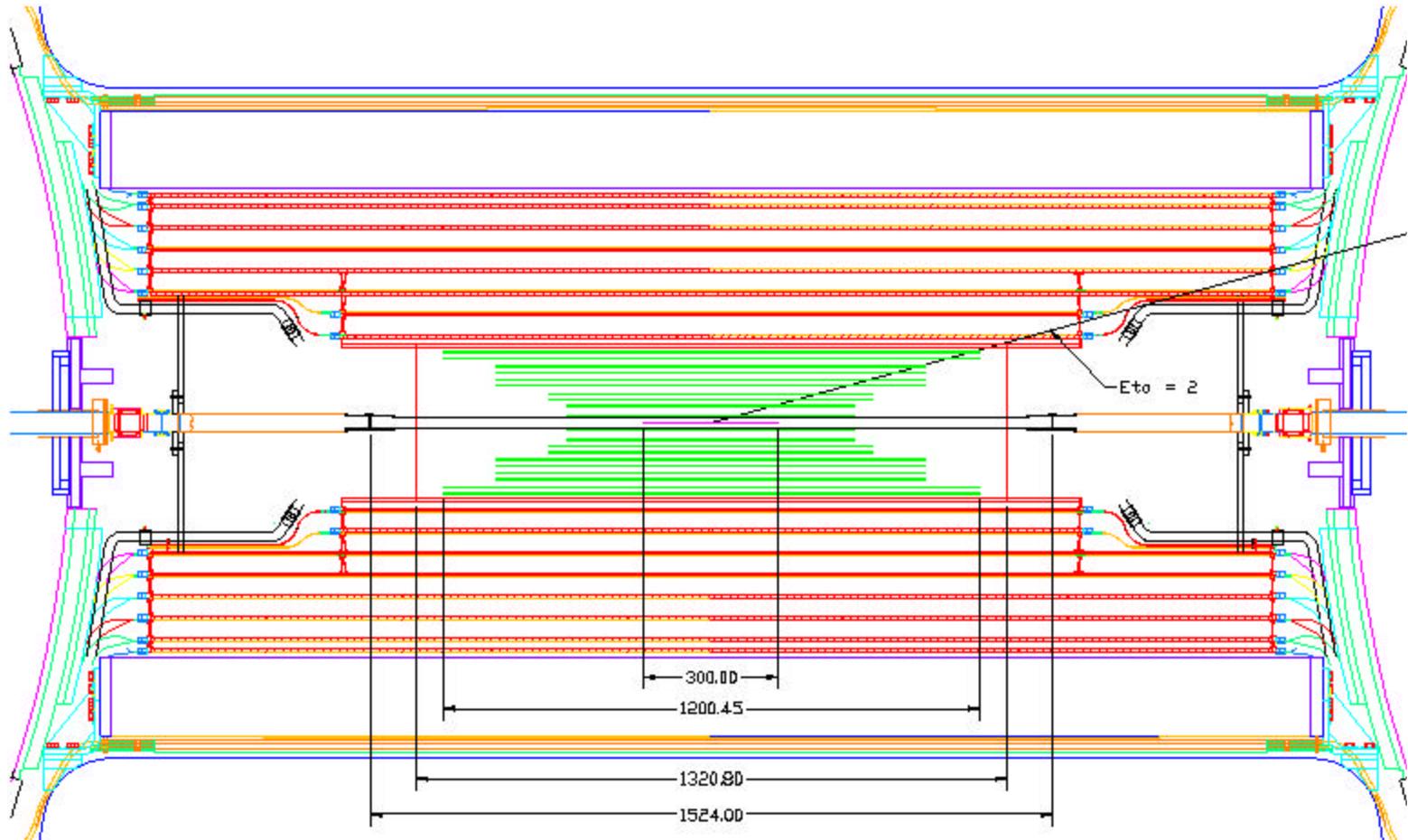
Baseline Tracker Design

- ◆ DØ is developing a detailed “Baseline Design” for the proposed Run 2b silicon tracker
- ◆ “Barrel” design with 6 layers
 - » L0-1 serve to pin down a track’s impact parameter
 - » L2-5 provide pattern recognition, sagitta measurement
- ◆ Tracker acceptance optimized for high- p_T processes
 - » Full coverage of central region, extending tracker coverage out to $|\eta| \sim 2$ to match DØ’s excellent electron and muon coverage
 - » Silicon-only tracking gives $>3\sigma$ sign determination for $p_T < 80$ GeV
- ◆ Only 3 types of detectors
 - » 1-chip and 2-chip detectors in L0-1, 5-chip detectors in L2-5
 - » Stereo measurements in L2-5 using rotated 5-chip detectors
- ◆ Readout uses SVX4 chip, existing DAQ components
 - » Decision to use SVX4 made in December after review of readout options



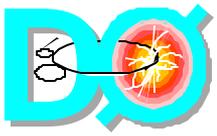


Tracker Side View



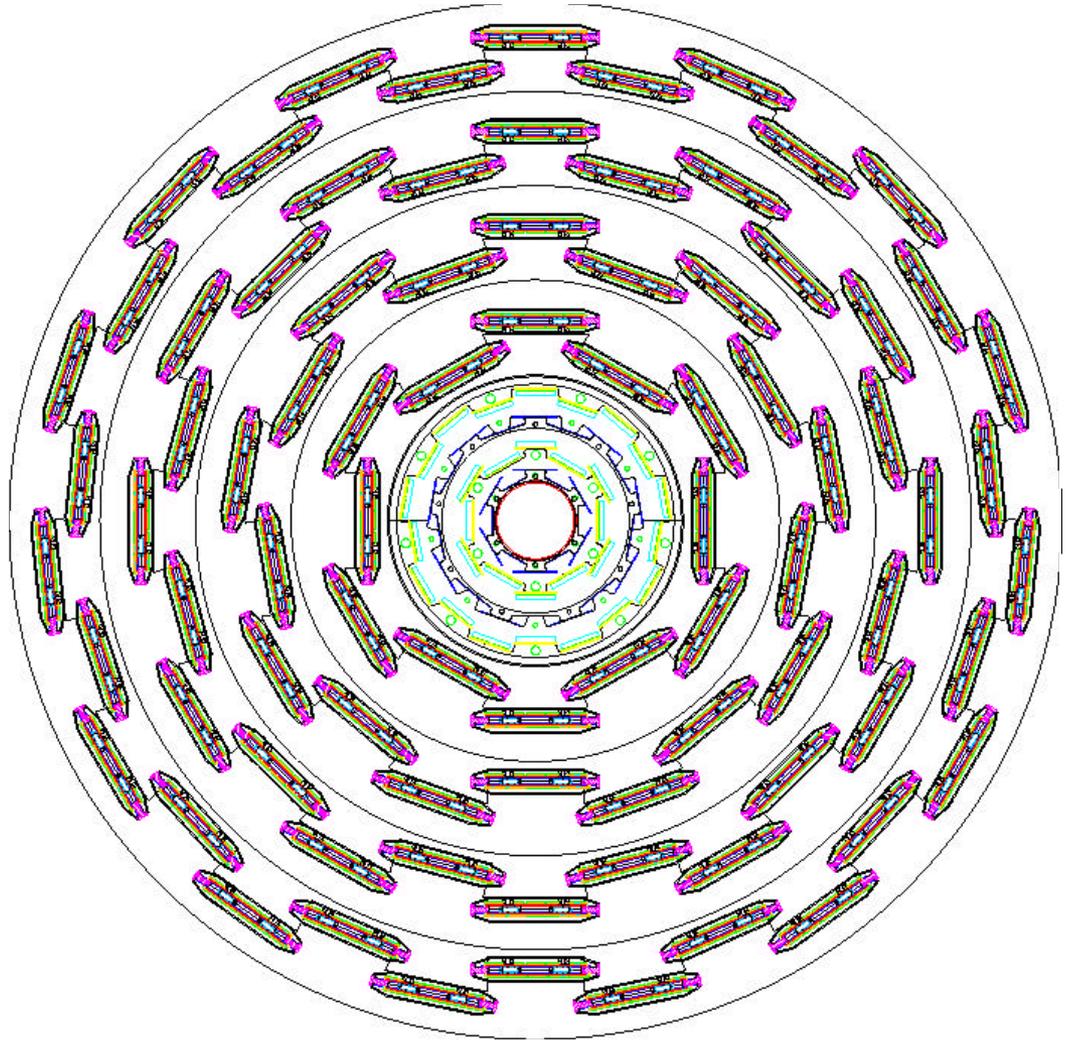
- ◆ Tracker installed as a single unit up to 52" (1320 mm) long

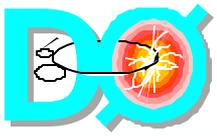




Silicon Tracker End View

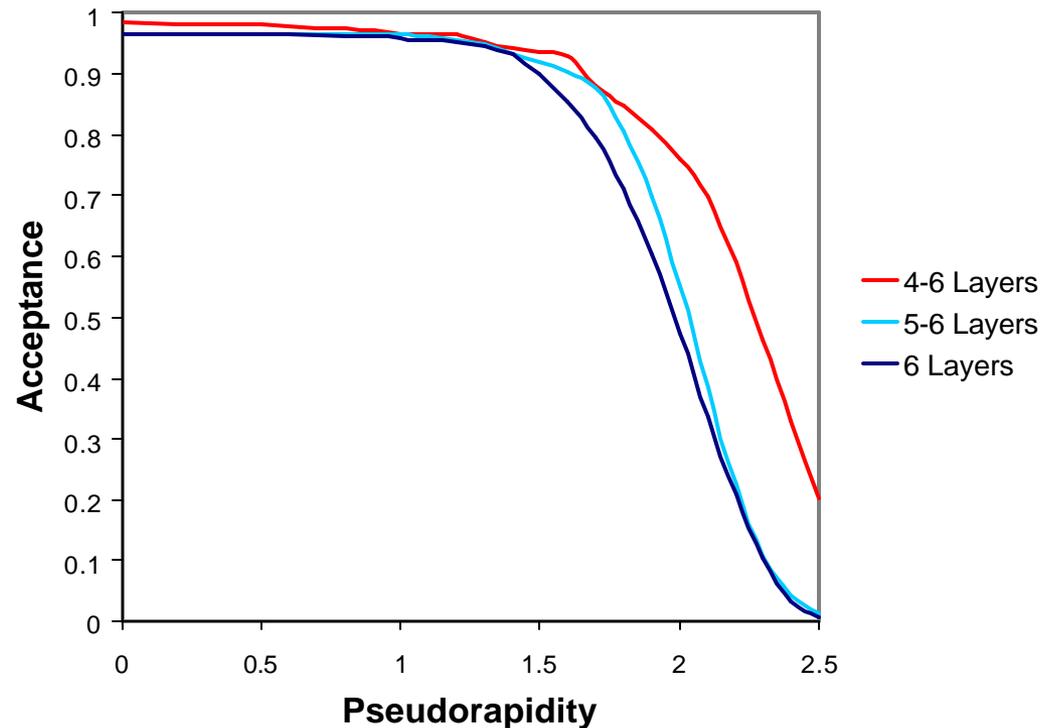
- ◆ Outer constrained to fit inside fiber tracker
- ◆ L0 sensors mounted on new 1" diameter beam pipe

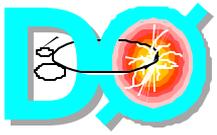




Tracker Acceptance

- ◆ Coverage for $|\eta| < 2$ in all layers ($z_v = 0$)
- ◆ Full coverage for central tracks with $|z_v| < 32$ cm
- ◆ Tracker acceptance calculated for $\sigma_z = 15$ cm

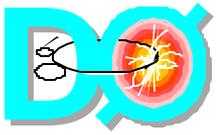




Tracker Parameters

Layer	Radius (mm) (approximate)	Axial/ Stereo	Silicon Sensor (#SVX4, length)	# Phi	#Z	# Sensors	# Chips
0	16	A	1 or 2chip, 8cm	12	8	96	144
1	35	A	2 chip, 8cm	18	8	144	288
2	62	A+S	5 chip, 12cm	12	6	144	720
3	95	A+S	5 chip, 12cm	18	8	288	1440
4	127	A+S	5 chip, 12cm	24	8	384	1920
5	160	A+S	5 chip, 12cm	30	10	600	3000
Total		6A, 4S	3 types			1656	7512

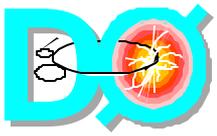
- ◆ Plan to gang two sensors per readout channel for L2-5
- ◆ Maximum of 948 readout channels (no ganging of L0-1)
- ◆ Fits within current DAQ (960 readout channels available)



Readout Electronics

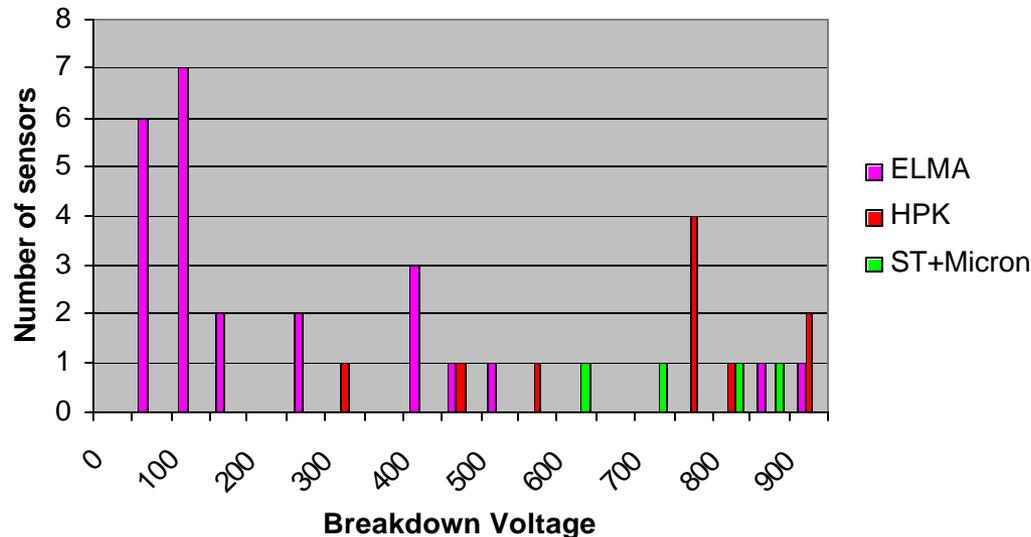
- ◆ DØ has substantial DAQ infrastructure designed around SVX2 readout chip
- ◆ We have demonstrated that SVX3 chips can be operated in “SVX2 mode”
 - » Re-map SVX3 IO signals to match SVX2 signals
 - » Some changes in DAQ firmware required
 - » Test board built to do SVX3 → SVX2 signal re-mapping
 - » SVX3 chip successfully read-out using DØ’s existing DAQ
- ◆ Allows CDF and DØ to use a common readout chip based on the SVX3 design with only small differences in the final metalization layer
- ◆ Decision made in early December to adopt SVX4 readout chip being developed in rad-hard 0.25 μm technology

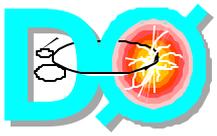




Layer 0-1

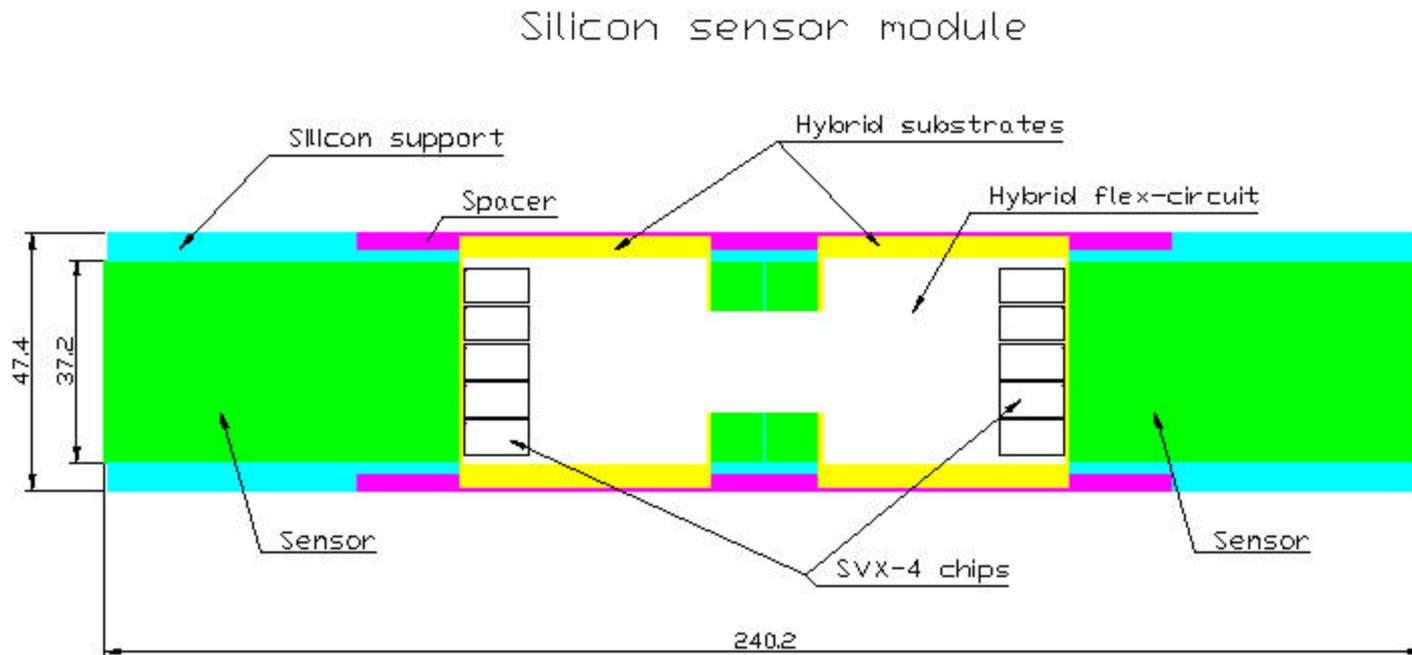
- ◆ 25 μm pitch axial strips with 50 μm readout pitch
- ◆ Mechanical constraints dominate design considerations
 - » Fine pitch flex cables to bring signals out to SVX4 readout chips
 - » Common solution for CDF and DØ may be possible
- ◆ Have begun probe testing, radiation damage studies of single-sided detectors from several vendors

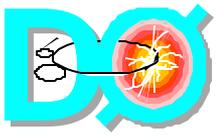




L2-5 Sensor+Hybrid Modules

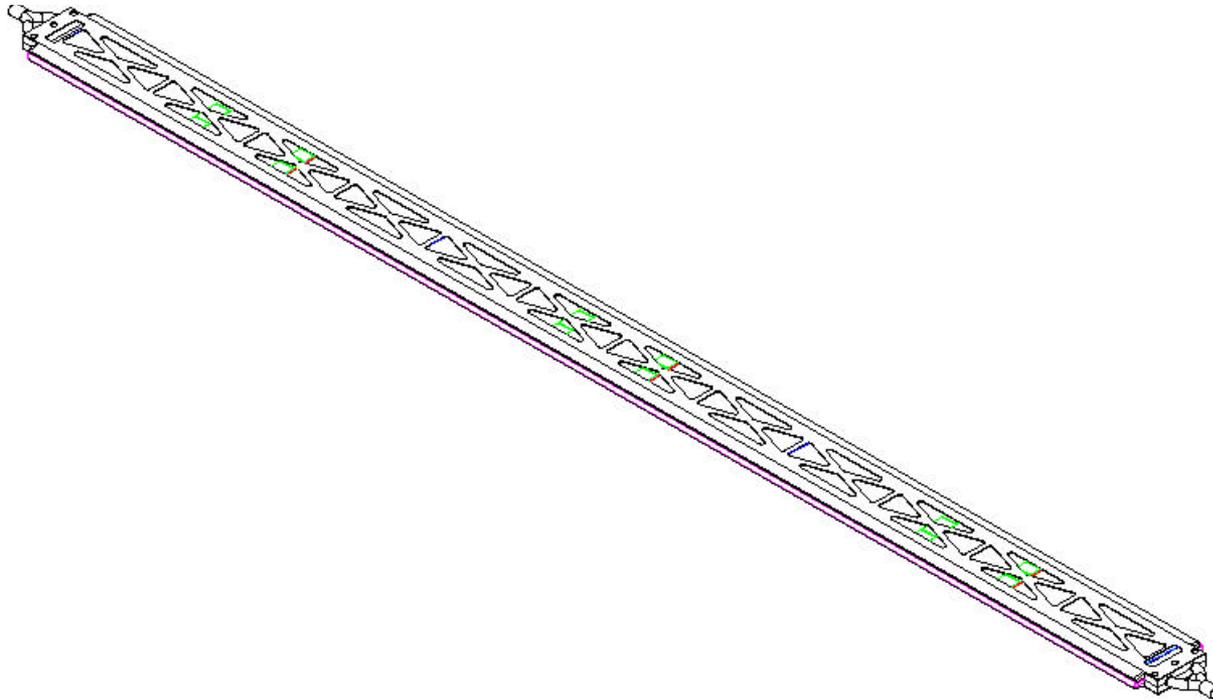
- ◆ Two 12 cm long, 5 chip wide sensors with $\sim 55 \mu\text{m}$ pitch
- ◆ Flex circuit hybrid laminated on substrate; wire bonds directly connect sensor to SVX4 readout chips
- ◆ Stereo sensors mounted on opposite side of silicon support

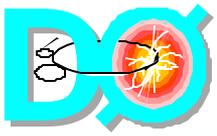




Stave Support Structures

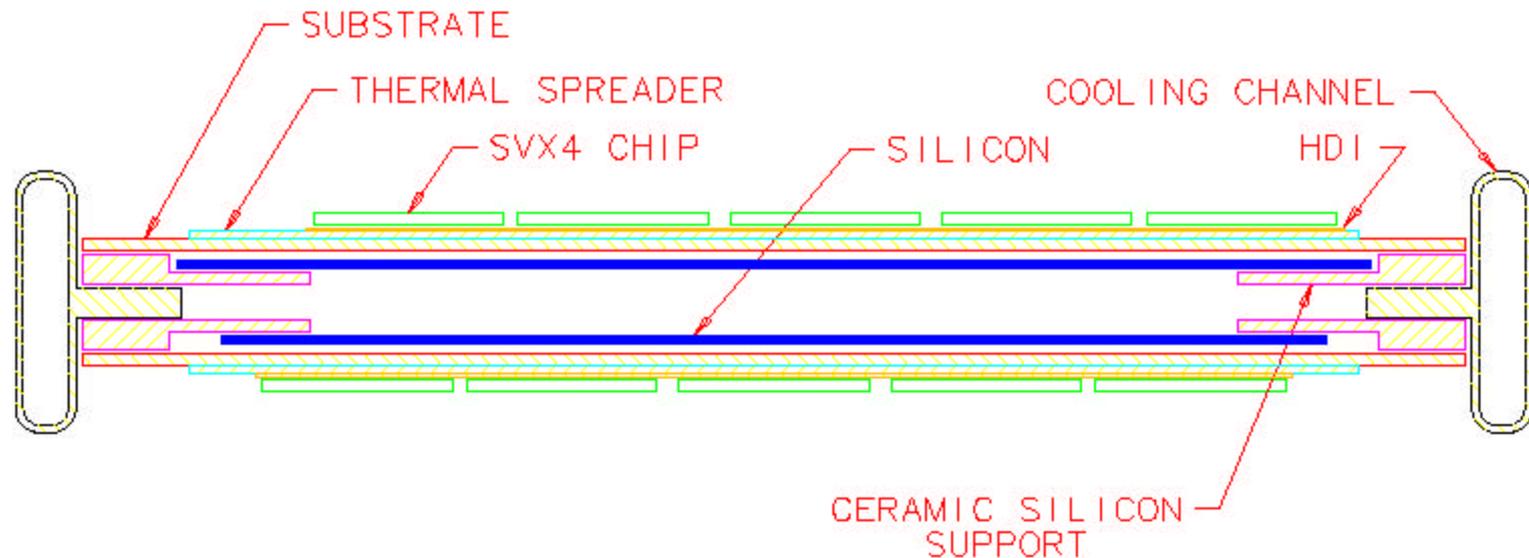
- ◆ Modules are mounted on “Stave” support structures that run the full length of the tracker
- ◆ Cooling, low-mass cables run along length of stave
- ◆ Two different module designs are being investigated





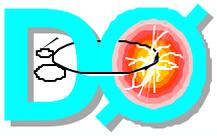
Edge-Cooled Module Design

- ◆ Sensor and hybrid are thermally separated
- ◆ Heat transferred to cooling channel through edge supports

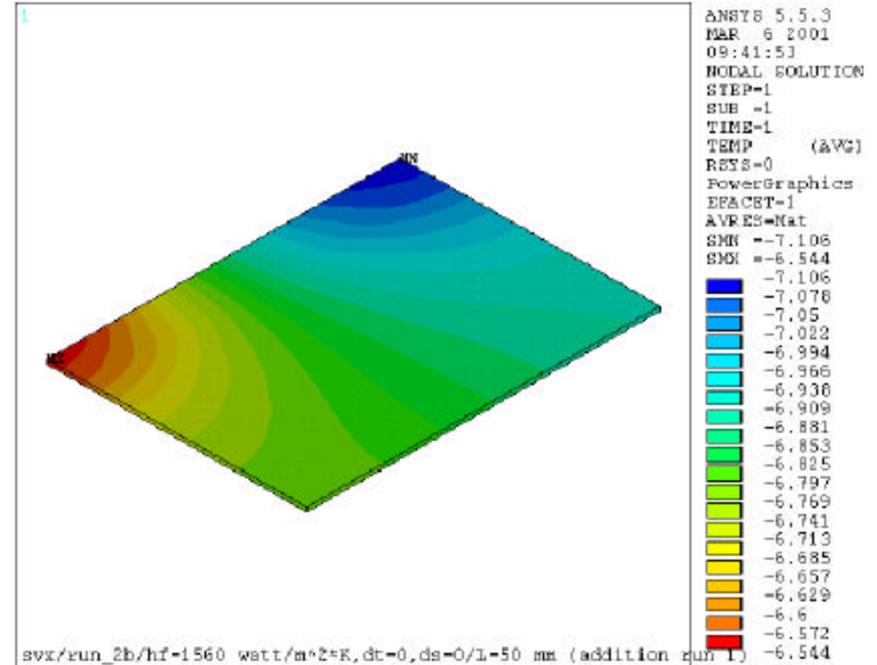
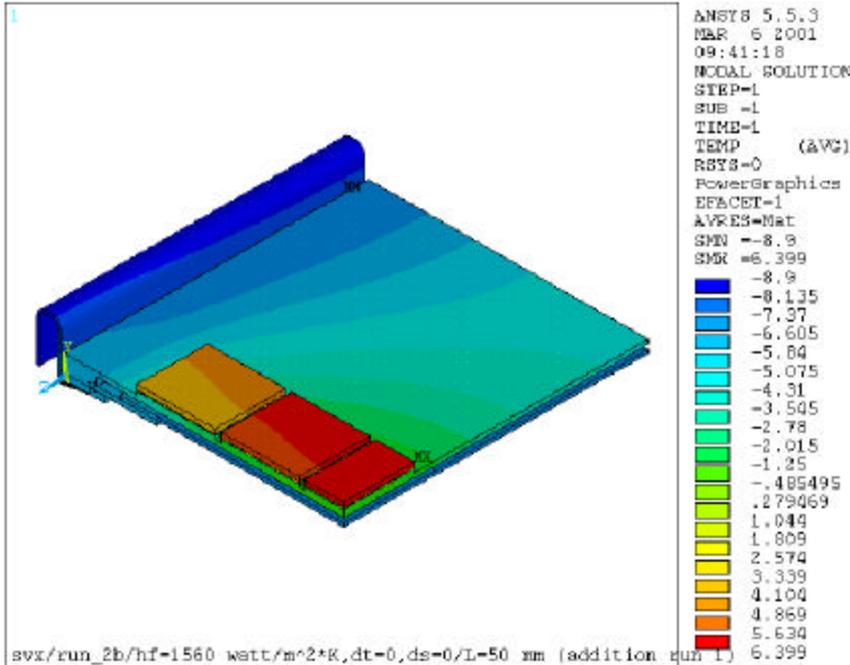


DO RUN 2B SILICON
PROPOSAL "A"





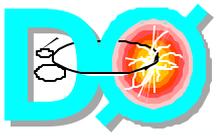
Edge Cooling Thermal Study



Sensor, Hybrid, Mechanics

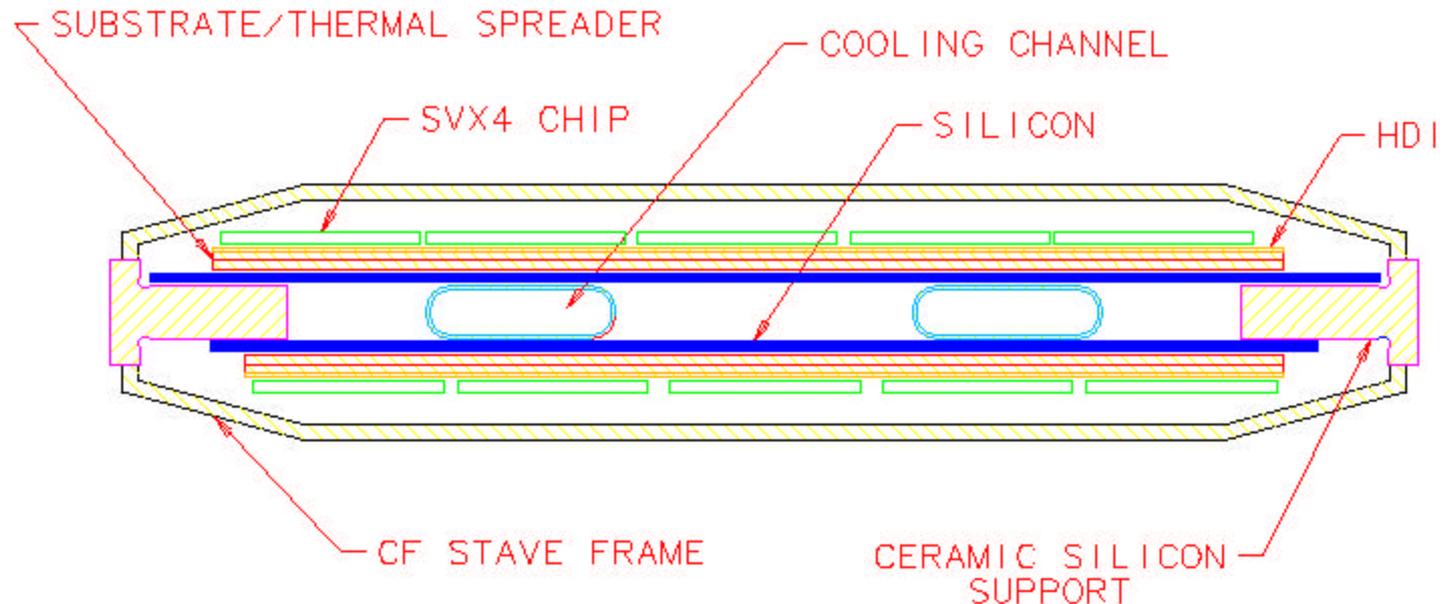
Sensor Only





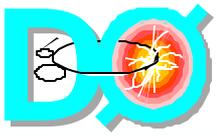
Interior-Cooled Module Design

- ◆ Sensors have large area in contact with cooling channels
- ◆ Hybrid cooled through silicon

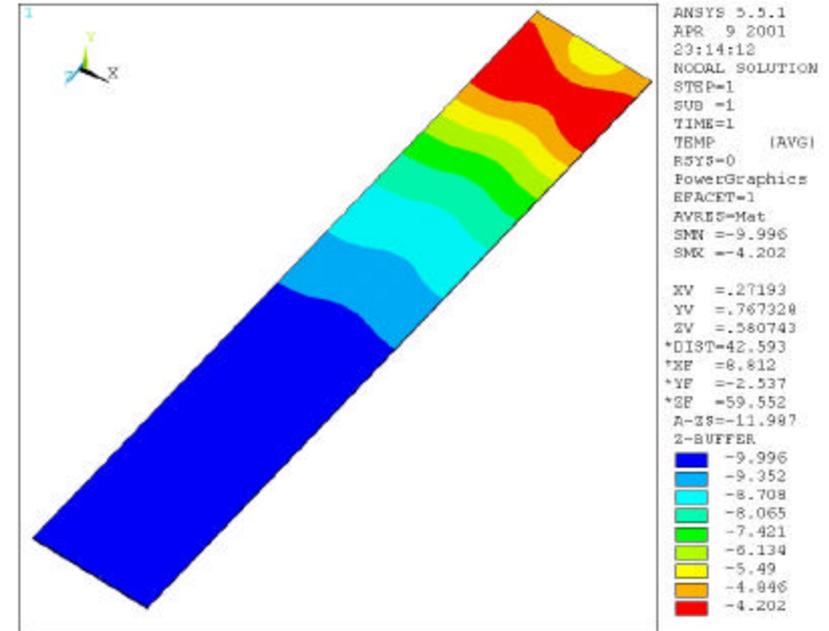
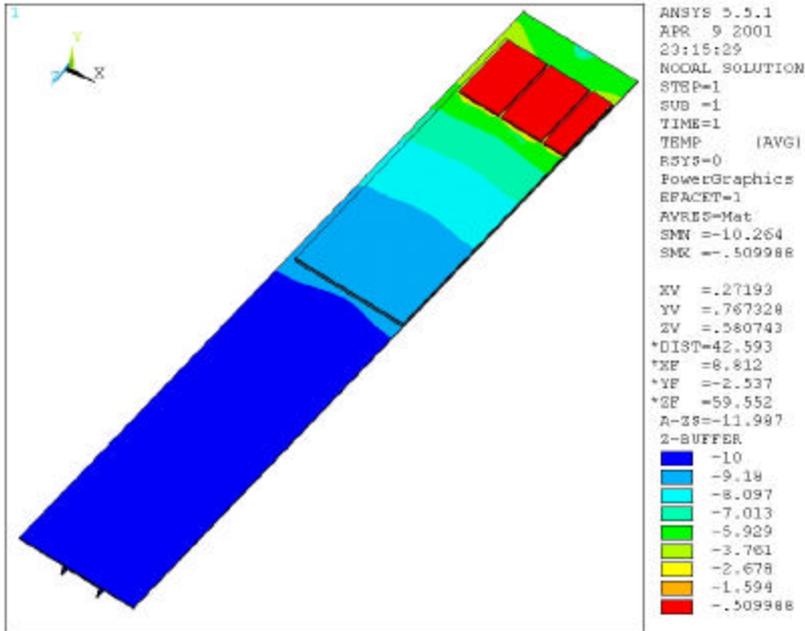


DO RUN 2B SILICON
PROPOSAL "B"





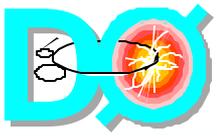
Interior Cooling Thermal Study



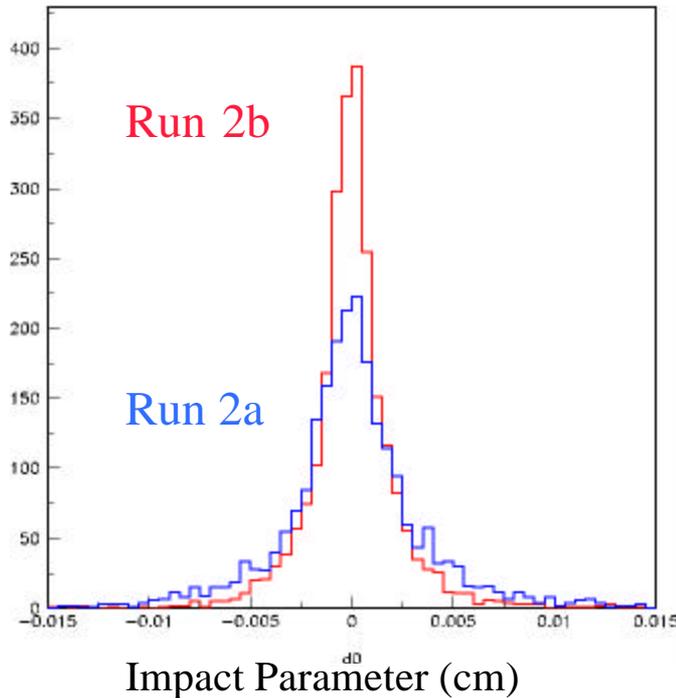
Sensor, Hybrid, Mechanics

Sensor Only





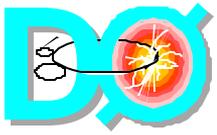
Tracker Performance



- ◆ L0, L5 added to Run 2a GEANT MC (not Run 2b geometry)
- ◆ Full tracking/pattern recognition
- ◆ Simple b-tagging algorithm
- ◆ L0 significantly enhances b-tagging efficiency at low luminosity
- ◆ L5 provides pattern recognition to recover efficiency in busy events

Option	$\sigma(d_0)$, μm	ε_b (%) $t\bar{t} + 0$ Minbias	ε_b (%) $t\bar{t} + 6$ Minbias
SMT	25	40	30
SMT+L0	15	47	35
SMT+L0+L5	15	48	40





Cost and Schedule

- ◆ First pass at cost and schedule
- ◆ Iterative process to refine cost and schedule

Cost estimate:

- ◆ Includes prototypes, spares, and substantial contingency
- ◆ Does not include engineering or SVX4 development costs

Estimated Cost: \$6.75M + \$3.21M contingency = \$9.96M

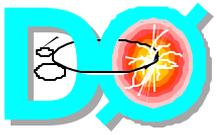
Schedule:

- ◆ Over 300 tasks incorporated into schedule
- ◆ Resource loading has begun but not yet complete

Tracker construction completed: 9/24/04

Tracker installed and ready for collisions: 12/24/04

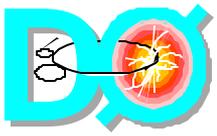




Tracker Status

- ◆ Baseline tracker design is being vigorously pursued
- ◆ Sensor probing and radiation tests being performed on possible L0-1 sensors
- ◆ Developing specifications for prototype sensors
 - » Long lead-time item; would like to place order soon!
- ◆ Working with chip designers and CDF to develop detailed SVX4 specifications
- ◆ MRI proposal submitted in February requesting \$2M in NSF funding for silicon tracker
- ◆ First pass at detailed cost estimate and schedule

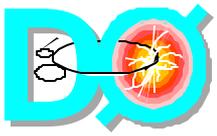




Run 2b Trigger Upgrades

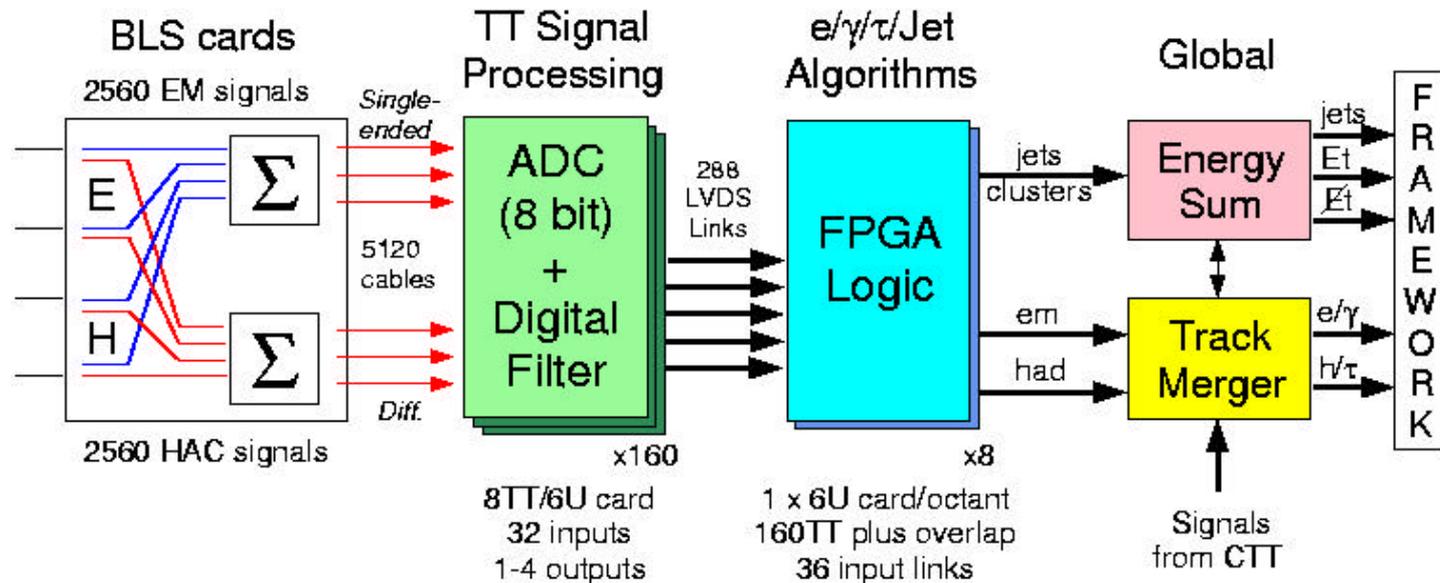
- ◆ Level 1 trigger rate limited to 5-10 kHz
 - » Higher rates incur an unacceptable level of deadtime
- ◆ Level 2 trigger rate limited to 1.8 kHz by calorimeter readout
- ◆ High p_T triggers expected to exceed these limits in Run 2b
- ◆ Need to increase trigger rejection, particularly at Level 1
 - » L1 Calorimeter trigger upgrade to sharpen thresholds
 - » L1 Tracking trigger upgrade to maintain rejection
 - » L2/L3 Processor upgrades

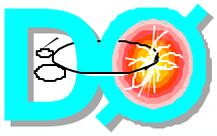
Luminosity ($\text{cm}^{-2}/\text{sec}$)	Crossing Time (ns)	$\langle n \rangle$	L1 High P_T Rate	L1 Total Rate	L2 High P_T Rate	L2 Total Rate
2×10^{32}	396	6.6	4.3	9.5	1.4	3.2
5×10^{32}	132	5.5	10.8	23.8	3.5	8



Calorimeter Trigger Upgrade

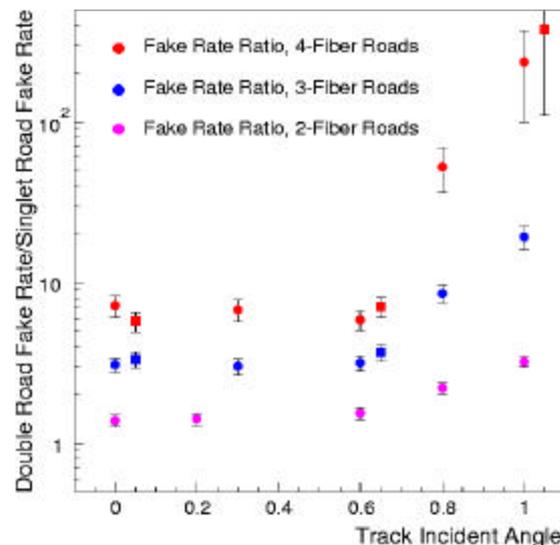
- ◆ Improve energy resolution with digital signal processing
- ◆ Double granularity of trigger towers in ϕ ($0.2 \rightarrow 0.1$)
- ◆ Sharpen thresholds by introducing EM, Jet clustering
- ◆ Match tracks and calorimeter objects
- ◆ Groups: Saclay (new engineering) and Michigan State

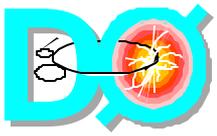




Tracking Trigger Upgrades

- ◆ Tracking trigger rates sensitive to occupancy
- ◆ Upgrade options include:
 - » Narrow tracker roads by using individual fiber hits (singlets) rather than pairing adjacent fibers (doublets)
 - » Use stereo hits to validate tracks found by current track trigger
- ◆ Several simulation studies in progress

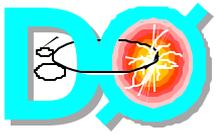




Conclusions

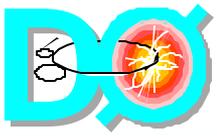
- ◆ Substantial progress since last PAC meeting
 - » Decision to use SVX4 readout chip
 - » Baseline tracker design developed
 - » Detailed tracker engineering studies have begun
 - » Sensor evaluation, radiation testing underway
 - » Trigger upgrade options are being refined
 - » Silicon and trigger simulation results providing useful feedback
 - » Cost estimate and schedule have been developed for silicon upgrade
- ◆ Need to proceed vigorously with design, prototyping, and construction to meet Run 2b time constraints
 - » Sensor prototype order is on the critical path, need to submit order soon
- ◆ Working on developing Project Management team
 - » Mechanical design team led by Bill Cooper in place
- ◆ Need to conduct internal evaluation of baseline design





DØ Run 2b upgrade has
begun in earnest





DØ Trigger Architecture

- ◆ Level 1
 - » Calorimeter trigger
 - » Fiber tracker trigger
 - » Preshower (e/γ) trigger
 - » Muon trigger
- ◆ Level 2
 - » Silicon track trigger
 - » Introduce Correlations, Refine Level 1 decision
- ◆ Level 3
 - » Full event information available
 - » Farm of high-performance computing nodes

