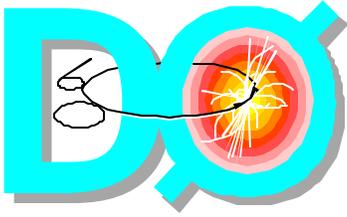


SIFT Replacement

Marvin Johnson

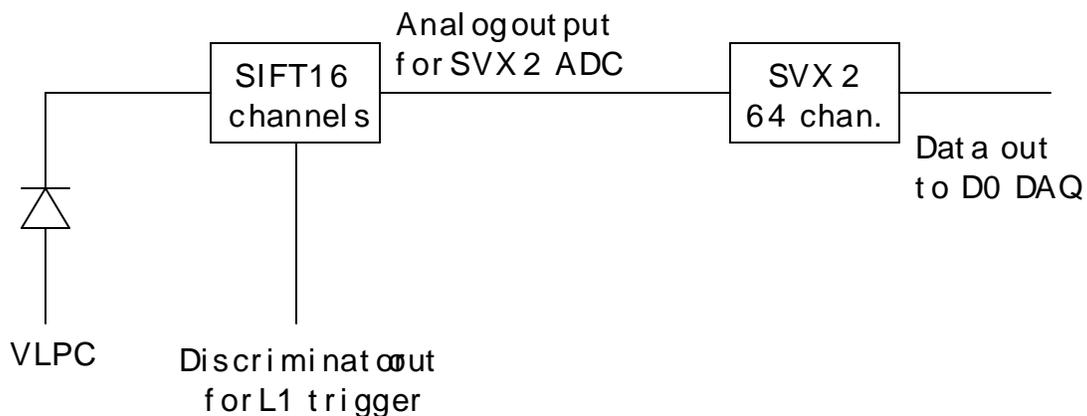


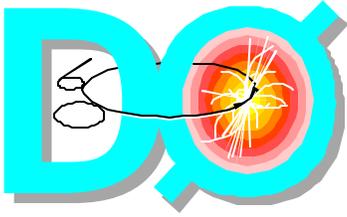
What is the SIFT?

- **Scintillating Fiber Trigger chip**

- ◆ **Custom IC for Level 1 triggers from the Scintillating fiber tracker & pre shower detectors**

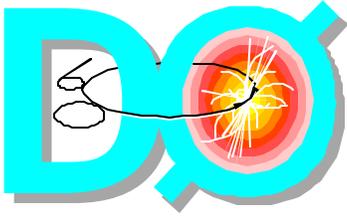
- ◆ **Provides trigger pick off for VLPC signals**
- ◆ **Sends analog signals on to the SVX II for digitization**





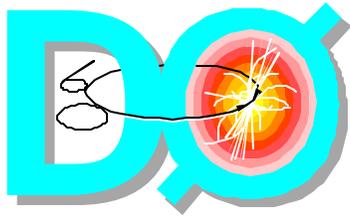
SIFT Parameters

- 16 channels/chip
- 5 fC - 300 fC discriminator range
 - ◆ 1 PE ranges from 4 to 7 fC (gain of VLPC)
- Analog out gain of .25 & .5
 - ◆ Too much charge from preshowers for the SVX 2
- 400 fC dynamic range
 - ◆ Requires preamp reset every crossing
- Discriminator reset at every crossing



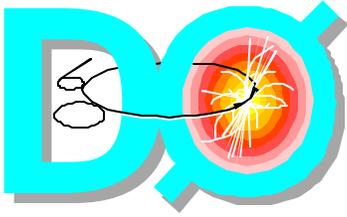
Why Replace It?

- **Tracker charge collection time longer than expected**
 - ◆ Requires 70 ns for 90% collection from fiber tracker
- **SIFT is too slow**
 - ◆ 69 ns for 80% of the charge to analog output
 - 33 fC (~5 PE) step input
 - ◆ Need about 40 ns to reset SIFT and read out analog signal
 - ◆ Minimum time is about 180 ns.



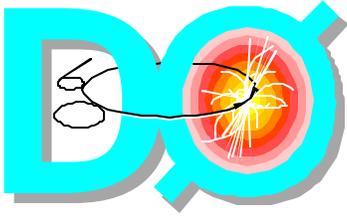
Squeeze SIFT to 132 ns

- **Get 43% charge at discriminator (70 ns integration time)**
 - ◆ **Not enough S/N to trigger on one PE**
- **Operation is unstable**
 - ◆ **Spread in disc. thresholds and analog output**
 - ◆ **Not enough time to reset preamp or discriminator**
- **Get feedback from disc. Into analog out**
 - ◆ **both occur at the same time**



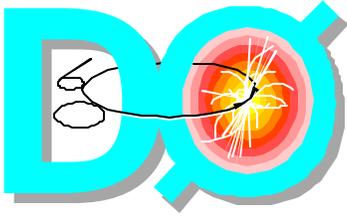
Why can we do better?

- Use .25 micron process
 - ◆ SIFT is .8 micron
 - ◆ Lot of experience in .25 micron
 - FPIX, SVX 4...
- Multistage amplifier
- Incorporate pipeline on chip
 - ◆ No output unless trigger
 - Saves analog output time
 - Eliminates disc. cross talk into analog.
 - SIFT requires analog out at different time than disc. Out.
 - ◆ Output can be slow (7.5 MHz).
- Low inductance package.



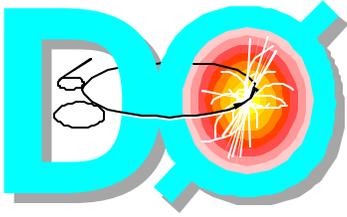
Chip Plan

- 64 channels per chip
- Multi stage preamp
 - ◆ 4 to 500 fC dynamic range
 - ◆ Programmable on chip gain
 - 16 ranges (4 bits)
 - ◆ 95% of charge in 70 ns
 - ◆ Reset time of 60 ns
 - Discriminator output here
- Use SVX 4 pipeline
- 4 multiplexed analog outputs
 - ◆ 4 commercial flash ADCs
- Control by local FPGA



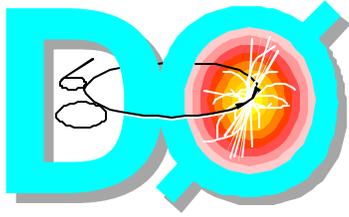
Chip packaging

- **Current SIFT is in an MCM**
 - ◆ **4 SIFTS+1 SVX for 64 channels**
- **8 MCM's per PC board**
- **Can replace MCM with PC board**
 - ◆ **1 new SIFT, 2 dual ADCs, 1 FPGA**
 - ◆ **Use chip on board for space.**
- **Alternative is standard packaging in quad flat pack**
 - ◆ **Easier diagnostics**
 - ◆ **Cheaper packaging**
 - ◆ **Simpler repair**



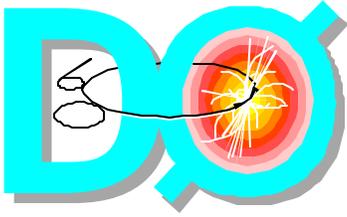
Board Options

- **Replace MCM's with PC board**
 - ◆ **Pro**
 - ◆ Reuses existing boards
 - ◆ **Con**
 - ◆ Need rapid replacement to avoid long shut down
 - ◆ MCM's are hard to remove without damaging board (10-20% loss)
 - ◆ Small PC boards are expensive
 - ◆ Labor for board replacement is expensive
 - ◆ New FPGAs eliminate almost all of the other chips on the board



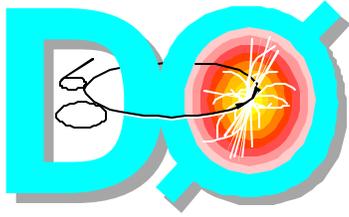
Board Options II

- Total cost of the two options is within 10%
- New board is simpler so easier to build & repair.
- Present choice is to make a new board



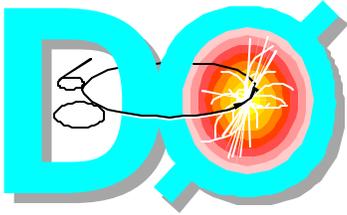
Cost Estimate

- Plan to share first submission with FPIX and SVX 4
 - ◆ Cost will be about \$80K
 - ◆ Get enough chips if they are OK



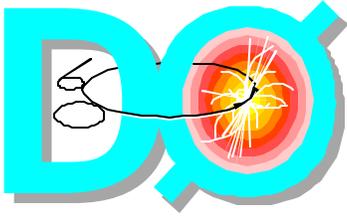
Chip Schedule

- **First Chip Submission**
12/20/01
 - ◆ TSMC takes 2 months
 - ◆ Need about 4500 chips
- **Second Submission 8/1/02**
 - ◆ 6 months to test chip and fix design errors
- **Chips packaged and ready for use 1/29/03**
 - ◆ 4 months to test wafers and put them in quad flat packs
 - ◆ Need to test only 6 or 7 wafers
 - ◆ Testing will be done at FNAL



Board Schedule

- **Schematic and layout are very similar to current board**
 - ◆ **Eliminate unneeded parts**
- **Schematic starts 12/17/01**
- **First Prototype 8/14/02**
 - ◆ **Use first submission chips**
 - ◆ **9 months for schematic, layout and prototype construction**
- **Second prototype 4/9/03**
 - ◆ **2 months after packaged chips**
- **Production done 2/27/04**
 - ◆ **11 months for prod. & testing**



Summary

- **Current SIFT will not work for 132 ns crossing interval**
- **Advances in chip design and process allow a chip that will**
- **Board replacement is about the same cost as repair so we chose board replacement**
- **Schedule allows enough time to complete the project**