'The DØ Run 2b Silicon Tracker Project'

A Technical Overview

External Independent
Review
November 4-8, 2002

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For the Run 2b Silicon Group

Outline

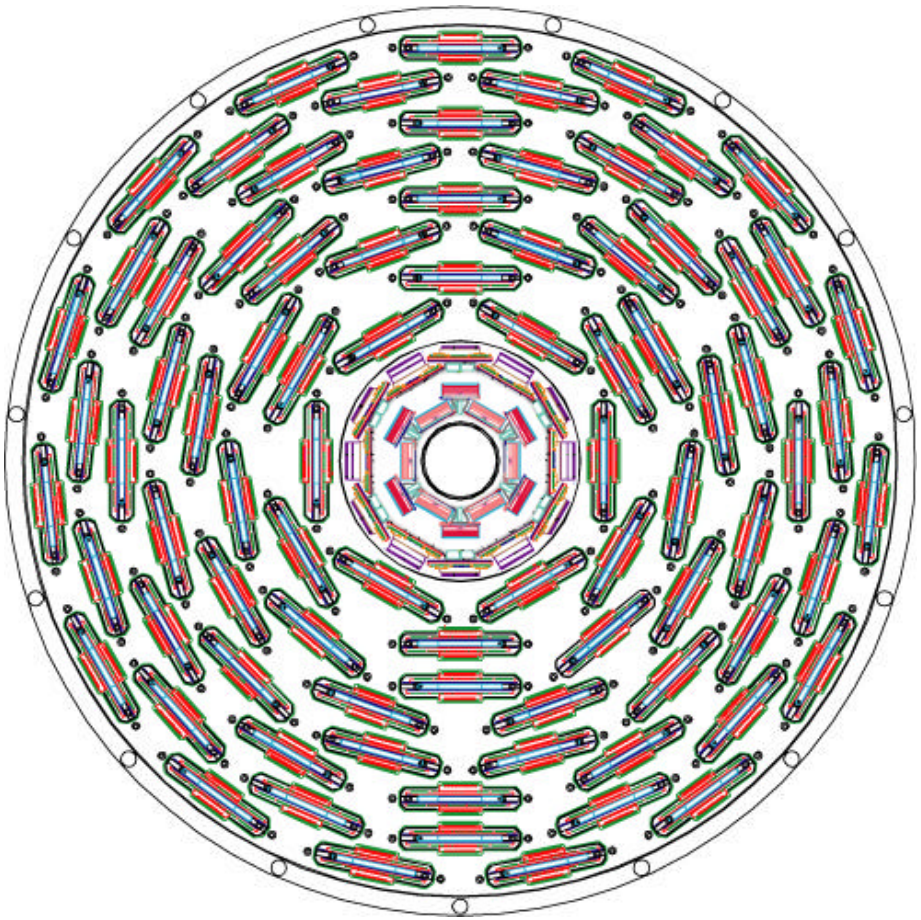
- Overview of Silicon Detector Design
  - Design considerations
  - Summary of design
  - Expected Performance
- Status of design and prototyping
  - Sensors, Mechanical, Electrical, …
- Testing status
- Summary and Conclusions

Design Considerations

- Guiding Principles
  - Able to build expeditiously
  - Minimal cost and minimal shutdown time
- Benefit from Run IIa experience
  - Choose design adequate to achieve physics goals, but do not over-design
  - Modular design, minimize the number of different elements
  - Use established technologies: single sided silicon only
- Spatial
  - Installation within existing fiber tracker, with inner radius of 180 mm
  - Full tracking coverage
    - Fiber tracker up to $|\eta| < 1.6$
    - Silicon stand-alone up to $|\eta| < 2.0$
- Data Acquisition
  - Retain readout system outside of calorimeter
  - Current cable plant allows for ~912 readout modules
  - Total number of readout modules cannot exceed 912
- Silicon Track Trigger
  - Respect 6-fold symmetry

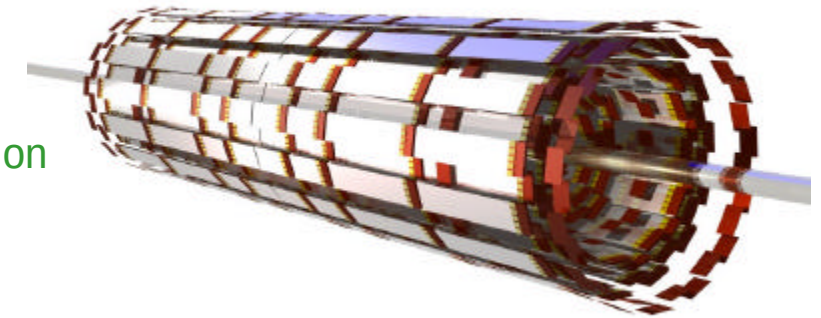
Detector Design

- Six layer silicon tracker, divided in two radial groups
  - Inner layers: Layers 0 and 1
    - 18mm < R < 39mm
    - Axial readout only
    - 50/58 μm readout for L0/L1
    - Assembled into one unit
    - Mounted on integrated support
  - Outer layers: Layers 2-5
    - 53mm < R < 164 mm
    - Axial and stereo readout
    - 60 μm readout
    - Stave support structure
  - All sensors intermediate strips
- Employ single sided silicon only, 3 sensor types
  - 2-chip wide for Layer 0
  - 3-chip wide for Layer 1
  - 5-chip wide for Layers 2-5
- No element supported from the beampipe



Performance of Proposed Detector

- Performance studies based on full Geant simulation
  - Full model of geometry and material
  - Model of noise, mean of 2.1 ADC counts
  - Single hit resolution of ~11 μm
  - Longitudinal segmentation implemented
  - Pattern recognition and track reconstruction



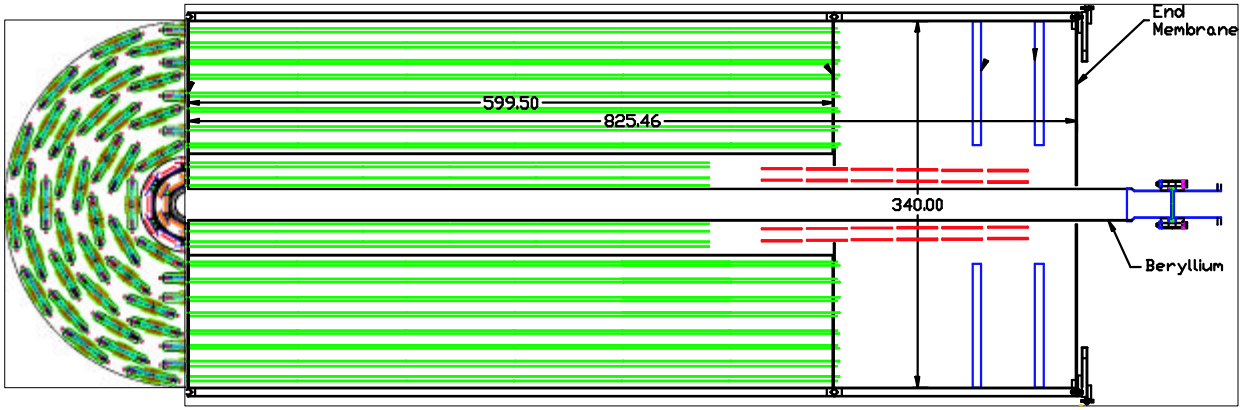
- Benchmarks
  - $\sigma(p_T)/P_T$ ~ 3% at 10 GeV/c
  - $\sigma(d_0)^2 = 5.2^2 + (25/p_T)^2$
    - $\sigma(d_0) < 15$ μm for $p_T > 10$ GeV/c
- b-tagging
  - Loose b-tag algorithm: signed impact parameter
    - Loose track selection
    - Impact parameter significance
      - 2 tracks: $d_0/\sigma(d_0) > 3$
      - 3 tracks: $d_0/\sigma(d_0) > 2$
  - b-jet tagging efficiency of ~ 65% per jet

	TDR
$P(n_b \geq 1)$	76%
$P(n_b \geq 2)$	29%
Mistag Rate	< 1.5 %

Based on WH-events, with b's falling within acceptance

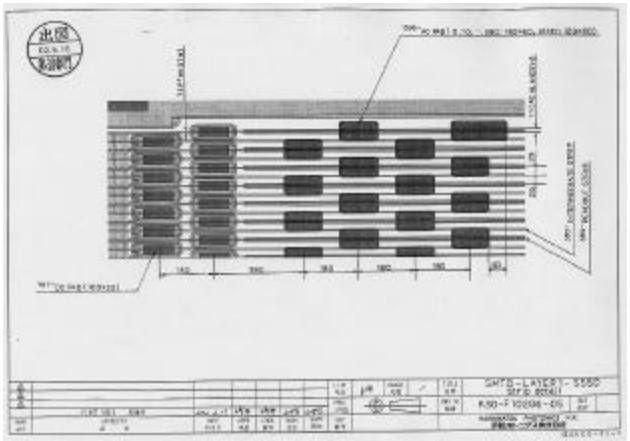
From Basics to Details

- Alternate designs and other options were considered and were found not to be compatible with the constraints and physics motivation for Run IIb
- Overview of nearly all elements of the detector following the signal path
  - Sensors
  - Support Structures
  - Hybrids
  - Downstream Electronics
- And how we are setup for testing and production
  - ...



Sensors

- All sensors are single-sided silicon with axial strips only
- Layer 0
  - 2-chip wide, 50µm pitch, intermediate strips, 15.5x79.4 mm cut dimension
  - Sensors will be based on CDF layer00 design; ELMA and HPK as manufacturer
    - HPK
      - Proven track record; manufactured CDF sensors, V_{break} > 700V, irradiated by DØ
      - 'Old' CDF Layer00 sensors meet all our specifications
      - No prototype sensors ordered; specifications are the same as for Layer 1 sensors, for which prototypes have been ordered from HPK
    - ELMA
      - 60 Lyr 0 sensors produced 47 received: 20 mechanical, 27 currently being tested
- Layer 1
  - 3-chip wide, 58µm pitch, intermediate strips, 24.3x79.4 mm cut dimension
    - HPK
      - Order placed with HPK and mask revised to take into account HPK recommendations
      - 10 prototype sensors received at the end of September

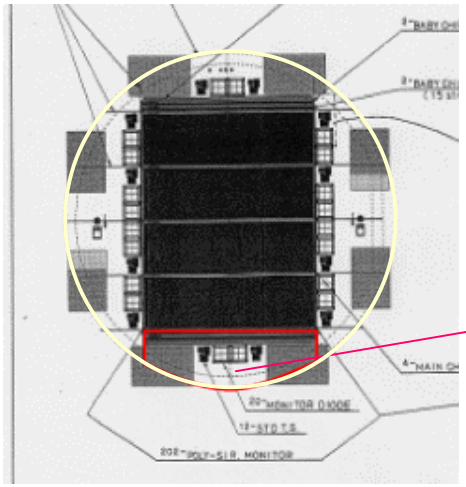


Layer 1 detail

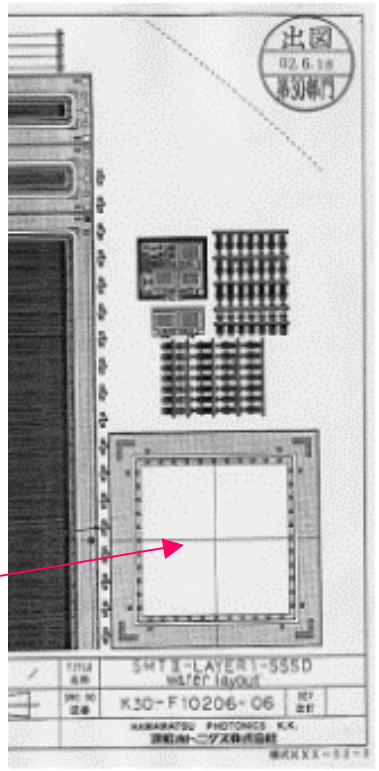
Sensors

- ELMA (Layer 1)
  - 13 sensors produced; currently being tested. Sensors are being used for module prototypes

- Layers 2-5
  - 5-chip wide, 60μm pitch, intermediate strips, 41.1x100 mm cut dimension
  - Order placed with HPK; prototype sensors to be shipped mid-November
  - Sensors very similar to CDF outer layer sensors
- Silicon Diodes
  - Needed for radiation monitors
  - Diodes are part of our specifications and are implemented in the test structures
  - Test structures allow for tests of wafer

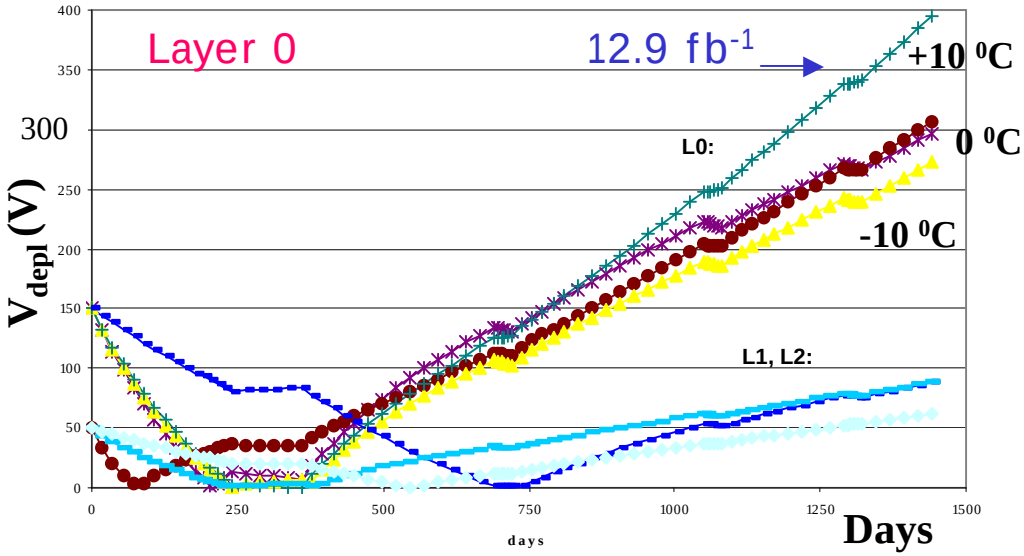


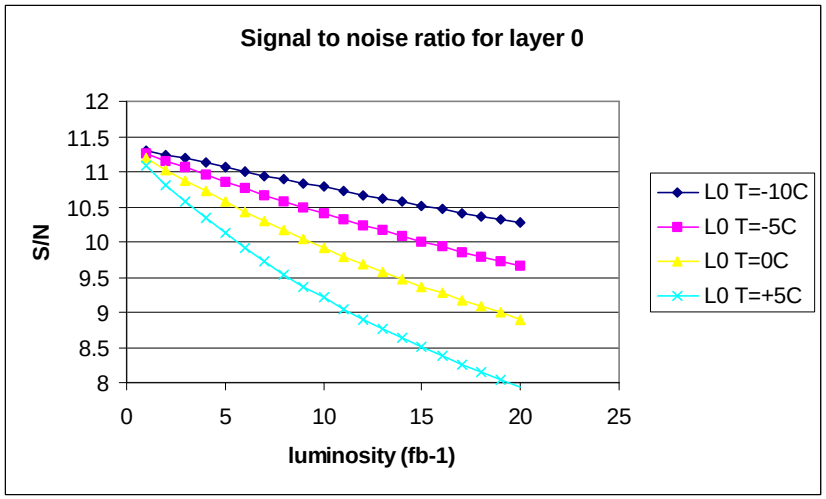
HPK Layer 1 Wafer Layout



Radiation Damage Requirements

- Sensors will be subjected to fluence of 2 10^{14} 1 MeV neutron equiv./cm^2
- Parameters for detector
  - V_{depl} after irradiation
  - Signal to Noise ratio
- Requirements
  - S/N ratio > 10 after 15 fb^{-1}
  - $V_{depl} \ll V_{break}$ to allow for over-depletion for full charge collection

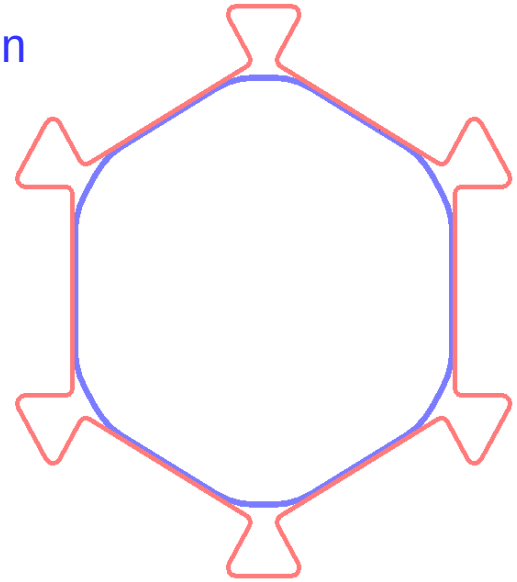


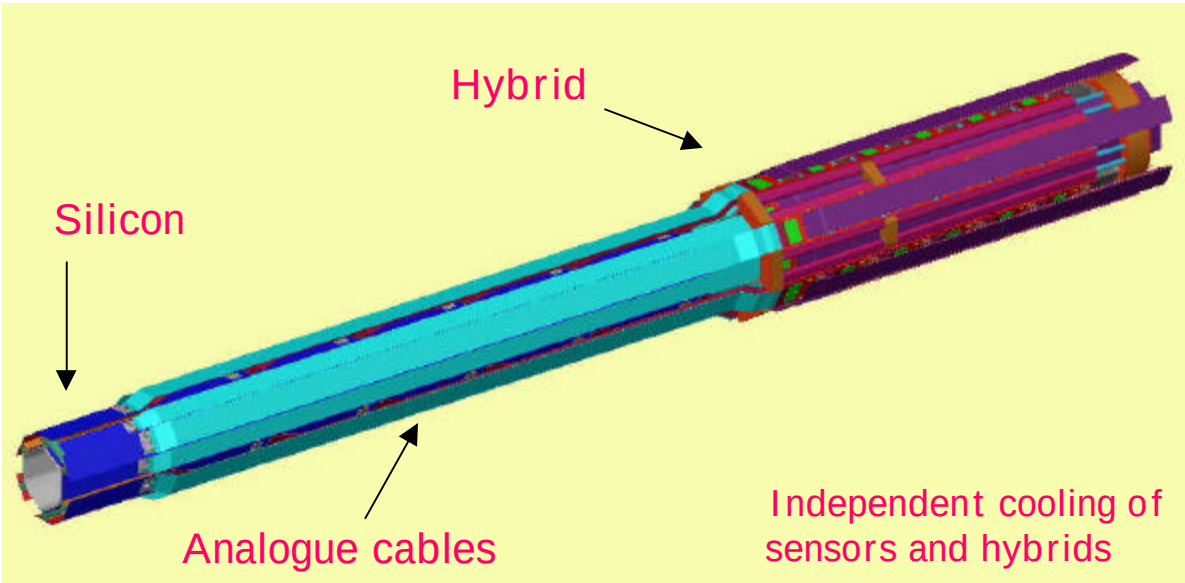


Layer	T_silicon (C)
Layer 0	-10
Layer 1	-5
Layer 2	0
Layer 3	>0
Layer 4	>0
Layer 5	>0

Layer 0 and Layer 1

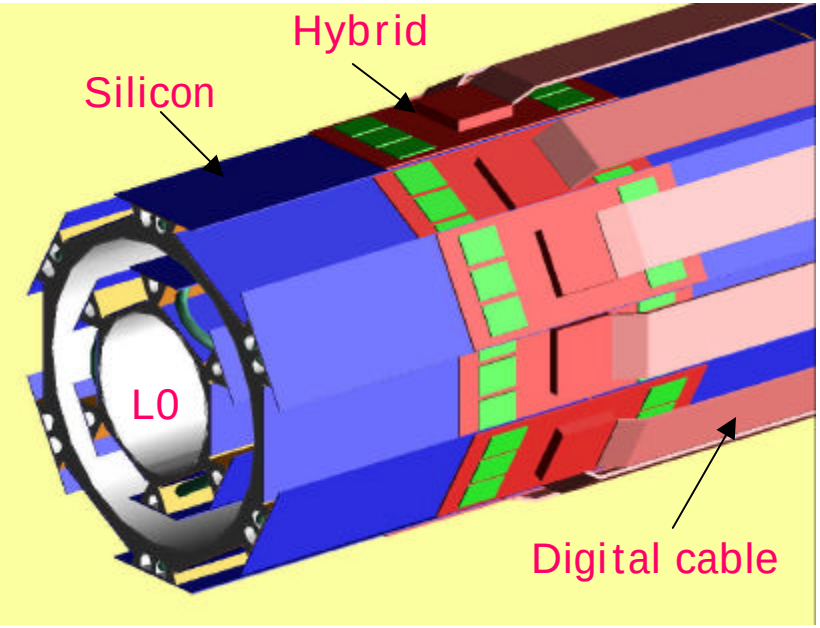
- Support Structure by University of Washington
  - Inner shell, carbon fiber
    - 12-sided
    - 4 layers $[0,90]_s$ lay-up
  - Outer shell, carbon fiber
    - 12-fold crenellated geometry
    - Possible use of pyrolitic graphite (L0)
    - Sensors cooled to T=-10 ^{o}C
  - Uses analogue cables:
    - minimize material
    - stringent space constraints
    - T. requirements





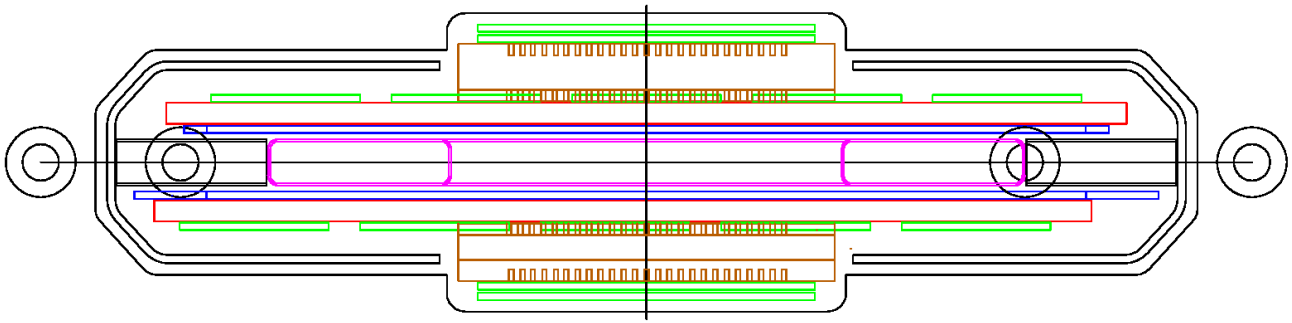
Layer 1

- Support structure similar to Layer 0, also done by U. of Washington
- Readout electronics mounted on the sensors:
  - Power dissipation of 0.5W/chip
  - Power dissipation of < 0.1 W/sensor after 15 fb^{-1}
- To minimize radiation damage, $T_{Si} < -5\ ^0C$
- Cooling:
  - Layer 0
    - Hybrids outside tracking volume
    - Independent cooling of sensors and hybrids
  - Layer 1: hybrids mounted on sensors
    - Modestly conservative power dissipation of svx4 chips assumed
    - Current design achieves adequate cooling



Layers 2-5: Staves

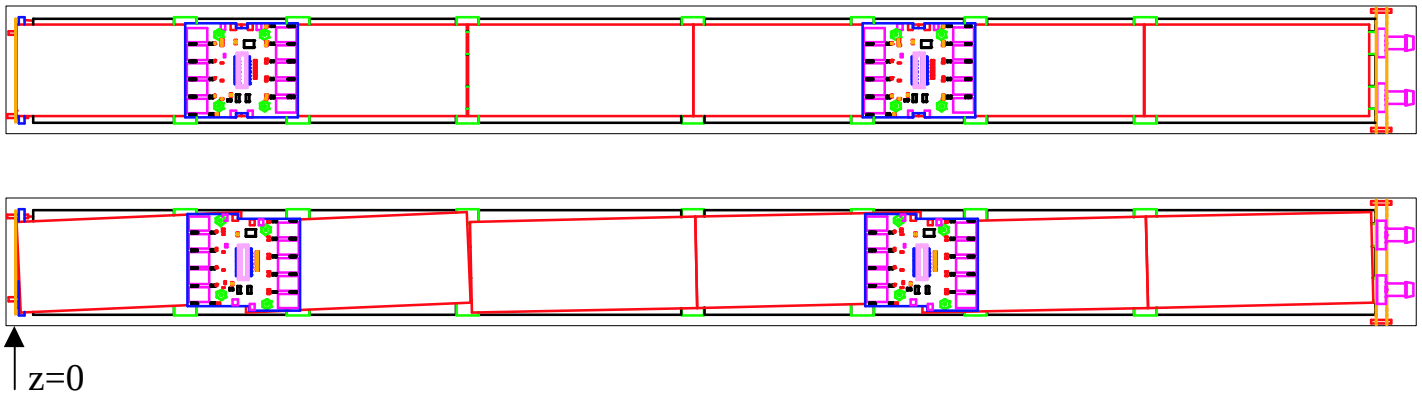
- Basic building block of the outer layers is a stave



- Stave is:
  - two-layer structure of silicon sensors
  - One layer of axial only, and one layer of stereo only readout
    - stereo angle obtained by rotating the sensor
  - Layers separated by a “core” with positioning and reference pins and cooling tubes
  - Total of 168 staves
- C-shells at edge of stave provide stiffness
- Staves are positioned and supported in carbon fiber bulkheads at z = 0 and z = 605 mm.
  - Locating features on stave provide the alignment

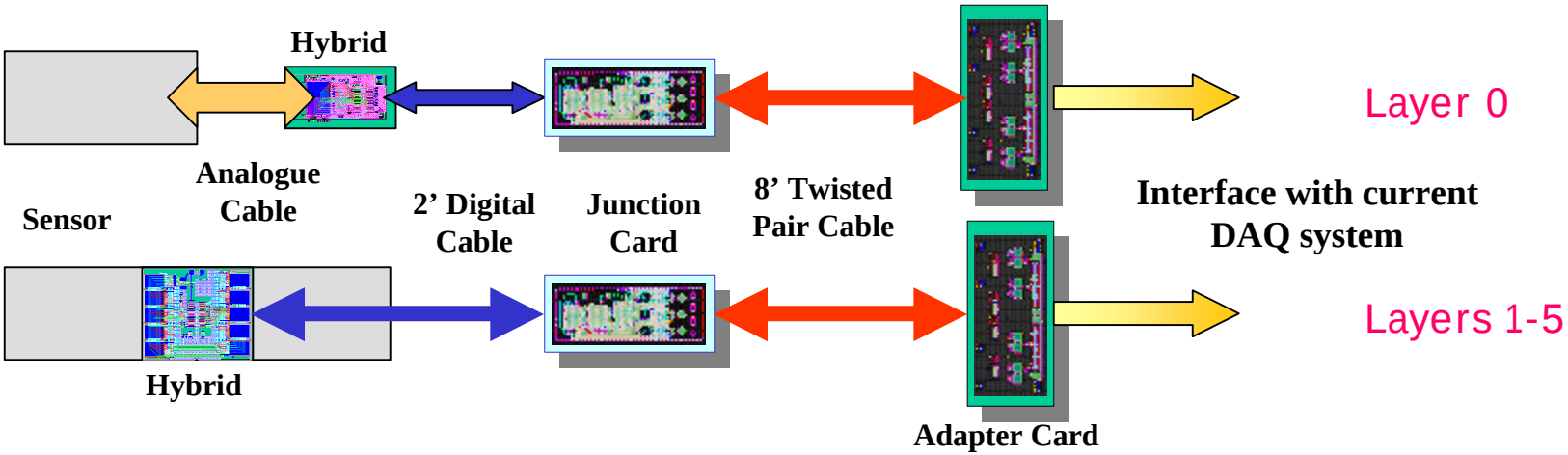
Readout Modules

- Each stave has four readout modules
- Readout module length varies with z-position.
  - For all layers, the modules closest to z = 0 are 200 mm long
  - Those furthest from z = 0 are 400 mm long
- Four Readout module types
  - 10-10 (axial, stereo)
  - 20-20 (axial, stereo)
  - Ganged sensors will have traces aligned (sensors are 10cm long)
- Module configuration



- Each hybrid has two independent readout sections serviced by one readout unit (double-ended hybrid)

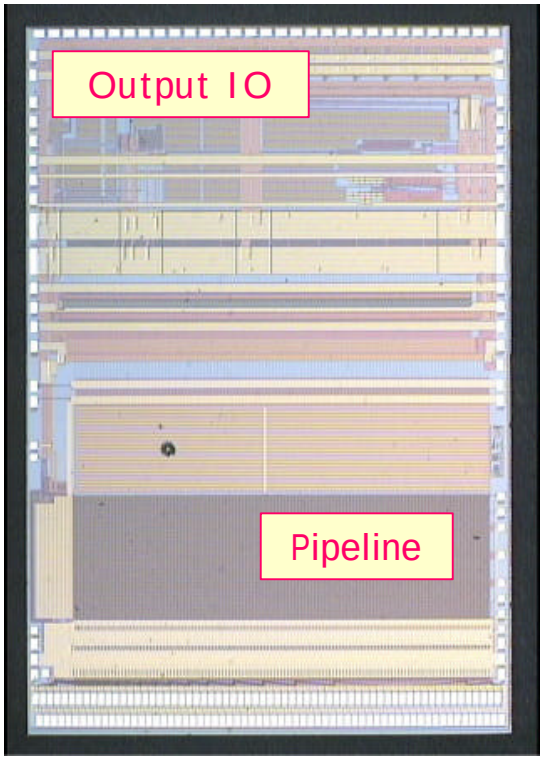
Readout Schematics



- Layers 1-5: Hybrids mounted on silicon
  - Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- Layer 0: Hybrids mounted off-board
  - Analogue Cable -> Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- SVX4 chips mounted on hybrid; employed in SVX2 readout mode

SVX4 Chip

- SVX4 full prototype chip received and being tested
  - 0.25 μm technology, intrinsically rad-hard
  - Successor of SVX2 and SVX3 chip
  - Both experiments use the same chip
  - Major success in commonality between CDF and DØ
  - DØ operates the chip in DØ-mode (dead-time)
  - Preproduction versions
    - Pre-amp (MOSIS 11/25/00)
    - Pre-amp and pipeline (MOSIS 06/04/01)
- SVX4 chip works !!
  - Major success and gives both projects an excellent headstart for full-scale testing of all elements of the detector
  - Tests at LBL
  - Tests at Fermilab
    - Stimulus setup



SVX4 Chip

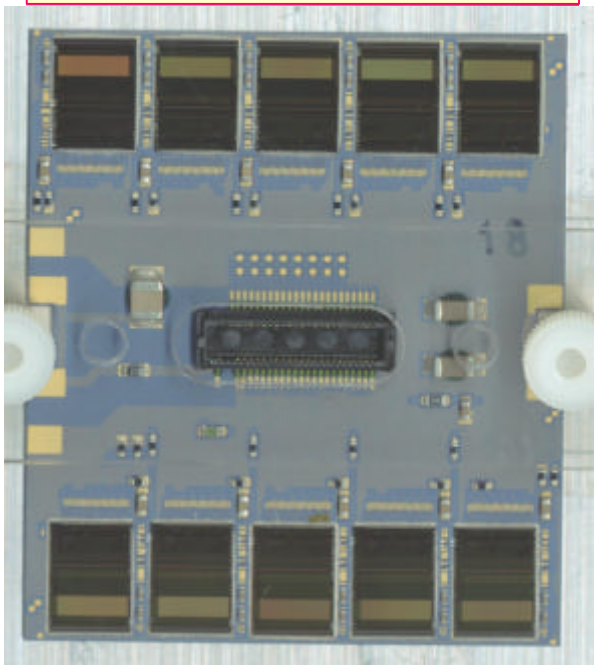
- Sample list of verifications done so far
  - ENC = 300e + 41e/pF C (Fermilab)
  - ENC = 600e + 32e/pF C (LBL)
- Known problems:
  - Add pull-up to USESEU
  - Add pullup or pulldown to DØ-mode
  - Pull MSB of ChipID high
  - Pedestal uniformity (ADC)
  - Change FECLK gating scheme for FE control in DØ-mode
- Tests to do
  - Frequency & duty cycle margin
  - Systematic test of all SVX4 specifications
  - Power consumption in various modes
  - SVX4 with silicon - black hole clamping feature, behaviour with various cables
- SEU studies already performed at UC Davis; irradiation with ^{60}Co-source to follow soon. No significant problems observed below 10 MRad.

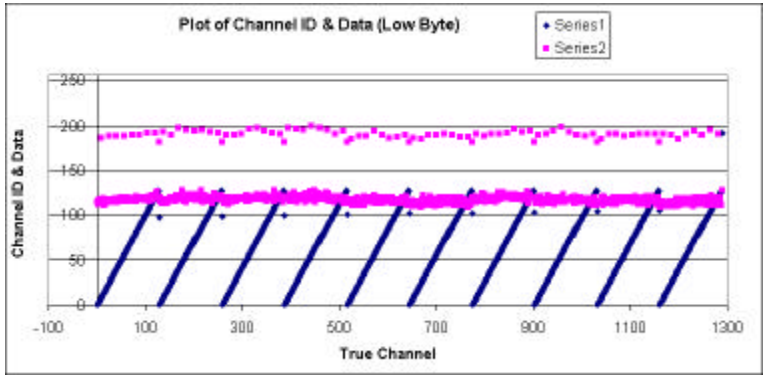
	Parameter	Spec	Met
Preamp	Gain	3mV/fC	✓
	Gain Unif.	< 5%	✓
	Risetime	60-100 ns	✓
	Rise adjust.	4 bits	✓
	Noise	2000e @ 40pF	✓
	Dyn. range	> 200 fC	✓
	Cal inject		✓
Pipeline	Reset time	< 20ns	✓
	Ped. Uniformity	<500e	
	Linearity	<0.25%	✓
	Diff. non-lin.	<0.5 LSB	
Outpt	Risetime	2ns - 4ns	✓
	Bus	bi-directional	✓
	Priorities In-Out		✓
Regstr/Cnt	Cells	SEU tolerant	
	Bit assignments		✓
	Resets		✓
	ch. 63 latch		✓
	D0 mode		

Hybrids

- Design:
  - BeO substrate with multi-layer circuit on substrate
    - 6 Au layers and 5 di-electric layers
    - Use screenprinting, min. via size 8 mils, ~10 mil spacing
  - Four types of hybrids
    - Layer 0: two-chip
    - Layer 1: six-chips, double-ended
    - Layer 2-5: ten-chips, double-ended
      - axial and stereo (only different in width)
  - Use 50 pin AVX 5087 connector, 2.5 mm high
- Prototypes
  - Layer 1
    - 18 hybrids received from CPT (CA)
    - all tested; electrically good; 7 stuffed
  - Layer 2-5
    - 23 axial received from Amitron (MA)
    - 50 axial, 50 stereo ordered from CPT
      - to arrive in November
  - In the process of qualifying both vendors
  - Hybrid readout with current readout system !

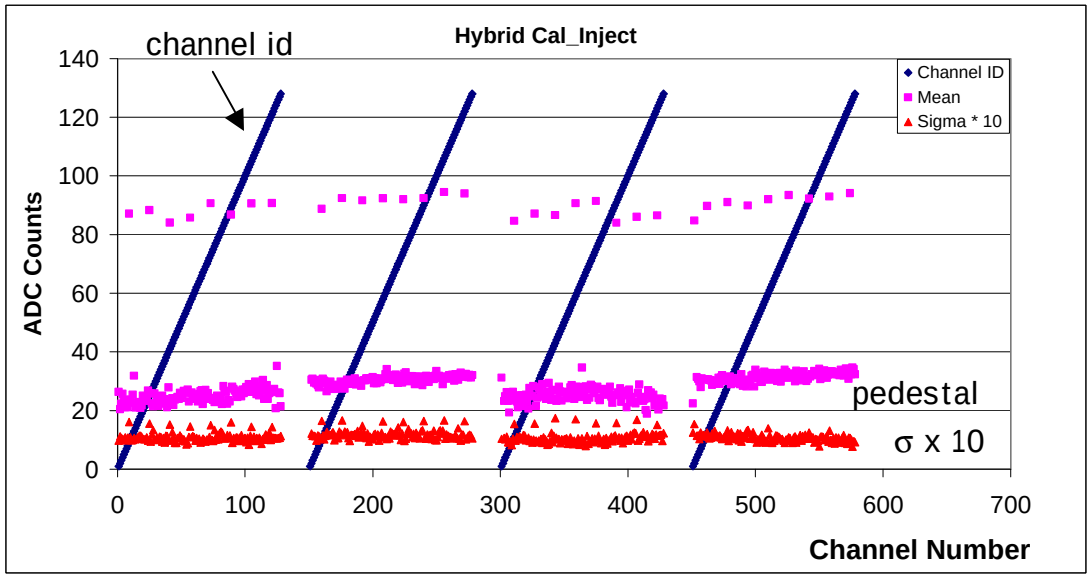
L2-5 axial Hybrid

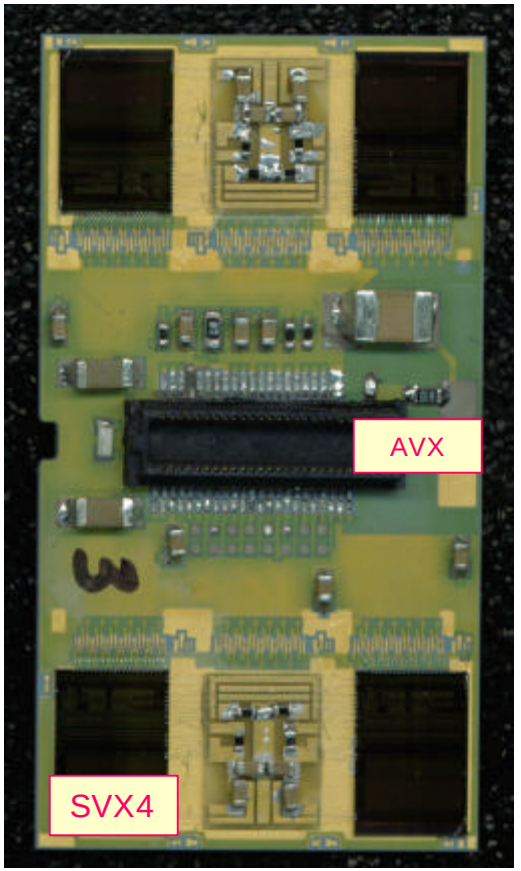




Layer 1 Hybrid

- One Layer 1 hybrid mounted with four SVX4 chips
- Readout with current DØ stand-alone readout system
  - All channels readout
  - Cal-inject set pattern of channels

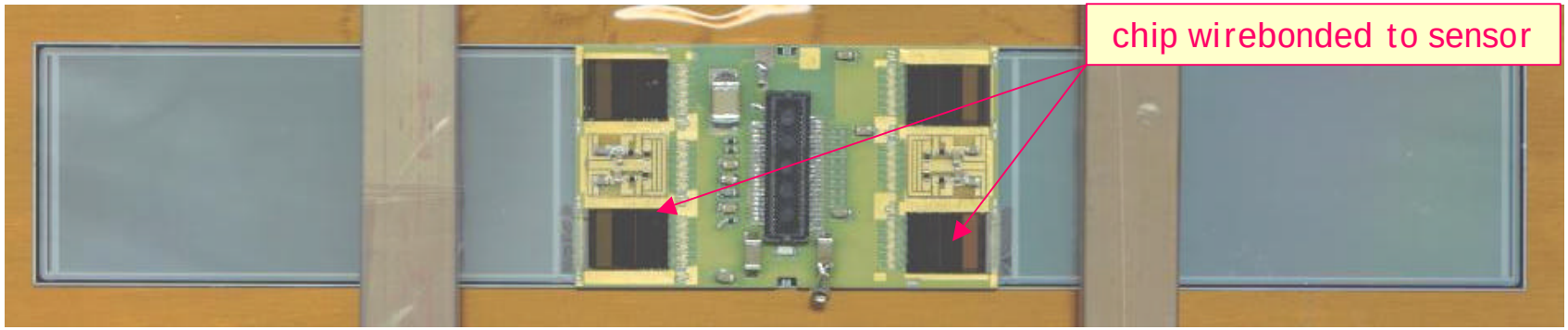


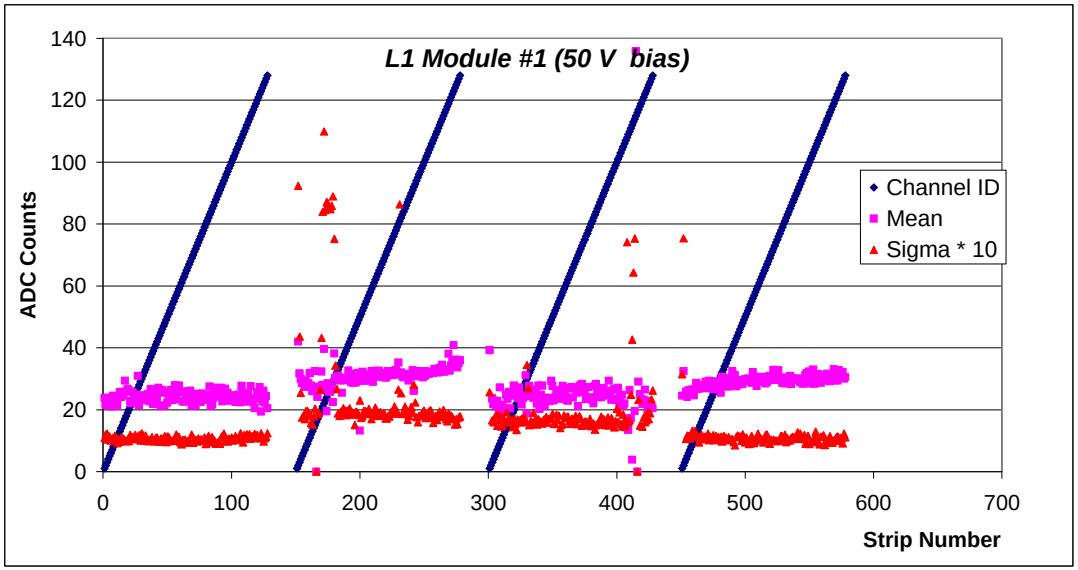


Major success on many fronts !

Layer 1 Readout Module

- Mount the hybrid on two Layer 1 ELMA sensors and try to read it out





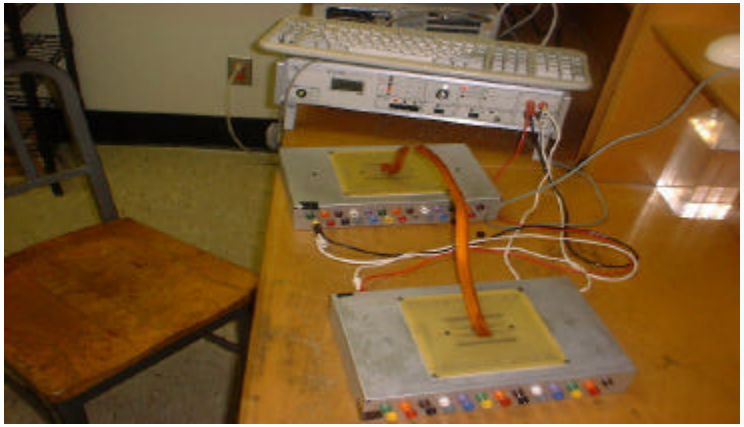
- Chip 2 and 3 wirebonded to sensor
- Detector biased to 50V
- Noise is higher for chip 2 and 3
- Sigma of pedestal
  ~ 1 ADC count (no sensor)
  ~ 1.8 ADC counts w/ sensor
  Meets spec.
- Proof of principle that Si + SVX4 + Hybrid + Readout System work !
- Tests continue

Digital Jumper Cable

- All layers use the same design done by KSU
  - 10-12 different lengths, max length ~ 1 m
  - Kapton substrate, total thickness 250 μm for L0-1, 330 μm for L2-5
  - HV on the same cable
  - AVX 50-pin connector on both sides
- Prototypes received from two vendors
  - Honeywell
  - Basic Electronics
  - All cables test ok
- Test Center being setup at Louisiana Tech
  - Impedance, Resistance, cross-talk

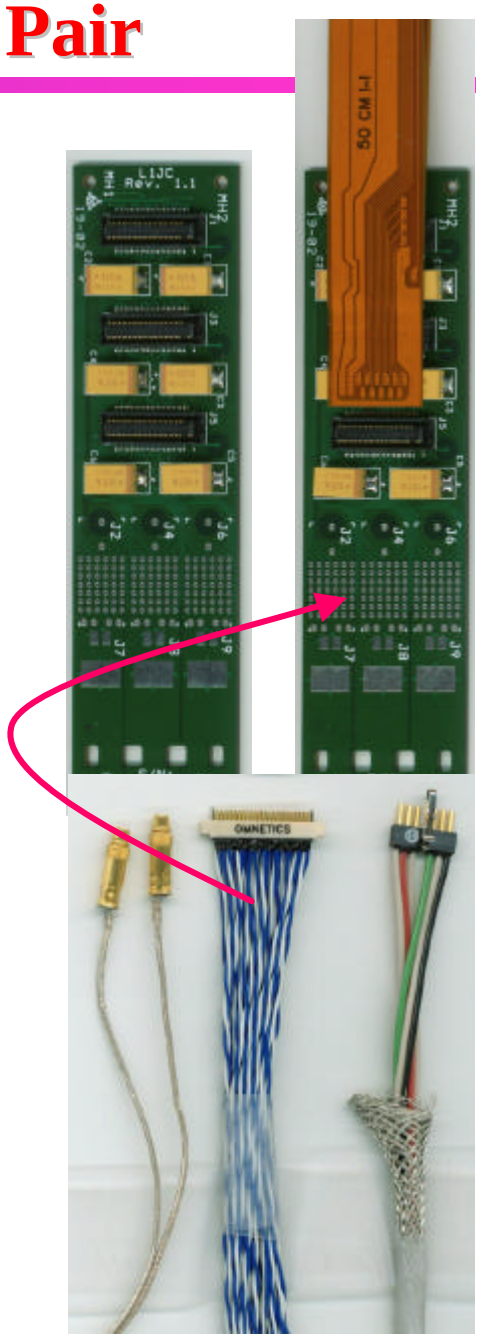
	L2-5			L0-1	
	50cm	100cm	35cm	50cm	100cm
Honeywell	10	20	10		
Basic Elc.	10			10	20

Pin #	Trace	Cable 1 Resistance	Cable 2 Resistance	*Specified in*: dl_section_27 nov01
37	AVDD	0.133 Ω	0.148 Ω	0.168 Ω/m
39	AVDD	0.133 Ω	0.139 Ω	0.168 Ω/m
45	DVDD	0.125 Ω	0.149 Ω	0.144 Ω/m
47	DVDD	0.126 Ω	0.136 Ω	0.144 Ω/m
7	GND	0.0715 Ω	0.0685 Ω	0.068 Ω/m



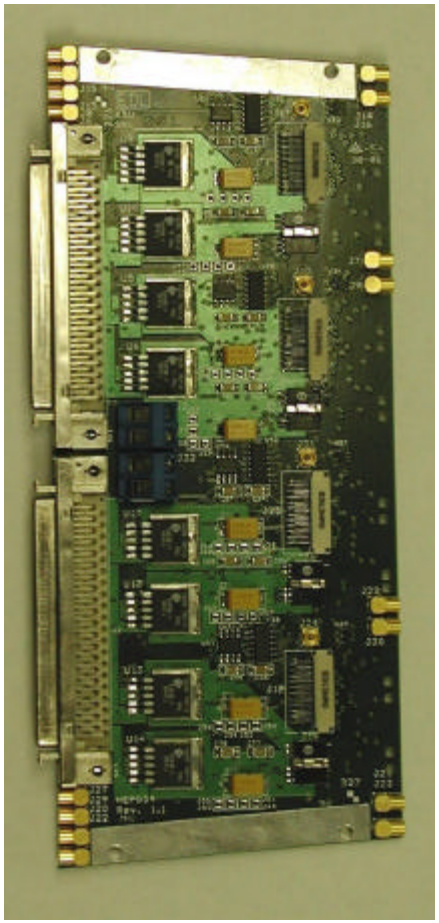
Junction Card and Twisted Pair

- Two types of Junction cards
  - L0/1: 3 hybrids → 1 junction card
  - L2-5: 2 hybrids → 1 junction card
- Designed by KSU
  - Card has no active elements
  - Receiving: 50-pin AVX connector
  - Outgoing: soldered twisted pair cable bundle
- Twisted Pair (Fermilab)
  - Power & HV lines : 6-pin Omnetics connector
  - Signal pairs : 44-pin Omnetics connector
  - Coax cables for clock signals
  - 5 cables received
    - 3 kits sent to BINP Novosibirsk for attachment
  - Vendors:
    - New England Wire and Omnetics
    - Considering Axon (France), Ecolab (Germany) (common with CDF)



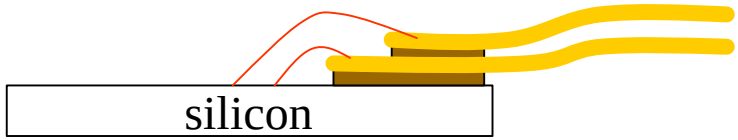
Adapter Card

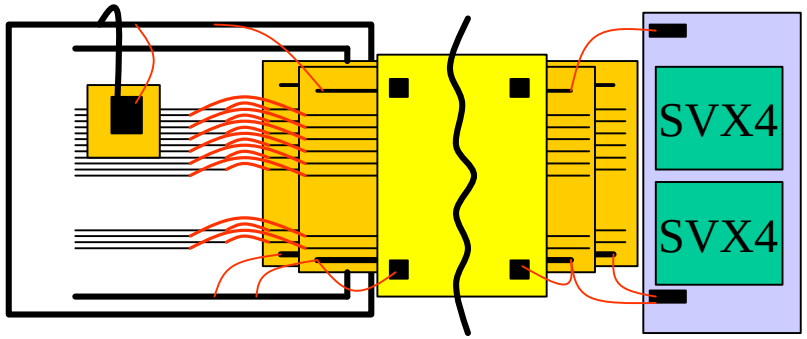
- Active Card, designed by KSU
  - Two voltage regulators per hybrid: analog and digital voltages
  - Differential-to-Single-Ended 2.5 to 5 V translation for SVX4 Data
  - 5 to 2.5 V translation for SVX4 Controls
  - Routing of Clock and HV
- Each adapter card has four or six channels
  - Input: twisted pair
  - Output 80-conductor 3M cable (existing)
  - 12 boards fabricated, one stuffed
  - Currently being tested
- Adapter Cards are mounted on face of calorimeter
  - Four rings of adapter cards (dubbed the “horseshoe”)
  - Now active element, needs cooling, ~700W per end
  - Cooling being studied



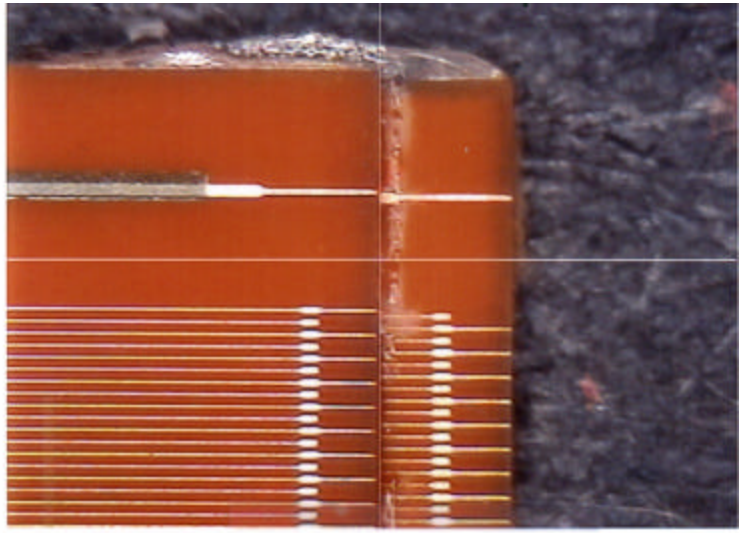
Analogue Flex Cables

- For layer 0 need low mass, fine pitch flex cables to carry analogue signals to hybrids
  - Technically challenging
    - **Trace width ~ 15 - 20 mm, pitch 91 mm**
    - **2 cables offset by 50 mm**
  - Noise determined by capacitance
    - For S/N > 10: **C < 0.55 pF/cm**
    - current design, with 16mm trace width -> 0.32 pF/cm



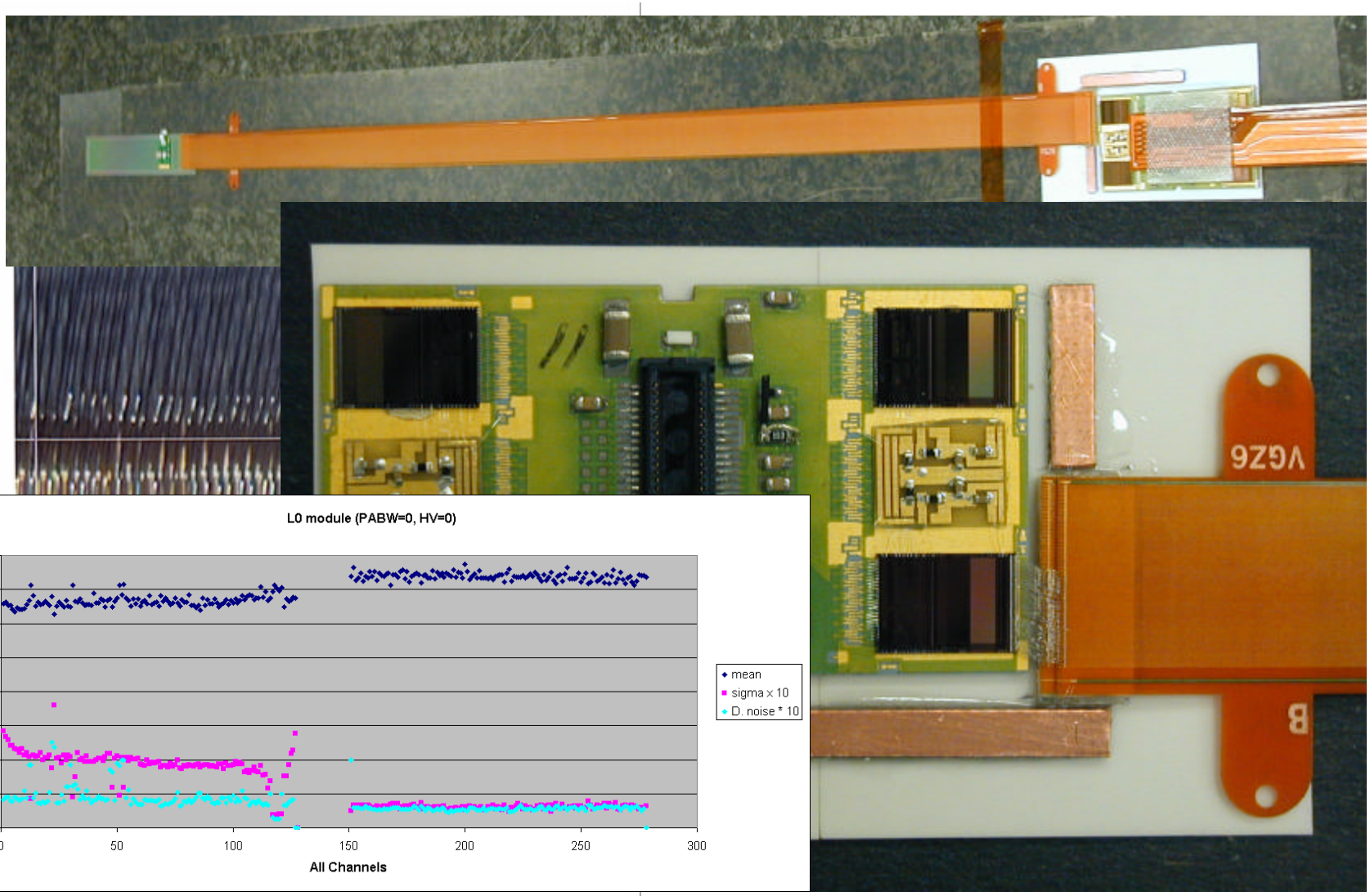


- Second prototype cables (Dyconex)
  - First batch: 12 cables.
    - Two had 2 open/shorts, remaining were good
  - Second batch: 27 cables
    - 16 perfect, 9 had 1 open, 2 = 2 open/short
  - Cables laminated and bonded
- Study of noise with various shielding configurations started



Layer 0 Module Prototype

- Built first full prototype of layer 0 module, layer 1 hybrid with SVX4



Summary of Prototyping

Component	Vendor	Design	First Prototype Ordered	First Prototype Delivered	Second Prototype Ordered	Second Prototype Delivered
L0 Sensors	ELMA	✓	✓	✓		
	HPK	✓				
L1 Sensors	ELMA	✓	✓	✓		
	HPK	✓	✓	✓		
L2 Sensors		✓	✓			
Analogue Cable	Dycx	✓	✓	✓	✓	✓
L0 Hybrid		✓	✓			
L1 Hybrid	CPT	✓	✓	✓		
L2A Hybrid	CPT	✓	✓			
	Amitr.	✓	✓	✓		
L2S Hybrid	CPT	✓	✓			
Digital Cable	Honey	✓	✓	✓	✓	✓
	Basic	✓	✓	✓	✓	✓
Junction Card		✓	✓	✓		
Twisted Pr. Cable		✓	✓	✓		
Adapter Card		✓	✓	✓		
Purple Card		✓	✓	✓	✓	✓
Test Stand Elctr.		✓	✓	✓		

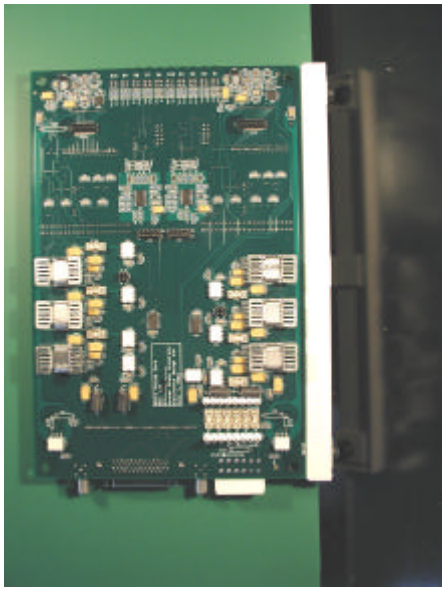
- Except for HPK sensors and Layer 0 hybrids, have prototypes of all components in hand and no major issues have been encountered so far

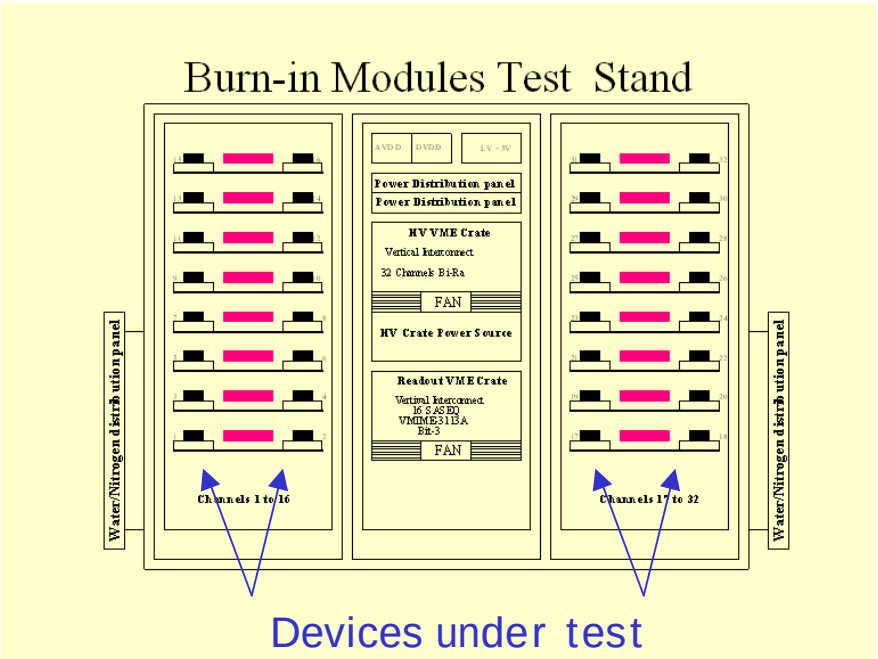
Vertical Slice Tests

- Readout System at SiDet identical to the readout system used in the experiment; two systems will be erected:
- "1% Test"
  - For functionality test of individual components up to a total of 8
  - Will reside in burn-in area at SiDet; operational October '02
- "10% Test"
  - For functionality test of multiple components; operational spring '03
  - Will reside in the Lab C clean room as was done in Run IIa
  - Tests scheduled
    - Sector test of Layer 0
      - 3*6= 18 hybrids, i.e. 3 ϕ-sectors; study noise with analogue cables
    - Sector test of Layer 1
      - 3*6 = 18 hybrids, i.e. 3 (6) ϕ-sectors; study and monitor operating conditions
    - Full sector test
      - Minimum of 5 full staves readout, i.e. 20 hybrids
      - Combination of Layer 0, Layer 1 and Staves
- The 1% test is currently being setup at SiDet to study the SVX4 chip with the full readout system

Burn-in and Purple Card

- Burn-in is performed with stand-alone sequencer system; UIC responsible for setup and running
  - The equivalent of the Adapter Card is a Purple Card
- Purple Card designed by KSU
  - Uses same components and schematic solutions as AC
  - Each card has 2 channels
  - 12 boards fabricated, 6 stuffed, 2nd proto. Oct.
  - Note: L1 and L2A hybrid, L1 and L0 readout module used this card





- Test stands for testing first components being setup at SiDet
  - Two hybrid burn-in test stands, 16 channels each
  - Two module burn-in test stands, 32 modules each
    - with associated cooling
  - Two burn-in cycles per week

Summary and Conclusions

- A lean and robust Silicon Tracker has been designed to pursue the physics goals for Run IIb
- Project has already various fully working electrical modules with SVX4 readout
- Project has prototyped all major components of the design (except L0 hybrids) and nearly all meet our specifications
- Project has a strong technical team with a tight grip on all technical issues
- All L3 managers have a thorough understanding of the critical issues and the effort involved to succeed with this project; most are Run IIa veterans
- Many university groups involved, all with clearly delineated responsibilities

- We are ready to move beyond the prototyping stage