**Report of TAB/GAB Production Readiness Review**
**October 7, Nevis Labs**

I. Bertram, D. Edmunds, R. Hirosky (chair), J. Steinberg

Report dated 10/15/04

Executive Summary:

The committee was charged to evaluate a number of readiness criteria for the TAB and GAB boards, many of which extend naturally into installation and commissioning phases of the boards. We comment on these general issues related to the successful completion of the project, though most of our focus was given to the question of readiness for assembly of the TAB/GAB boards. The committee agrees that this is an important decision point for proceeding towards completing the calorimeter trigger upgrade on time. After considering design issues and results of test procedures, we feel that **the current design is ready for assembly to begin**.

- Numerous I/O tests have been performed to verify all connections on both boards. TAB outputs to the L1 muon system were verified in-situ to test the data path to the future CALTRACK. Latencies were also verified at 630ns for the jet algorithm, w/in the allowable latency period. The Tau algorithm is expected to have too much latency to send to CALTRACK. The latency of the electron algorithm has not been verified, but is expected to be w/in limits for use w/ CALTRACK. Given its relative complexity to the jet algorithm, its latency is expected to be only slightly longer and consistent with allowable latencies for input to CALTRACK.
- While, it is not possible to test for unexpected effects that might appear in a fully connected TAB before ADF boards are produced we feel that good design principles were employed and that tests with 10% of the TAB inputs driven were performed carefully. The TABs should be tested with all inputs driven as soon as sufficient numbers of ADF boards are in hand.
- Although the PCB's have been on hand for around 12 months, gold plating and hermetic storage should have provided good resistance against board decay. We recommend proceeding cautiously in the assembly of these PCBs in consultation with the assembly plant. Suggestions are: (1) Request that the assembly company examine the raw pcb's for "solderability" before proceeding. (2) Request that the assembly company examine the first card through the assembly line for any problems caused by the 1 year of raw pcb storage before sending the rest of the cards through the assembly process.
- Sufficient engineering resources are available to complete the firmware projects, looming competition with ATLAS projects should not affect TAB/GAB development as long as we proceed on the project without significant delay

The reviewers were asked to determine:

1. *if the design and prototype technical performance meet the requirements of the baseline design.*

2. *if the resources are adequate to produce the TAB/GAB system on schedule and on budget. As part of this, you are asked to determine if the technical, financial, and personnel contingency are adequate to provide reasonable assurance of successful project completion.*

The *specific topics evaluated* and the committee's detailed comments follow.

***1. Hardware:*** *Review the design and determine if it meets specifications. What tests have been done to prove it meets specifications and what changes are needed from existing to production modules? Check the grounding and shielding plans, cooling needs and plans, power supplies, installation and maintenance plans as well as the adequacy of spare boards and parts. Comment on the test stand planning and needs.*

Remarks:
A significant amount of the hardware discussion focused on electrical tests of the boards. We note the following:

- All input / output connections have been tested at a minimum for proper connectivity.
    - TAB inputs have been tested w/ a diagnostic sender board capable of driving three input channels simultaneously. The board was tested with numerous combinations of inputs driven, both on channels w/in a single connector and across connectors.
    - TAB input channels have been shown to work w/ ADF outputs.
    - Bitwise comparisons were done on O(hundreds of events) to verify TAB jet clustering FW.
    - All GAB connections have been verified, but only under test bench conditions.

- It has not been possible to test the function of a TAB with all 30 input channels driven simultaneously, due to lack of hardware to generate the inputs (preferably ADF's). A possible risk is that 30 input PLLs in the receiver chips will suffer some sort of channel-to-channel interference when all are running together.
    - While, it is not possible to test for unexpected effects that might appear in a fully connected TAB before ADF boards are produced we feel that good design principles were employed (all inputs implement DPMs to synchronize data, extensive ground/power planes, and triple bypassing on all FPGS power inputs) and that tests with 10% of the TAB inputs driven were performed carefully.
    - The TABs should be tested with all inputs driven as soon as sufficient numbers of ADF boards are in hand.

- TAB outputs to the L1 muon system were verified in-situ to test the data path to the future CALTRACK.
    - Muon accept rates were shown to be correlated with fake objects rates from the TAB. This demonstrates the essential connectivity between the TABs and CALTRACK.

- Latencies were also verified at 630ns for the jet algorithm, w/in the allowable latency period.
    - The Tau algorithm is expected to have too much latency to send to CALTRACK. It will only be available for L1CAL tiggers.
    - The latency of the electron algorithm has not been verified, but is expected to be w/in limits for use w/ CALTRACK. Given its relative complexity to the jet algorithm, it's latency is expected to be only slightly longer.

- The VME/SCL card has been available and working for more than a year.

In addition to the above remarks, Dan Edmunds has provided a summary of further technical discussions that followed the PRR presentation:

> We began the discussion Thursday afternoon with Bill going through the details of how the TAB and GAB establish data transmission synchronization both at the Frame level (aka Event level) and at the Bit level. The requirement of Frame level synchronization is obvious (all parts of the system must be working on the same event). Bit level synchronization in the ADF to TAB data transfer is taken care of internally by the Channel Link chips. The Bit level synchronization in the TAB to GAB data transfer is taken care of by FPGA firmware on these cards. The high speed serial data transfer from the TAB to the GAB and the serial data processing in both the TAB and GAB are the keys to making this part of the Run 2B L1 Cal Trigger practical to build with current technology.
>
> In the TAB and GAB a cyclic 1:159 Beam Crossing Number is carried along with the event data through the various processing stages. In the current firmware this "BX" number in the TAB and GAB does not match the Tevatron BX from which the associated event data came. Rather, currently a correction is done at the end and then the event alignment is verified. We discussed the advantages of modifying the firmware so that the "BX" number carried through the various TAB GAB data processing stages matches the Tevatron BX from which the data came. Jaro and Bill are going to look at the firmware to see if there are any serious problems in implementing a cyclic 1:159 "BX" number that matches the Tevatron BX from which the event came. I have written and today will send to Hal a detailed follow up note about this. All of this involves just FPGA firmware - not circuit board trace layout.
>
> The second major topic Thursday afternoon was to review the layout of the section of the TAB card that receives 30 Channel Link connections from the ADF cards. This is a critical section TAB card because:
>
> - other serial data transfer systems at Fermi have had trouble when many channels are instanced on a single card
>
> - and because, due to the ADF card being behind schedule, the engineers at Columbia have not been able to full test (i.e. all channels operating at once) this section of the TAB card.
>
> The layout of this part of the TAB card (actually of all the TAB card) looks clean and well thought out. Everything that is recommended by the manufacturer of the Channel Link chips to insure their proper operation has been done. Correct layout of the high speed clock and data traces, full wide bandwidth power supply bypassing, and quiet independent power and ground for the Channel Link PLL's have all been implemented. All currently practical testing of this part of the TAB card has been done. There is nothing else that I know of that could be done on the TAB cards to insure the proper operation of the ADF to TAB Channel Link connections.
>
> We concluded the afternoon with an overall visual review of both the TAB and GAB cards and discussed the board assembly company that would be doing this assembly work. Everything on both cards looks well thought out and cleanly implemented. Bill and Jaro have an established relationship with a board assembly company that has done good work for them on this type of cards in the past.
>
> There is nothing that I know of that should hold up giving Hal the immediate "OK" to proceed with the assembly of these cards.

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***2. Software*** *for operating, testing and configuration*

Remarks:
Several projects remain for operations of the boards:

- TAB
  - Tau algorithm not yet verified
  - Finalize choice on EM algorithm, most likely to use ATLAS algorithm. Some further discussions should be held w/ trigger and physics groups. Notably, some groups are very resistant to giving up single tower EM triggers.
  - Monitoring software/firmware needs development
  - Full TAB simulation code needs development
  - Develop firmware for L2 output
- GAB
    - Develop FW for trigger terms
    - Develop software/FW for Monitoring
    - Develop firmware for L2 output

***3. Interfaces:*** *(to ADF, TFW, Cal-track, L2, L3, ...) hardware, designs and tests or plans for tests*

Remarks:

- successful I/O tests have included:
  - writing of data into each of 30 TAB input channels (though only 3 at a time)
  - GAB to VBD
  - GAB to muon system ( to test input path to be provided by L1 Cal Track)
- data format is specified for Gab-> L1 Caltrack
- draft of data format for L2 output
- data format for L3

***4. Personnel*** *for production and testing. Comments on personnel and planning for installation and commissioning are encouraged, but should not hold up the board production.*

Remarks:
1 postdoc working on simulation with plans to move to hardware testing.
2nd postdoc and student to join in commissioning

Sufficient engineering available at Nevis to complete FW. However, competition from ATLAS necessitates a prompt start on the above FW projects.

Personnel resources seem sufficient to complete hardware installation and commissioning.

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***5. Timeline*** *for production, testing, integration tests, installation and commissioning.*

Remarks:

| Production: | | start | end |
|---|---|---|---|
| Delivery of remaining components: | 2W | 10/11/04 | 10/22/04 |
| Assembly Boards/Purchasing Admin: | 6W | 10/11/04 | 11/19/04 |
| Test at Nevis: | 12W | 11/22/04 | 02/11/05 |

***6. Installation Plan***

Remarks:
Installation and commissioning are reviewed in the SC-IPC report. The review did not cover physics commissioning plans. Commissioning is covered in the recent SP-IPC report.

***7. Documentation***

Remarks:
Available documentation includes the trigger TDR, webpage drafts of : TAB-to-CALTRACK communication, L2 output, proposed and-or terms.
Bit level documentation of all registers required. More formal documentation will need to follow.

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# Appendix A

**Charge to the Review Committee for the Production Readiness Review of the DZero Run IIb Level 1 Calorimeter Trigger TAB/GAB boards**

V. O'Dell
DZero RunIIb Project Manager
Oct. 4, 2004

Thank you for agreeing to serve on the DZero Run IIb TAB/GAB Production Readiness Review Committee. The purpose of this review is to determine:

1. if the design and prototype technical performance meet the requirements of the baseline design.

2. if the resources are adequate to produce the TAB/GAB system on schedule and on budget. As part of this, you are asked to determine if the technical, financial, and personnel contingency are adequate to provide reasonable assurance of successful project completion.

Specifically, items we would like to cover for each board (many items can be combined across all or part of them):

**Hardware:** Review the design and determine if it meets specifications. What tests have been done to prove it meets specifications and what changes are needed from existing to production modules? Check the grounding and shielding plans, cooling needs and plans, power supplies, installation and maintenance plans as well as the adequacy of spare boards and parts. Comment on the test stand planning and needs.

**Software** for operating, testing and configuring

**Interfaces:** (to ADF, TFW, Cal-track, L2, L3, ...) hardware, designs and tests or plans for tests

**Personnel** for production and testing. Comments on personnel and planning for installation and commissioning are encouraged, but should not hold up the board production.

**Timeline** for production, testing, integration tests, installation and commissioning.

**Installation Plan**

**Documentation**

While this review is specifically to decide if the TAB/GAB boards are ready for production as designed, it is beneficial to review them in the larger context of the L1 Calorimeter Trigger system. However, this review should focus on the aspects that would affect the TAB/GAB design or production. We will be organizing an additional review in the Spring of 2005 for installation, commissioning and operating the L1 Calorimeter Trigger System. The latter review will allow us to examine system tests in the wider system context.

The TAB/GAB review date has been set for Thursday, October 7, 10am – 4:30 pm at Nevis. A web page for the review has been set up at:

http://www.nevis.columbia.edu/~evans/l1cal/meetings/041007_prr/info.html

I would like to ask that the Committee submit a report summarizing their findings to me by Thursday, October 14.

Once again, thank you very much for agreeing to serve on this committee. The contribution of your time and experience is very much appreciated.