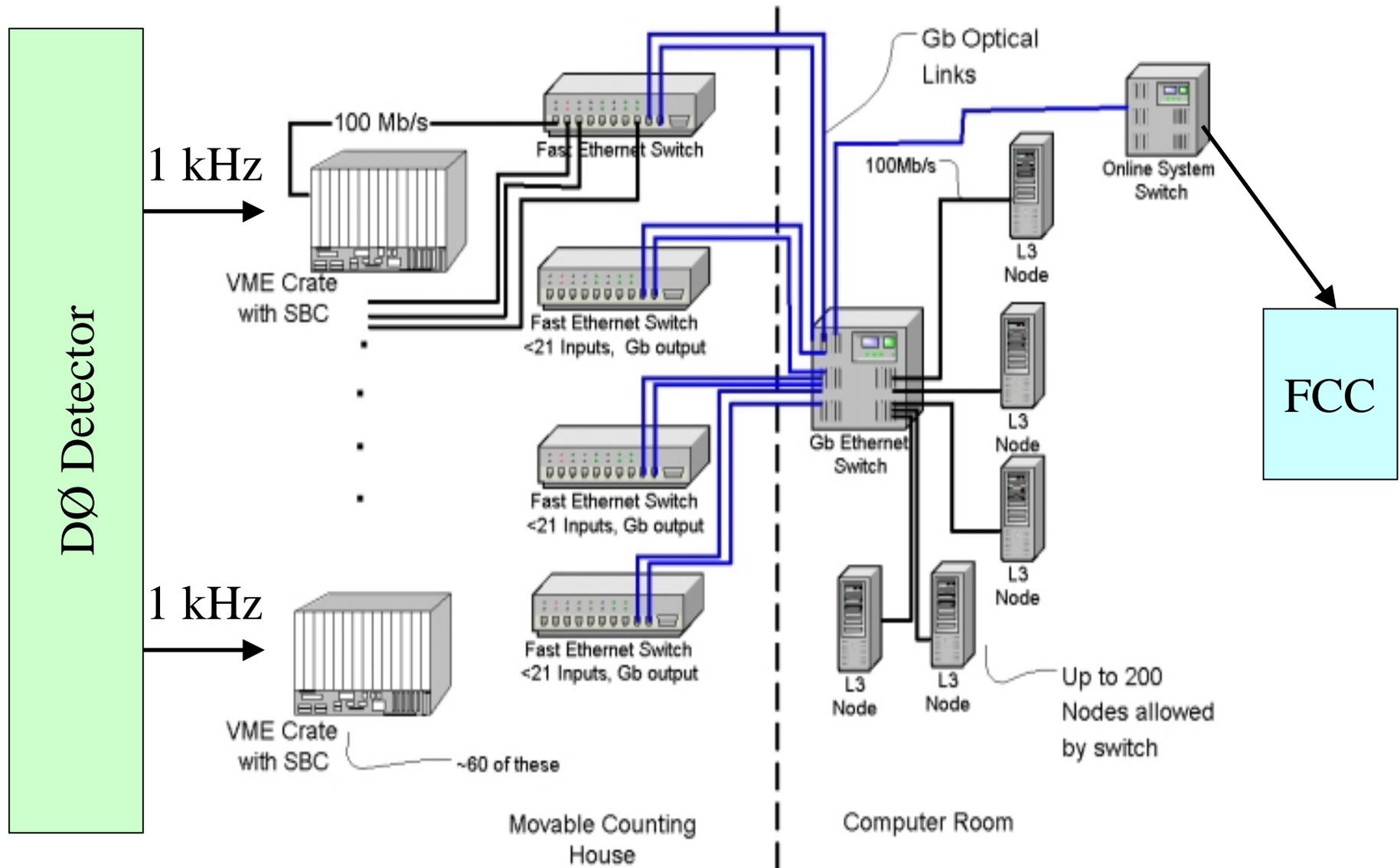


# DØ DAQ Status

June 17th, 2002

S. Snyder (BNL), D. Chapin, M. Clements, D. Cutts,  
S. Mattingly (Brown), B. Angstadt, G. Brooijmans,  
D. Charak, G. Guglielmo, M. Johnson, S. Fuess,  
A. Kulyavstev, M. Mulders, R. Rechenmacher, D.  
Slimmer, D. Zhang (Fermilab), R. Hauser (MSU),  
P. Padley (Rice), A. Haas, G. Watts (Washington)

# Commodity DAQ System



June 17th, 2002

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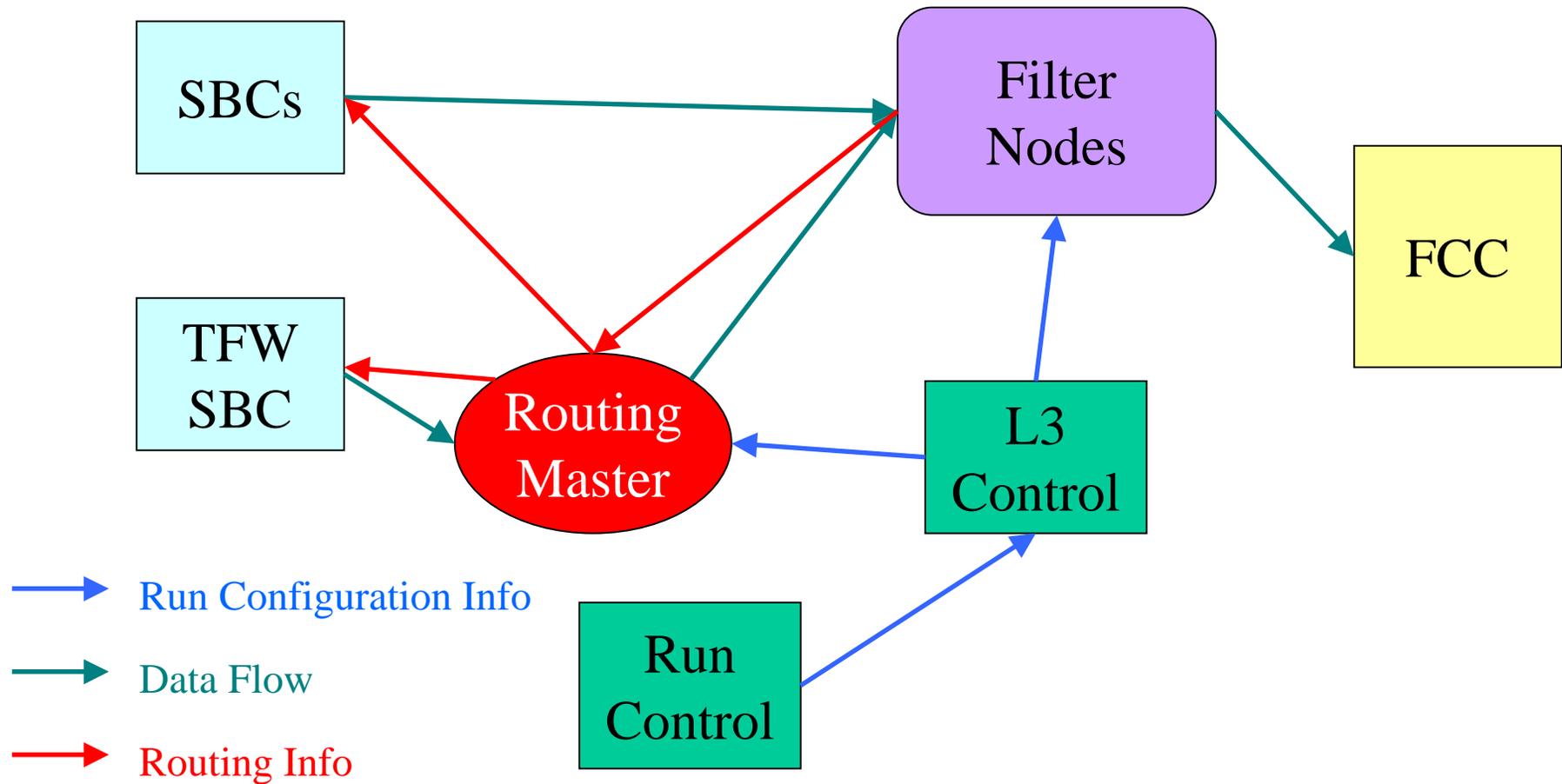
- Single Board Computers (SBC) read the event data over the VME bus, and send it to a Level 3 node over Ethernet, according to routing instructions received from the *Routing Master*
- The Routing Master program runs on an SBC in a special crate receiving data from the Trigger Framework (and can disable individual trigger bits if needed).
- Event building is done in the Level 3 nodes.

# Hardware Components

- Single Board Computers:
  - require good processor speed, enough memory, Ethernet, fast VME access, two channels of digital I/O (readout handshakes).
  - chose VMIC 7750: 933 MHz PIII, 128 MB RAM, 2 Ethernet ports, Tundra Universe II for VME-PCI interface. Added BVM digital I/O card.
  - One custom component: passive extender board to fit 6U SBCs in 9U crates.

- Switches:
  - Cisco 2948G (“concentrators”): 100 Mb/s (copper) input from SBCs, Gb (fiber) output. Limit to 10 SBCs per fiber → no congestion possible
  - Cisco 6509: capable of handling 16 GB/s (average expected rate is 250 MB/s). Gb fiber in (from 2948G’s), 100 Mb/s (copper) out to Level 3 Nodes, with 112 MB of buffering in the switch per 48 nodes.

# Software Components

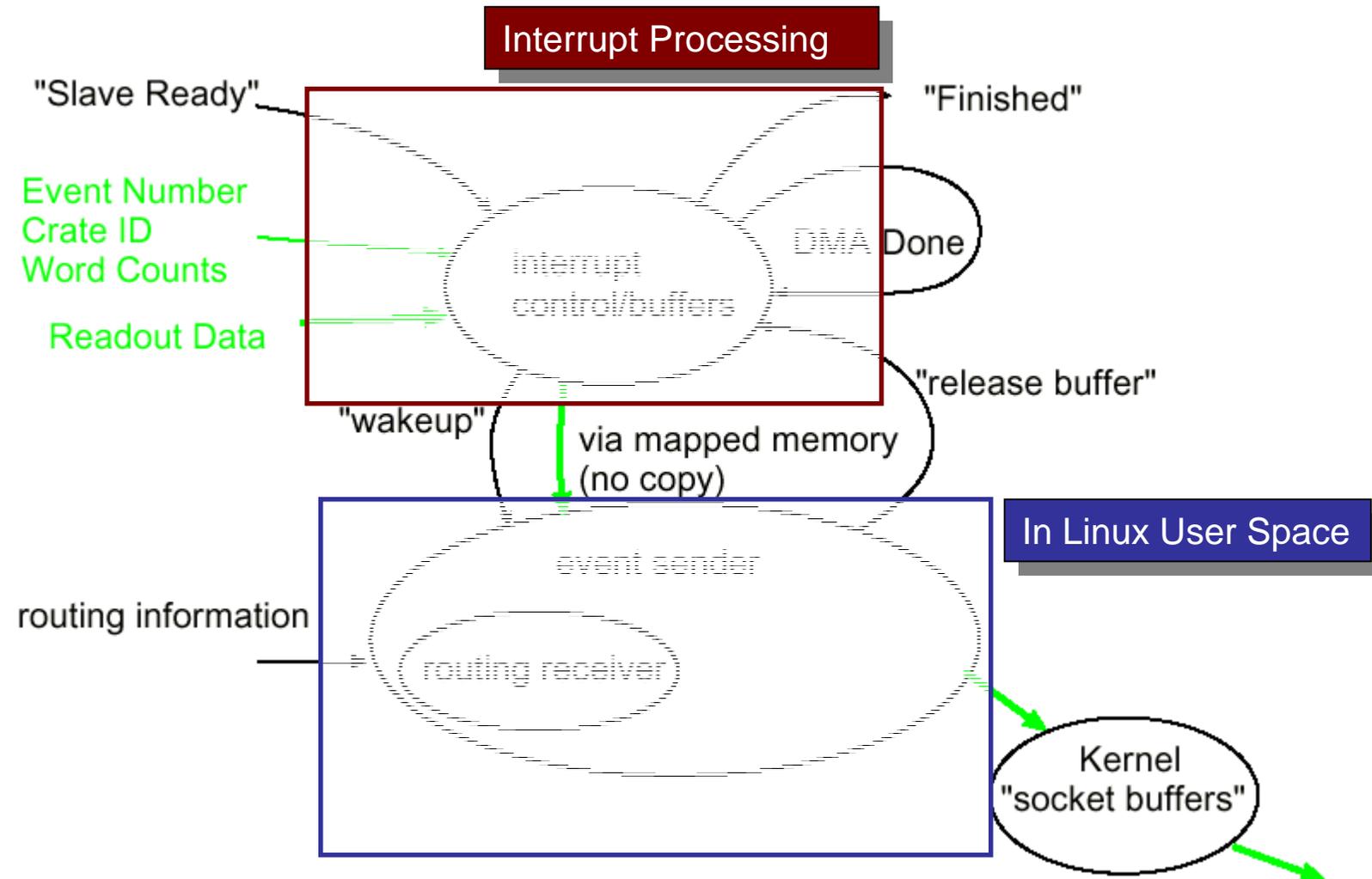


June 17th, 2002

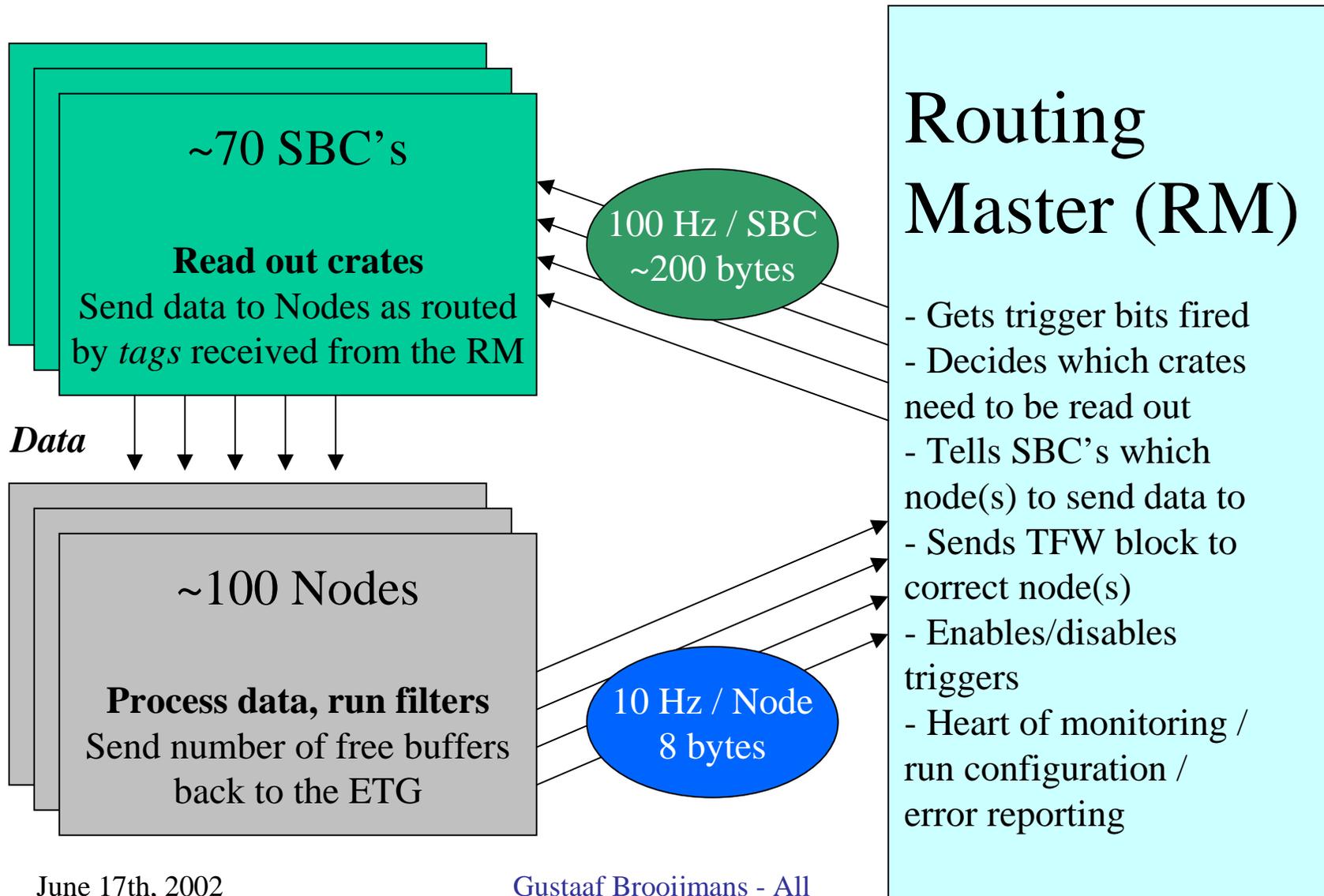
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# Single Board Computer Software



# Routing Master



June 17th, 2002

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# Status

- Go-ahead given at the end of December
- Software conversion made on March 26th
- Finished replacement of VBD's with SBC's on June 5th (6 weeks ahead of schedule)
- Started L3 input rate increase (from previous 100 Hz):
  - in April, demonstrated all readout crates can go at at least 1.17 kHz for evenly spaced triggers
  - For random triggers, problems in L1 muon readout around 550 Hz. Problem is understood (buffering of L2 accepts), working on firmware

# Prospects

- Increase in L3 input rate during physics running requires
  - DAQ and front-end capability
    - Can do 550 Hz now, don't expect many new problems between 550 Hz and 1 kHz
  - Adequate rejection at L3 (we were running at 100 Hz in, 25 Hz out, now want to go 1 kHz in, 50 Hz out → need to increase rejection by 5)
    - Studies being done, strategy being formulated
  - Enough cpu capacity in L3 farm
    - Benchmark tests done, purchasing additional 32 nodes (total will be 80)

# Summary

- Hardware and software conversion of the DAQ system are complete
- Commissioning increase in L3 input rate:
  - Working on L1 muon problem
  - Developing L3 trigger strategy
  - Purchasing additional L3 nodes to satisfy cpu requirements
- My best guess: DØ operating at  $\mathcal{O}(500)$  Hz in, 50 Hz out in July & August, 1 kHz/50 Hz starting in September