

1 Introduction

Because of the difference in time of flight (TOF) between D0 collision point and FPD spectrometers, an adjustment of their time is required, so FPD will match the Trigger Manager timing scale. The solution for the quadrupoles has been found, using a PLD device attached to a normal sequencer¹.

A new third delay is required in order to read the dipoles, which has a difference of 60 nanoseconds compared to the quadrupole ones.

One solution is around to find another sequencer and put a device that provides with the 3rd delay. However, it is not feasible because there is not space for a second sequencer in our crate.

Other way to find the solution can be drawn from an 8-MCM Analog Front End board (AFE)² approach. This board has a specific PLD in charge of generate the clock signals based in the Sequencer information³.

2 AFE Clock Gen module

This module is embedded in a Lattice PLD⁴. The design is quite flexible, so the delay can be modified in a very simple way. Figure 1 shows a panoramic picture of the relationship between 'Clock Gen' and the involved timing in the MCM control signals. The modifications that FPD requires must be located in two parts of the module: 'top-level' schematic and 'Reset Timing' ABEL⁵ code files.

2.1 Top-level

The top-level schematic file contains the routing between all of the entities that constitute the Clock Gen module.

¹ "Summer Project 2002." Anton Smith.

² Engineering Note 'a1000612'. "Software/Firmware map of 8-MCM Analog Front End Board (AFE) and Microcontroller Command List." John T. Anderson. June, 2000

³ Engineering Note 'a1000107'. "D-Zero CFT 8-MCM Analog Front End board. Design Specification." John T. Anderson. January 2000.

⁴ IspLSI2128VE-180LT176: Lattice PLD.

⁵ ABEL: Advanced Boolean Equations Language

The connections in which we are interested in are routed between the input coming from the delay line and the Clock Gen module. The delay line divides the Master XING signal in a fixed number of delayed signals, depending of the devices taps⁶, which are used into the 'SIFT multiplexor' module.

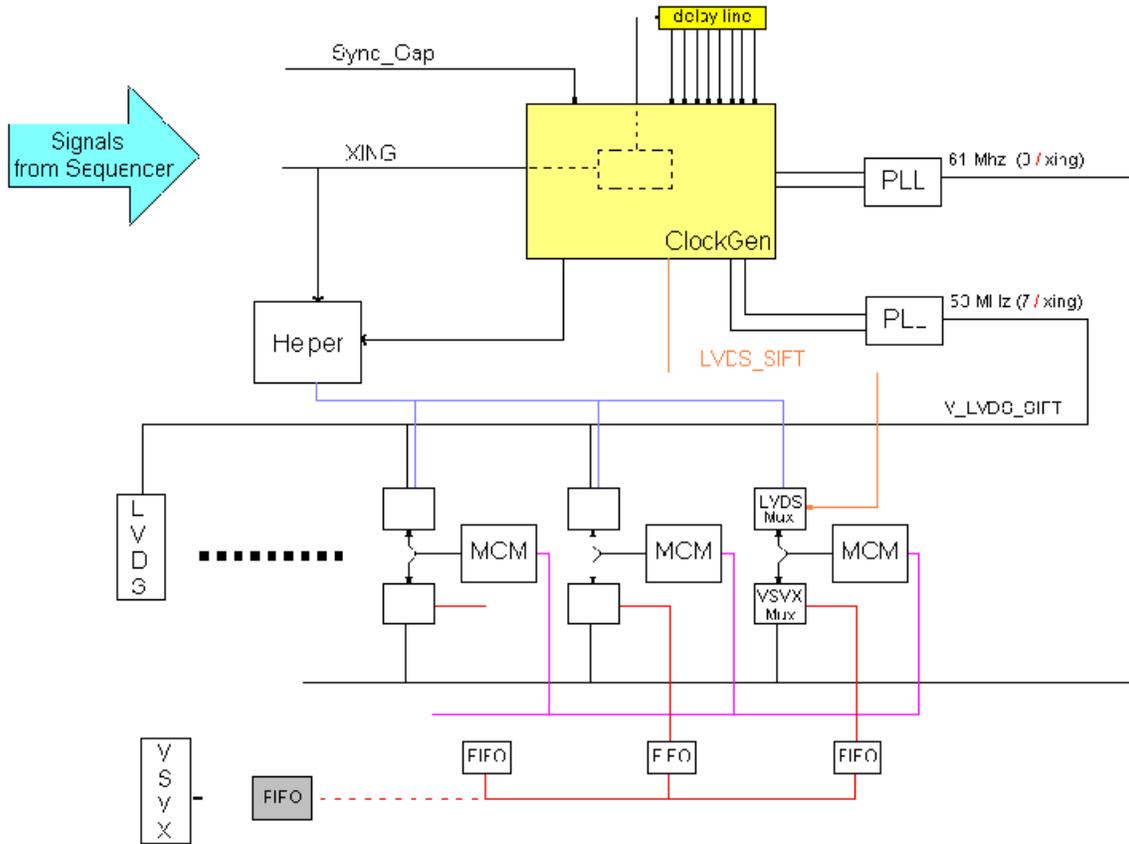


Figure 1 Clock Gen. – General Description

The SIFT multiplexor has the required logic in order to establish the following signals: 'Pre-Amp reset', 'Sample and Hold' and Read. These signals are used by the SIFT chips.

Figure 2 shows the required delay line taps, new values in red, for the 60 nanoseconds adjustment.

⁶ 3D7110: Monolithic 10-tap fixed delay line. Data Delay Devices, Inc.

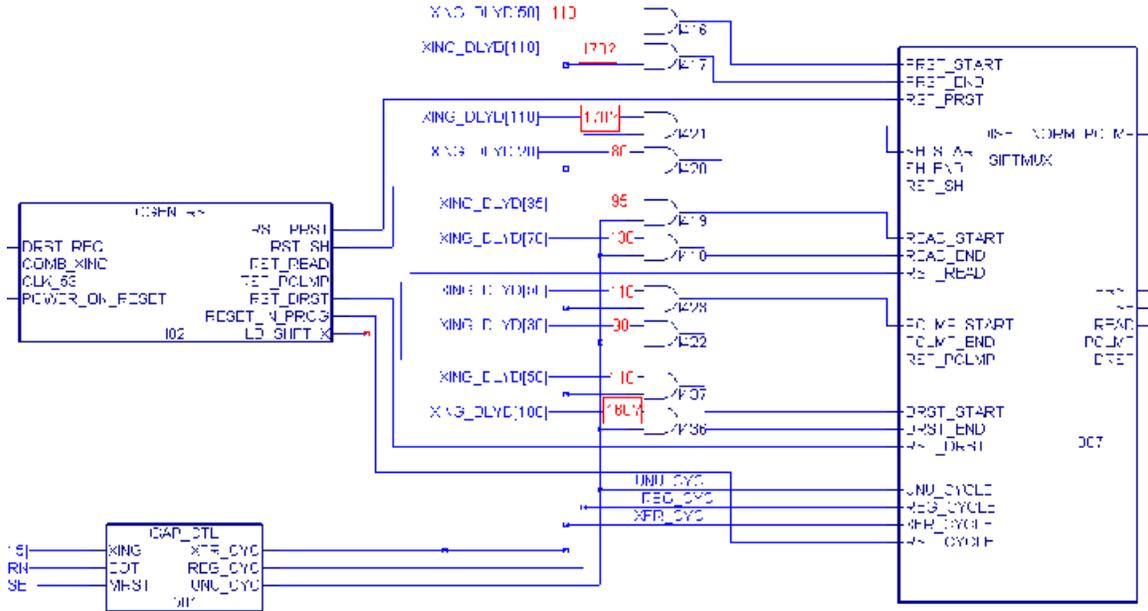


Figure 2 Changes in Clock Gen Top-Level File

2.2 Reset Timing

This module is a Finite State Machine (FSM) described in ABEL. It is in charge of the control the synchronization with the Cosmic and Sync Gaps, which work as resets. Also, this FSM must look for the XING signal that will provide the exact time for start the process.

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