

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WB\$	Resource Names
1	FIBER TRIGGER ELECTRONICS	299.4 w	10/3/94	9/25/00		As Soon As		
2		0.2 w	10/3/94	10/3/94		As Soon As F		
3	SVX II	168.6 w	10/1/96	3/8/00		As Soon As		
4	SVXII Rad Hard Chips Available	0 w	10/1/96	10/1/96		Start No Ear		
5	SVX II+Pick Off Packaging Proto.	54 w	10/1/96	10/30/97	4	As Soon As F		EEF115[0.2],EEU115[0.5]
6	Pickoff chip-third prototype	19 w	11/5/97	4/1/98		Start No Ear		EEF115[0.5],PhysF115[0.5]
7	M3-Fiber Trigger Pickoff Chips Ordered	0 w	7/1/97	7/1/97		As Soon As		
8	Pickoff Chip Production	16 w	11/19/98	3/26/99	6FS+6 w,7	Start No Ear	1.1.5.3.1.2(.28)	PhysU115,PhysF115[0.3],EEF115[0.5],k\$[0.15],k\$c[0.03]
9	Multichip Modules Ordered	0 w	10/20/97	10/20/97		Start No Ear		
10	Multichip Module Preproduction	77 w	11/26/97	6/24/99	8FF+4 w,9FS+4 w	Finish No Ea	1.1.5.3.1.1,1.1.5.3.1.2(.72),1.1.5	EEF115[0.5],k\$[8.48],k\$c[0.65]
11	Final Production - MCM	8 w	1/13/00	3/8/00	24	As Soon As F		ETF115,EEF115
12	Multichip Modules Received	0 w	3/8/00	3/8/00	11	As Soon As		
13								
14	FE Analog Boards	293.4 w	10/3/94	8/11/00		As Soon As		
15	Analog Board Prototype	34 w	11/1/95	7/2/96		Start No Ear		EEF115[0.5],ETF115[0.5],PhysF115[0.3]
16	Procure Parts - FY95	16 w	10/3/94	1/20/95	15	Start No Ear	1.1.5.3.2.2,1.1.5.3.2.3	k\$[0.2],k\$c[0.04]
17	Procure Parts - FY96	16 w	10/2/95	1/25/96	16	Start No Ear	1.1.5.3.1.8,1.1.5.3.1.11(.5),1.1.5	k\$[2.18],k\$c[0.09]
18	Analog Board Test with Cassette	35 w	4/13/98	12/23/98	17	As Soon As F		PhysU115,PhysF115[0.3]
19	M3-Fiber Tracker Analog Board Test Complete	0 w	12/23/98	12/23/98	18	As Soon As		
20	Preproduction Boards	40 w	4/1/99	1/26/00		As Soon As		
21	8-chip boards	32 w	4/1/99	11/15/99		Start No Ear		
22	12-chip boards	14 w	10/5/99	1/26/00	21FS-6 w	As Soon As		
23	Final Test	14 w	11/16/99	3/8/00		As Soon As		
24	8-chip test	6 w	11/16/99	1/12/00	21,10	As Soon As F		PhysU115[2],PhysF115[0.6],ETF115[0.5]
25	12-chip test	6 w	1/27/00	3/8/00	22	As Soon As		PhysU115[2],PhysF115[0.6],ETF115[0.5]
26	Redesign Boards	12 w	1/13/00	4/5/00		As Soon As		
27	8-chip board	4 w	1/13/00	2/9/00	24	As Soon As F		PhysU115[2],PhysF115[0.6],ETF115[0.5]
28	12-chip board	4 w	3/9/00	4/5/00	25	As Soon As		PhysU115[2],PhysF115[0.6],ETF115[0.5]
29	Bid 8-chip and 12-chip production	8 w	11/16/99	1/26/00	21	As Soon As F		
30	M3-Fiber Tracker Analog Boards Ordered	0 w	3/8/00	3/8/00	23,29	As Soon As	1.1.5.3.3.4,1.1.5.3.3.5(.78),1.1.5	k\$[1.06],k\$c[0.19]
31	Produce 10 boards	4 w	4/6/00	5/3/00	30,11,26	As Soon As		EEF115[2],ETF115[1.5]
32	10 Analog Boards Available	0 w	5/3/00	5/3/00	31	As Soon As		
33	Test 10 Boards	2 w	5/4/00	5/17/00	32	As Soon As		EEF115,ETF115
34	Produce and test remaining boards	12 w	5/18/00	8/11/00	33	As Soon As		EEF115[2],ETF115[1.5]
35	Analog Boards Ready	0 w	8/11/00	8/11/00	34	As Soon As		
36	Assemble Commission CTT System	13 w	8/14/00	11/13/00	35,64,76	Start No Ear		
37								
38	CFT Digital Boards	184.6 w	11/12/96	8/11/00		As Soon As		
39	Development	81 w	11/12/96	7/7/98		Start No Ear		EEU115
40	Test Board Prototype Fabrication	4 w	1/4/99	1/29/99		Start No Ear		EEF115[0.3],ETF115[0.5]
41	Test Board Prototype Complete	0 w	1/29/99	1/29/99	40	As Soon As		
42	Board Test	12 w	2/1/99	4/23/99	5,40	As Soon As F		PhysU115,PhysF115[0.3],EEF115,ETF115[0.5]
43	Final Design	28 w	4/1/99	10/18/99		As Soon As		
44	Design Motherboard	6 w	4/1/99	5/12/99		Start No Ear		EEF115,ETF115[0.5]
45	Design Level 1 Daughter Board	20 w	5/13/99	10/4/99	44	As Soon As F		EEF115,ETF115[0.5],PhysF115
46	Design Level 2 Daughter Board	22 w	5/13/99	10/18/99	44	As Soon As F		EEF115[2],ETF115[0.5]
47	Final Prototypes	26 w	5/13/99	11/15/99		As Soon As		
48	Mother Board Prototype	6 w	5/13/99	6/24/99	44	As Soon As F		EEF115,ETF115[0.5]
49	Level 1 Daughter Board Prototype	6 w	10/5/99	11/15/99	45	As Soon As F		EEF115,ETF115[0.5]
50	Level 2 Daughter Board Prototype	4 w	10/19/99	11/15/99	46	As Soon As		EEF115,ETF115[0.5]
51	Final Test	8 w	11/16/99	1/26/00		As Soon As		
52	Test Mother Board and Level 1 Daughter Board	6 w	11/16/99	1/12/00	48,49	As Soon As F		PhysU115,PhysF115[0.3],EEF115,ETF115[0.5]
53	Test Mother Board and Level 2 Daughter Board	8 w	11/16/99	1/26/00	50,48	As Soon As		PhysU115,PhysF115[0.3],EEF115,ETF115[0.5]
54	Redesign	6 w	1/13/00	2/23/00		As Soon As		
55	Motherboard Redesign	4 w	1/13/00	2/9/00	52	As Soon As F		PhysU115[0.5],PhysF115[0.1],EEF115[0.5],ETF115[0.25]
56	Level 1 Daughter Board Redesign	4 w	1/13/00	2/9/00	52	As Soon As F		PhysU115[0.5],PhysF115[0.1],EEF115[0.5],ETF115[0.25]
57	Level 2 Daughter Board Redesign	4 w	1/27/00	2/23/00	53	As Soon As		PhysU115[0.5],PhysF115[0.1],EEF115[0.5],ETF115[0.25]
58	Bid Mother and Daughter Boards	5 w	10/19/99	11/22/99	43	As Soon As F		
59	M3-CFT Digital Boards Ordered	0 w	11/22/99	11/22/99	58	As Soon As		
60	Produce 10 Boards	8 w	2/24/00	4/19/00	54,59	As Soon As	1.1.5.3.1.3,1.1.5.3.1.5-1.1.5.3.1.	EEF115,ETF115[0.5],k\$[1.98],k\$c[0.38]
61	10 Digital Boards Available	0 w	4/19/00	4/19/00	60	As Soon As		
62	Test Boards	4 w	4/20/00	5/17/00	61	As Soon As		
63	Final Production	12 w	5/18/00	8/11/00	62	As Soon As	1.1.5.3.6.3,1.1.5.3.6.5-1.1.5.3.6.	EEF115,ETF115[0.5],k\$[2.7],k\$c[0.49]
64	CFT Digital Boards Ready	0 w	8/11/00	8/11/00	63	As Soon As		
65								
66	Mixer Boards	60.8 w	4/1/99	6/21/00		As Soon As		
67	Test Board Design	19 w	4/1/99	8/13/99		Start No Ear		EEF115[0.5]
68	Test Board Prototype	9.8 w	8/16/99	10/22/99	67	As Soon As F		EEF115
69	Prepare Final Design	6 w	10/25/99	12/7/99	68	As Soon As F		EEF115
70	Mixer Board Design Finished	0 w	12/7/99	12/7/99	69	As Soon As		
71	Build Mixer Prototype	11 w	12/8/99	3/7/00	70	As Soon As F		EEF115,ETF115[0.2]

Fiber Tracker Electronics
All Tasks

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WB\$	Resource Names
72	Redesign Mixer Board	7 w	3/8/00	4/25/00	71	As Soon As F		EEF115
73	Bid Mixer Boards	6 w	10/25/99	12/7/99	68	As Soon As F		
74	Mixer Boards Ordered	0 w	4/25/00	4/25/00	73,72	As Soon As	1.1.5.3.8	k\$[1.27],k\$c[0.26]
75	Build Production Boards	8 w	4/26/00	6/21/00	72,74	As Soon As F		EEF115[0.5]
76	Mixer Boards Ready	0 w	6/21/00	6/21/00	75	As Soon As		
77								
78	Support Hardware	48.6 w	5/17/99	5/10/00		As Soon As		
79	Design FEA Backplane	4 w	5/17/99	6/14/99		Start No Earl		EEF115
80	Produce FEA Backplane	15 w	1/27/00	5/10/00	20	As Soon As F	1.1.5.3.1.11(.5),1.1.5.3.3.10(.5)	k\$[0.09],k\$c[0.02]
81	Design Motherboard Backplanes	4 w	9/1/99	9/29/99	43	As Soon As F		EEF115
82	Produce Motherboard Backplanes	15 w	9/30/99	1/28/00	81	As Soon As F	1.1.5.3.6.11(.67),1.1.5.3.7.10	k\$[0.11],k\$c[0.02]
83	Design Mixer Board Backplanes	4 w	12/8/99	1/18/00	69	As Soon As F		EEF115
84	Produce Mixer Board Backplanes	15 w	1/19/00	5/2/00	83	As Soon As F		
85								
86	Rack Prep in Movable Counting House	30 w	5/1/97	12/3/97		Start No Earl		EEF115[0.2],ETF115
87	Installation & System Test	6 w	8/14/00	9/25/00	34,63,75	As Soon As		EEF115[3],PhysU115[2],PhysF115,ETF115
88	First Crate Operational	0 w	5/17/00	5/17/00	33	As Soon As		
89	Commission fiber tracker	14 w	6/2/00	9/12/00	88	As Soon As F		