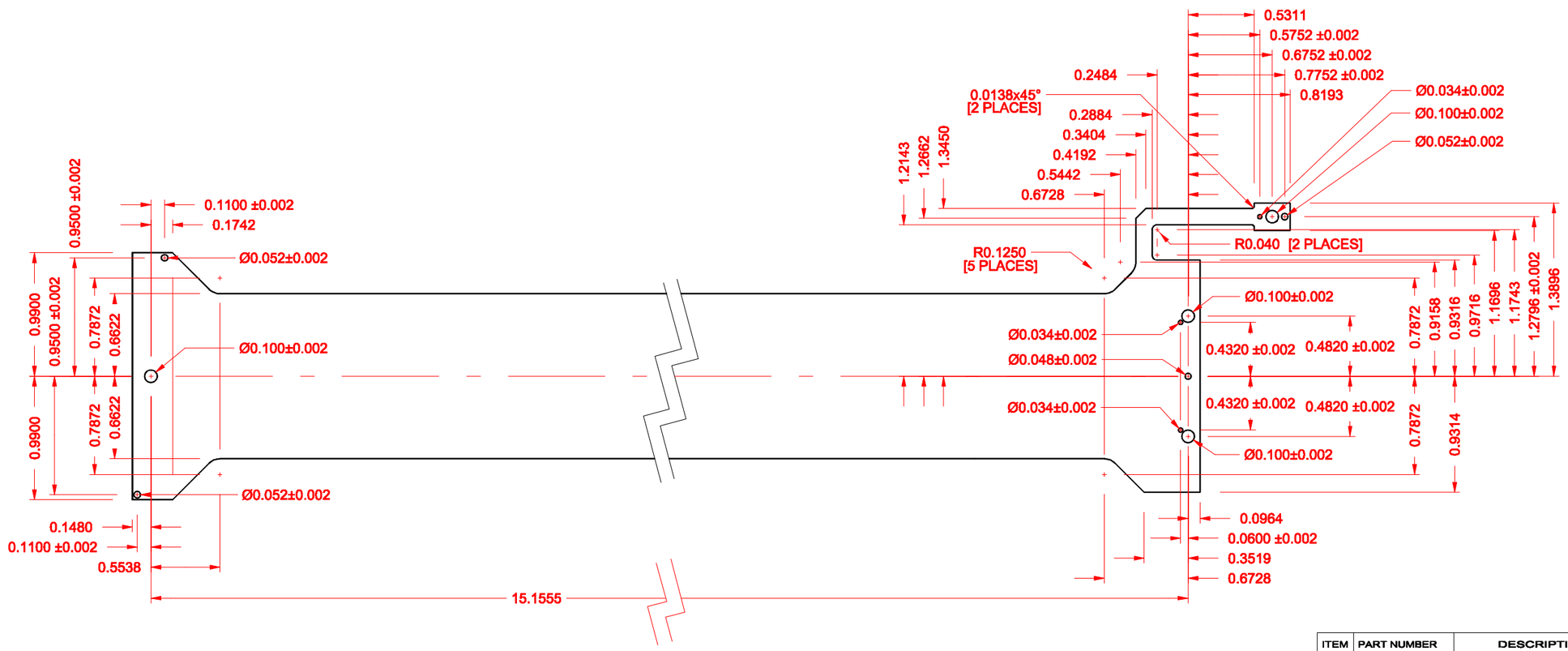
REV.	DESCRIPTION	DRAWN / APPD.	DATE / DATE
B.	REDUCED CIRCUIT WIDTH IN WARM INTERCEPT REGION, CREATED STAGGERED BIAS VIA ARRAY, INCREASED SIGNAL TRACE PITCH MID-CIRCUIT.	M. MATULIK	05/01/98
C.	RESTORED WARM INTERCEPT REGION WIDTH, INCREASED POWER TAIL WIDTH.	M. MATULIK	01/13/99
D.	INCREASED LENGTH BY 0.250 INCHES FOR BACKSIDE BIAS CONTACT POSITIONING	M. MATULIK	02/11/99
E.	REDUCED LENGTH BY 0.100, REDIMENSIONED DRAWING.	M. MATULIK	05/28/99



ITEM	PART NUMBER	DESCRIPTION OR SIZE	QTY

PARTS LIST

UNLESS OTHERWISE SPEC.				
RADII	DECIMALS	ORIGINATOR	M. Matulik	01/03/97
0.030	0.005	DRAWN BY	M. Matulik	01/03/97
DIMENSIONS IN INCHES.		CHECKED BY		
		APPROVED BY		
		USED ON -		
		MATERIAL -		

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

VLPC 64 Channel Readout Cable

Model J

Board Outline

SCALE	FILMED	DRAWING NUMBER	Sheet 1 of 4	REV.
		3823.113-MB-330202		E

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