

TFC Status

- TFC Design and layout
 - Layout of DSP + memory + power
COMPLETE
 - “Processing” Mode
 - Detailed block diagrams for programmable logic 80%
 - FPGA code 10% completed
 - “Internal Initialization” Mode
 - Starting detailed design
 - L2 Output format
 - evolved slightly (packing/precision)
 - looked at IOGen requirements, easy
 - Ordered first block of DSP's
 - 16 week lead time...

TFC status, con't

- **Soon we'll need to**
 - double check final STC data format
 - understand external initialization
 - double check L3 buffer access...
- **Fiber patch cables**
 - Initial lengths from FNAL, wrong
 - J. Foglesong sends corrections, but wants us (JDH?) to double check... which requires physical presence...
- **Trigsim, Wendy**