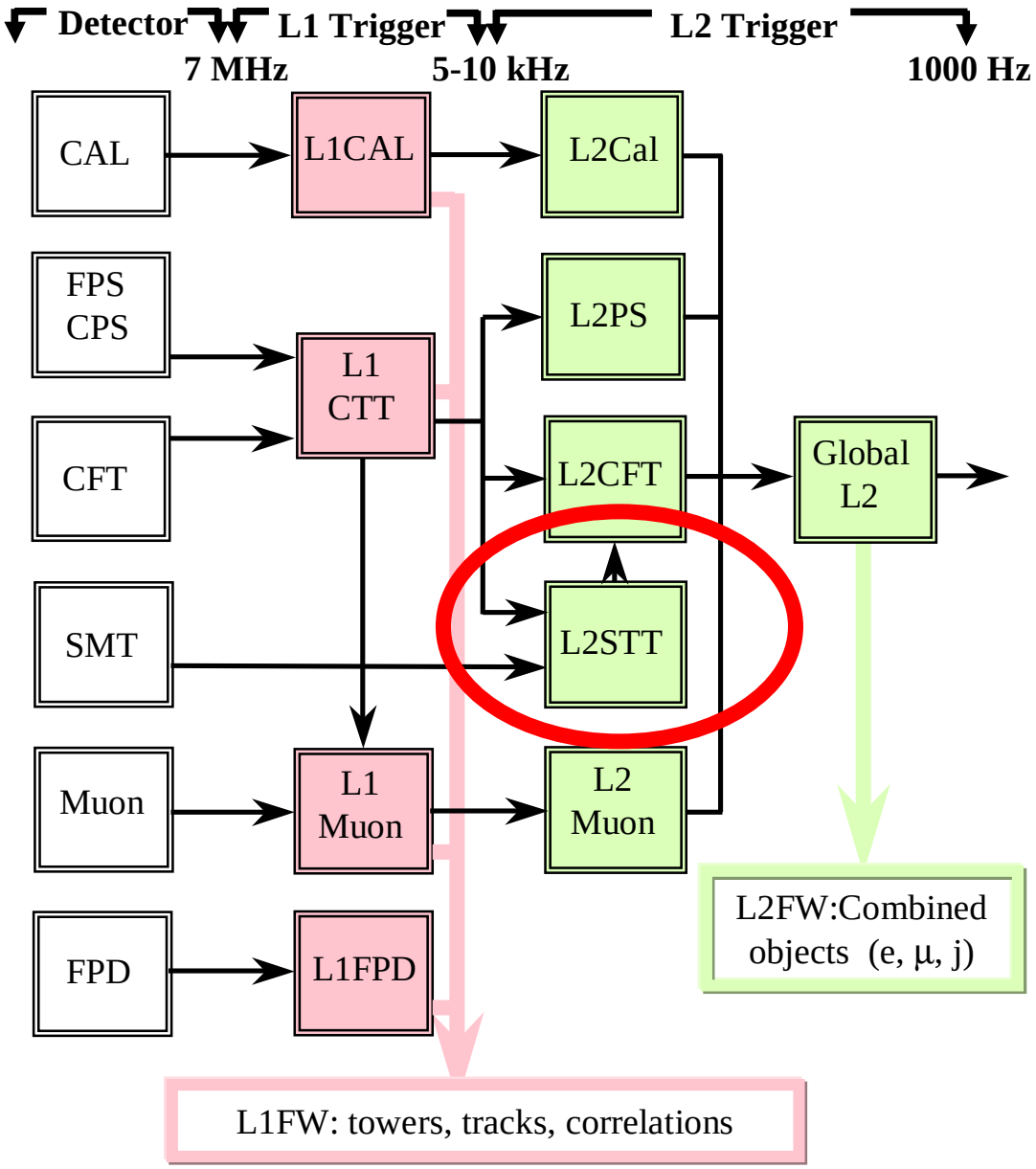
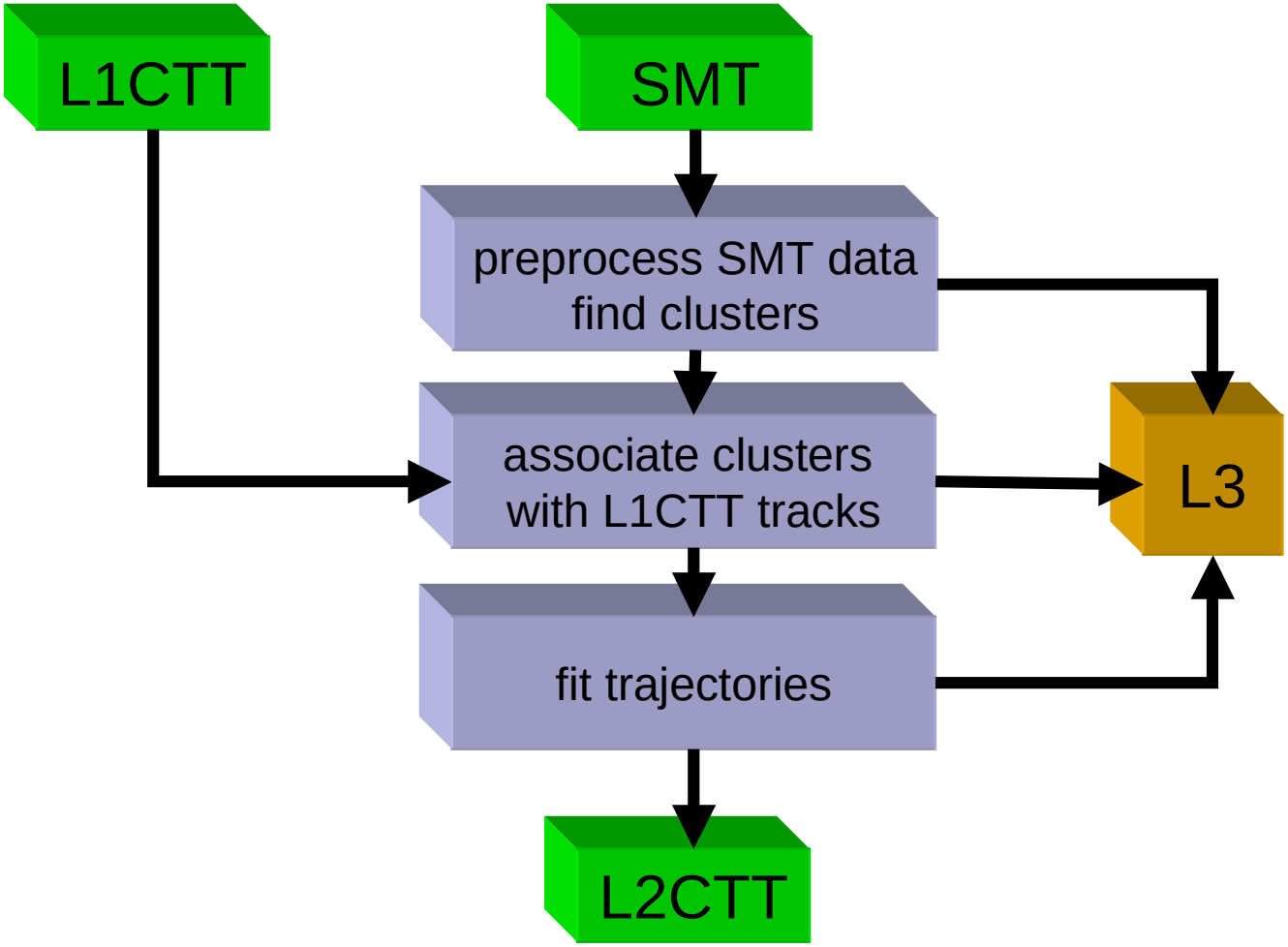
L2 Silicon Track Trigger

Ulrich Heintz
Boston University

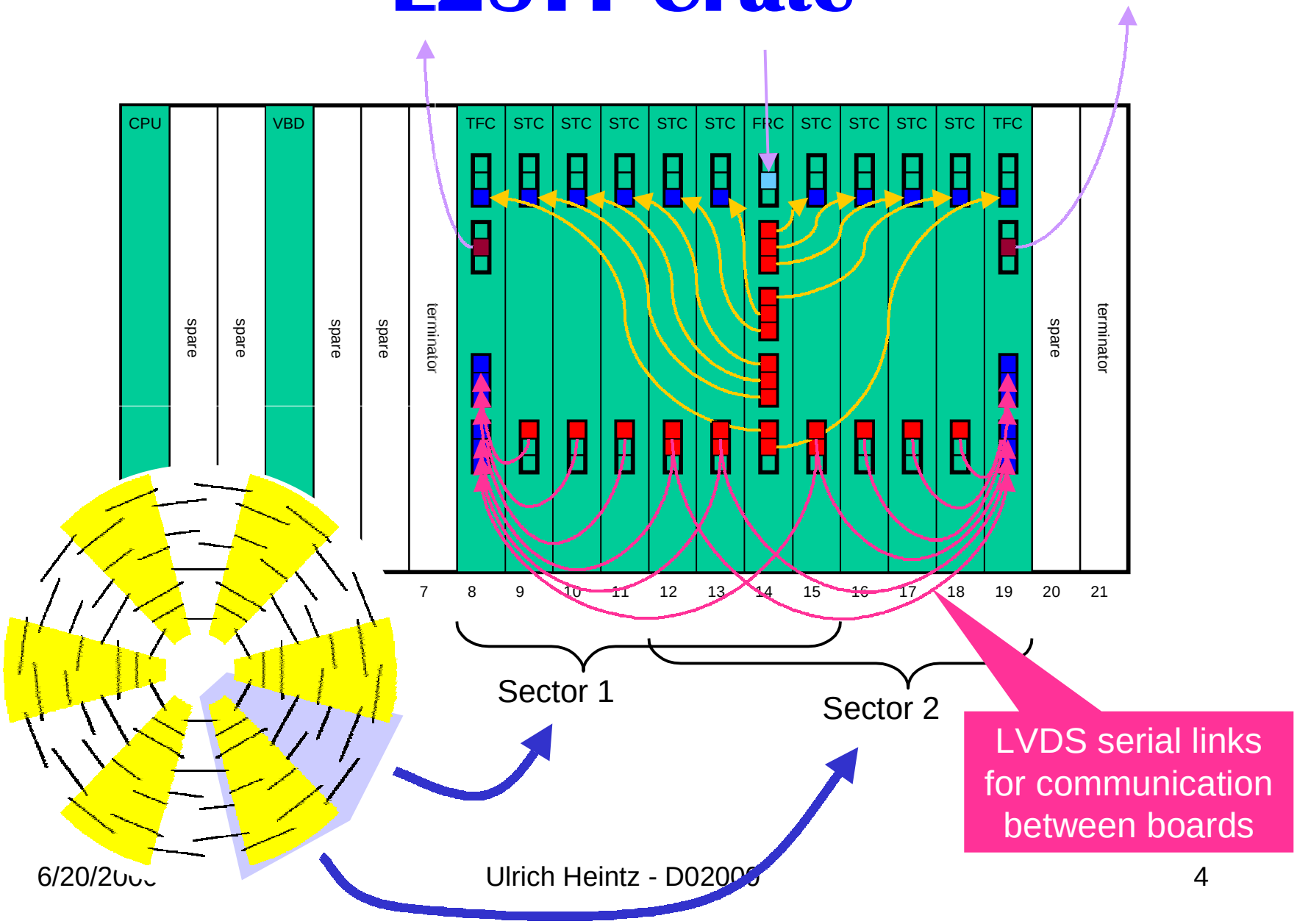
D0 Trigger System



L2STT


L1CTT
SMT
preprocess SMT data
find clusters
associate clusters
with L1CTT tracks
L3
fit trajectories
L2CTT

L2STT Crate

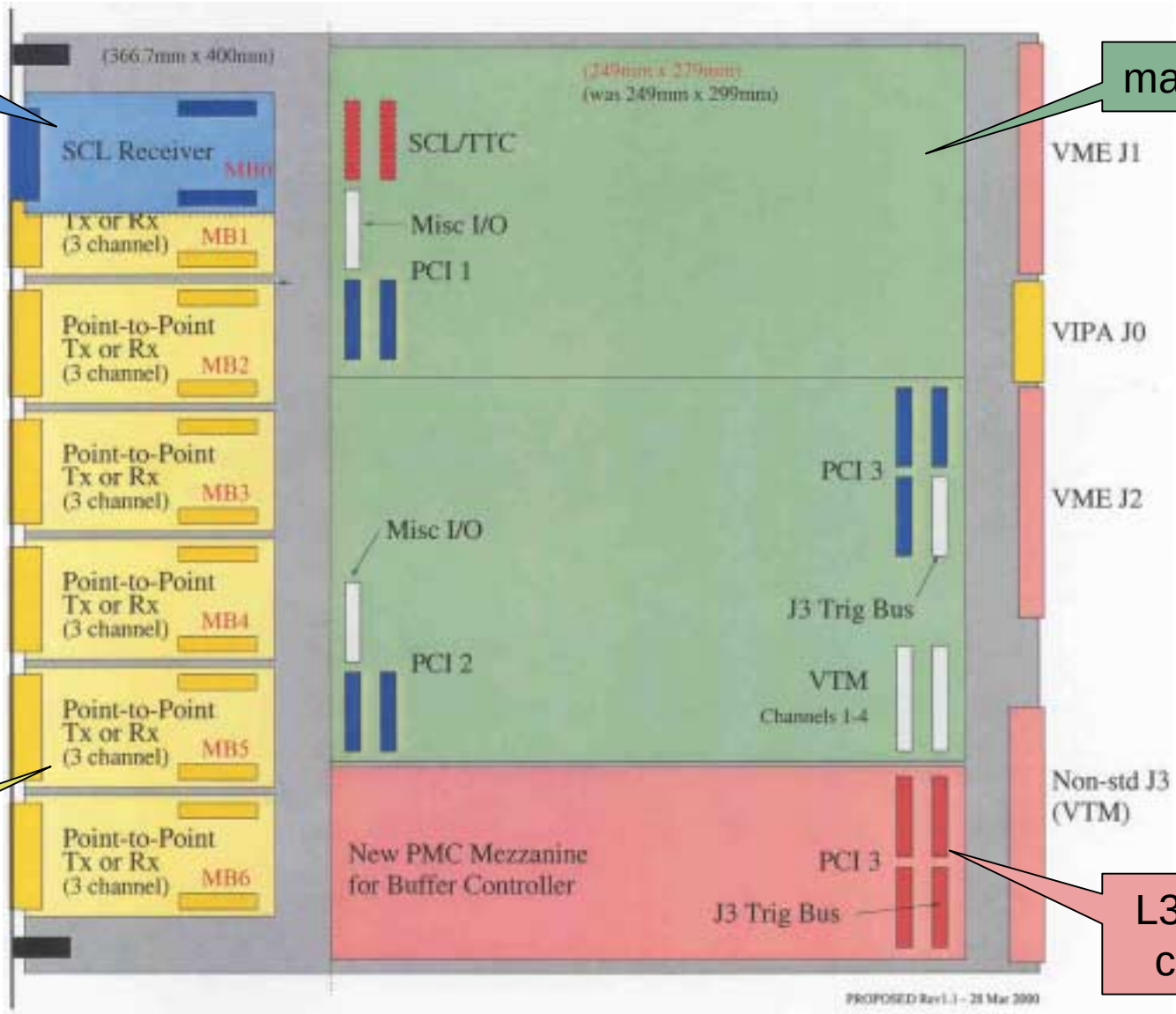

CPU
spare
spare
VBD
spare
spare
terminator
TFC
STC
STC
STC
STC
STC
FRC
STC
STC
STC
STC
TFC
spare
terminator
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
Sector 1
Sector 2
LVDS serial links for communication between boards

Motherboard

SCL receiver

PCI busses for onboard communication

link tx/rx



main logic

L3 buffer control

Card Flavors

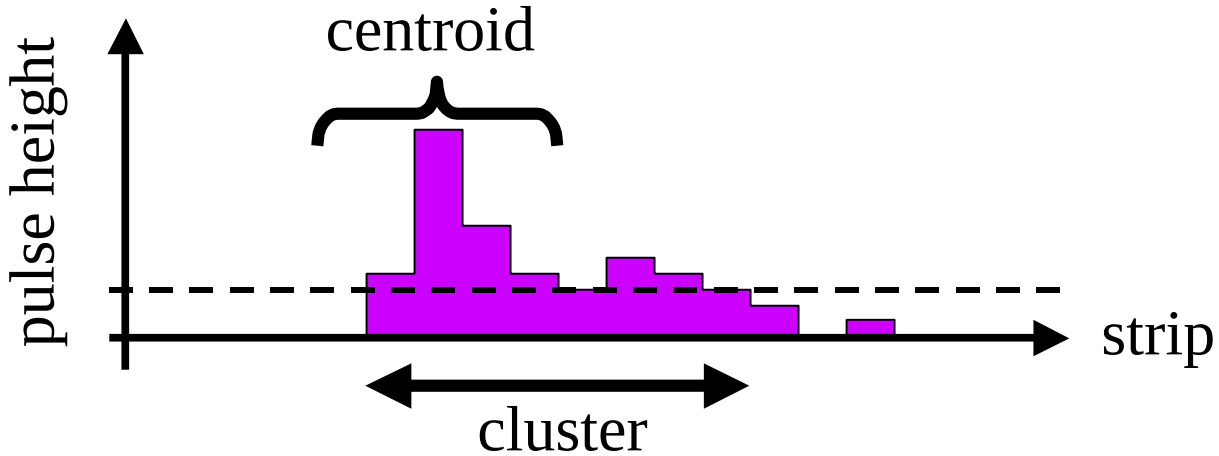
- fiber road card
  - receive SCL
  - fan out L1CTT data
  - manage L3 buffers
  - arbitrate VME bus
- silicon trigger card
  - preprocess SMT data
  - associate hits with CFT tracks
- track fit card
  - fit trajectory to hits
- CPU
  - initialization
  - downloading
  - monitoring
  - resets
- VBD

Status

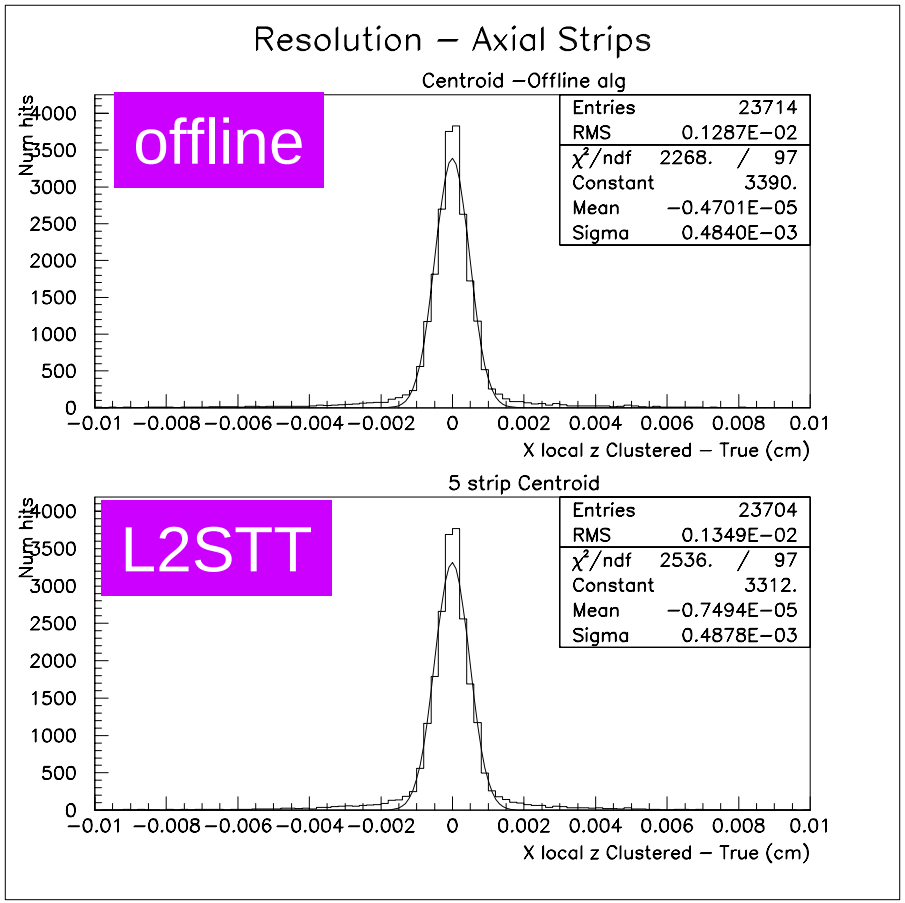
- Motherboard
  - design of schematic in progress
- Link tx/rx boards
  - 1st prototypes available – being tested
- Logic cards
  - prototype design under way
- CPU
  - hardware chosen

Processing of SMT Data

- bad strip mask
  - zero amplitude of flagged strips
- pedestal/gain calibration
  - chip-by-chip lookup table
- clustering algorithm
  - similar to offline, use 5 strips for centroid



Processing of SMT Data



Track Fit Algorithm

- require hits in
  - at least 3 of the 4 SMT layers
  - same 30 degree sector
  - at most 2 adjacent barrels
- choose hits
  - closest to trajectory defined by CFT and beam
- linearized χ^2 fit

Output

- to L2CTT
  - all data from L1CTT
  - for each track

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
p_T							±	S								ϕ								χ^2					x	x	f
b												x	dE/dx			track						x	x	f	f	f	f	barrel			f

p_T	transverse momentum encoded in 0.25(3) GeV increments for p_T <(>) 25 GeV:	b	impact parameter
		dE/dx	ionization
±	sign	track	track number (0-45)
S	impact parameter significance	barrel	barrel number
ϕ	azimuth	f	topology flags
χ^2	goodness of fit	x	spares

Output

- to L3 for each event
  - all information sent to L2CTT
  - for all SMT clusters

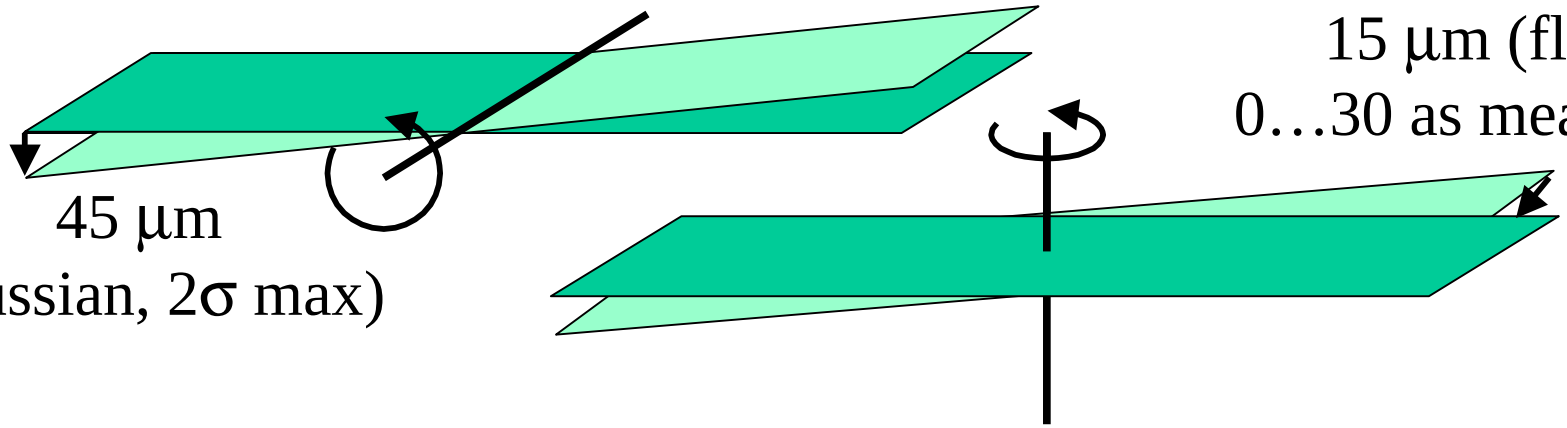
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	chan			typ		$\frac{dE}{dx}$		sequencer								HDI			chip				centroid								

  - for all SMT clusters associated with a track

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
track						$\frac{dE}{dx}$		sequencer								HDI			chip				centroid								

Performance

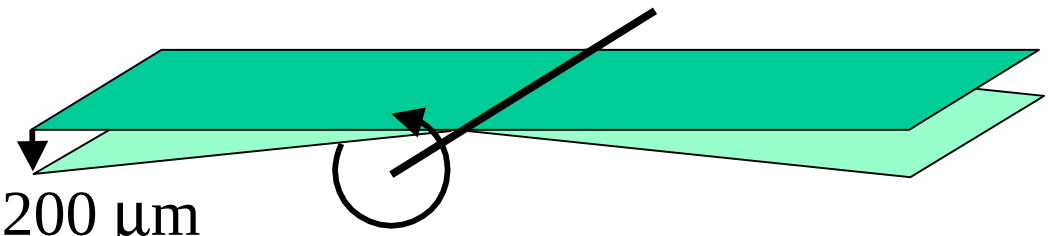
- "Nominal" assembly tolerances



45 μm
(gaussian, 2σ max)

15 μm (flat)
0…30 as measured

- "Tent" distortions (barrels 1,6 layers 1,3)



0…200 μm
as measured
(Y. Gershtein)

Performance

- generate helical tracks
- intersect with
  - ideal detector geometry
  - nominal assembly tolerance
  - nominal + tent distortions
- reconstruct with ideal detector geometry
- impact parameter resolution includes
  - multiple scattering (50 μm GeV/p_T)
  - beam spot size (30 μm)

Performance

p_T (GeV)	geometry	background pass rate	relative rate	impact par cut (2σ)	relative b efficiency	relative bb eff
		f	$\propto f^3$		ε	$2\varepsilon^3-(\varepsilon^3)^2$
∞	ideal	4.5%	1	68 μm	1.00	1.00
	nominal	10%	11	86 μm	0.95	0.90
	tent	14%	30	100 μm	0.95	0.88
3.0	ideal	4.5%	1	76 μm	1.00	1.00
	nominal	9%	8	94 μm	0.94	0.88
	tent	12%	19	110 μm	0.94	0.88
1.5	ideal	4.5%	1	96 μm	1.00	1.00
	nominal	7.5%	4.6	108 μm	0.96	0.91
	tent	10%	11	120 μm	0.96	0.91

assume: luminous region =22 cm, three tracks with S>2,
impact parameter of b-tracks =250 μm

Schedule

• 1st prototype	100-170 days	→ Oct 2000
• 2nd prototype	80-100 days	→ Mar 2001
• System test	60 days	→ May 2001
• Production	100-120 days	→ Nov 2001
• Commissioning	60 days	→ Feb 2002

Credits/References

- L2STT Group
  - Boston: W.Earle, S.Fatakia, E.Hazen, U.Heintz, M.Narain
  - Columbia: H.Evans, A.Qi, W.Sippach, G.Steinbrück
  - Florida: B.Connolly, W.Lee, S.Linn, S.Lolage, R.Perry, H.Prosper, S.Tentindo-Repond, S.Roper, H.Wahl
  - Stony Brook: J.Hobbs, C.Pancake, W.Taylor
- Documentation
  - http://www-d0.fnal.gov/~wahl/vtxt.html