



DØ Silicon Trackers

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Fermilab



Run II Silicon Design and Status

- Is there a Run IIb?
- Run II plan
- Comparison of Run IIa and IIb designs
- Run IIa design and performance
 - ◆ *Geometry, mechanical support, and alignment*
 - ◆ *Sensors*
 - ◆ *Readout*
 - ◆ *Cooling*
- Run IIb designs
 - ◆ *Geometry, mechanical support, and alignment*
 - ◆ *Sensors*
 - ◆ *Readout*
 - ◆ *Cooling*
- **Summary**



Is there a Run IIb?

- Run IIa silicon was commissioned during the spring of 2001.
 - ◆ Designed for an integrated luminosity of 2 fb^{-1}
 - ◆ Capability estimated by Ron Lipton to be 3.5 to 4 fb^{-1} , but with large uncertainties
 - ◆ Useful life is expected to be limited by radiation damage, a steadily increasing number of dead devices, “grassy noise” (possibly from micro-discharges), and loss of b-tagging efficiency.
- Run IIb silicon was designed as an improved, drop-in replacement for Run IIa silicon
 - ◆ Designed for an integrated luminosity of 15 fb^{-1}
 - ◆ Capability estimated from irradiation studies to be 30 fb^{-1}
 - ◆ Number of barrel layers increased from 4 to 6
 - ◆ Disks eliminated



Is there a Run IIb? (2)

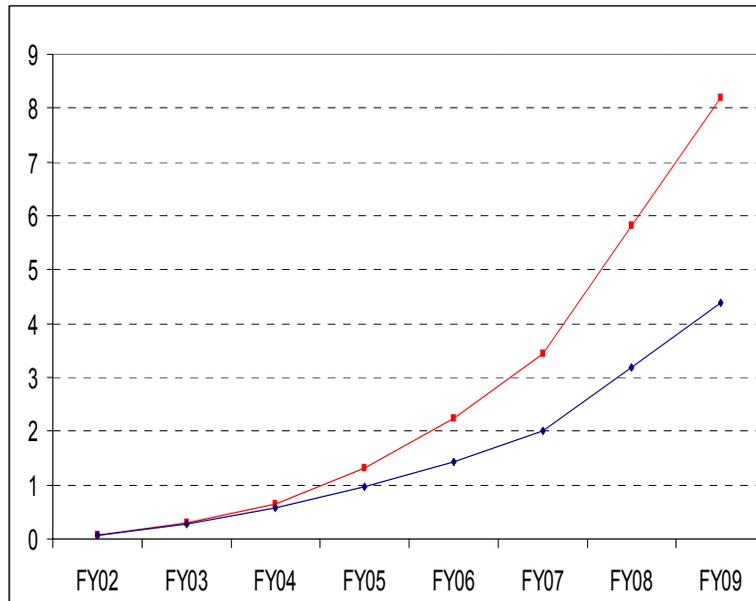
- The Director of Fermilab, Mike Witherell, announced on 3 Sep 2003 that “we will not include the silicon detectors in the continuing upgrade projects”.
- A six page note from the Director describes the decision.
http://www.fnal.gov/pub/now/Upgrade_Decision/Detector_upgrade_decision.pdf
- “The laboratory's goal is to achieve the greatest sensitivity possible to discoveries of new physics, and to do so as quickly as possible. To achieve this goal will require delivering the most integrated luminosity throughout Run II while keeping the detectors operating as efficiently as possible for the most important physics.”
- “The silicon detector teams in each collaboration have planned the upgrade project well and have made excellent progress. They deserve great credit for their rapid progress to date. The fast start on these projects demonstrates once again the excellence of the SiDet facility and the people who work there. In addition, the progress on developing the new readout chip, the SVX4, has been impressive. The present reconsideration of the silicon detector upgrade plan is motivated by the above considerations and not at all by any difficulties in the project execution.”
- Trigger and data acquisition upgrades will continue.



Run II Plan

Integrated luminosity plan submitted by Fermilab to DOE prior to the Aspen meeting

The design program is in red; the base program is in blue.



An integrated luminosity goal of 0.225 fb^{-1} to be delivered in 2003 was met on 22 August.

A careful study has been made of factors in the Tevatron which may limit luminosity. Beams Division personnel, outside experts, and personnel from other divisions participated in the study. Significant factors include:

1. Creep in the Tevatron magnet support system, which has led to a gradual drop of coil positions with respect to magnet iron and the generation of skew quadrupole components in the fields of magnets.
2. A gradual roll of magnets from tunnel floor motion. At some locations, this is associated with the removal of the original main ring magnets.
3. Magnet elevation changes due to ground motion.
4. Imperfect knowledge of Tevatron survey monument locations.

A ten week Tevatron shutdown was scheduled to address these.



Accelerator Shutdown

- The last store before accelerator shutdown was ended normally at 16:00 on 7 September 2003.
- Work will include:
 - ◆ The addition of shims between coil positioning cartridges and collared coils of dipole magnets.
 - ◆ The replacement of some magnet support stands.
 - ◆ The adjustment of magnet supports so that dipoles are level.
 - ◆ The addition of a survey and alignment system which ties monuments throughout the accelerator complex.
 - ◆ Tevatron surveys.
 - ◆ The installation of alignment monitoring equipment.

Date Created: Sunday, September 7, 2003 3:53:07 PM CDT
 Date Saved: Sunday, September 7, 2003 3:57:20 PM CDT
 Category - Topic - sequence number: SMT/Log - SMT_Log - 240122
 Operator(s): Ronald Sidwell
 Keyword(s): :SHIFT-SUMMARY:SMT:

SMT Shift Summary

Shift: DAY
 Time/Date: Sep 7, 2003,3:53:09 PM
 Shifter: sidwell
 Beam Status: colliding
 Run Status: global
 Non powered HDIs (look in title bar of IDVDD GUI): B: 63 F:

RUNS taken:

| Run Number | Run Type | Num Events | SMT Quality | Comments |
|------------|--------------|------------|-------------|----------|
| 180951 | PDAQ/PHYSICS | 597000 | GOOD | |
| 180952 | PDAQ/PHYSICS | 149000 | GOOD | |
| 180953 | PDAQ/PHYSICS | 12000 | GOOD | |
| 180954 | PDAQ/PHYSICS | 21000 | GOOD | |
| 180956 | PDAQ/PHYSICS | 426000 | GOOD | |

People you had to page (p.180):

| When | Who | Reason - Comments |
|------------------------|-----|-------------------|
| Sep 7, 2003,3:53:09 PM | | |

= no

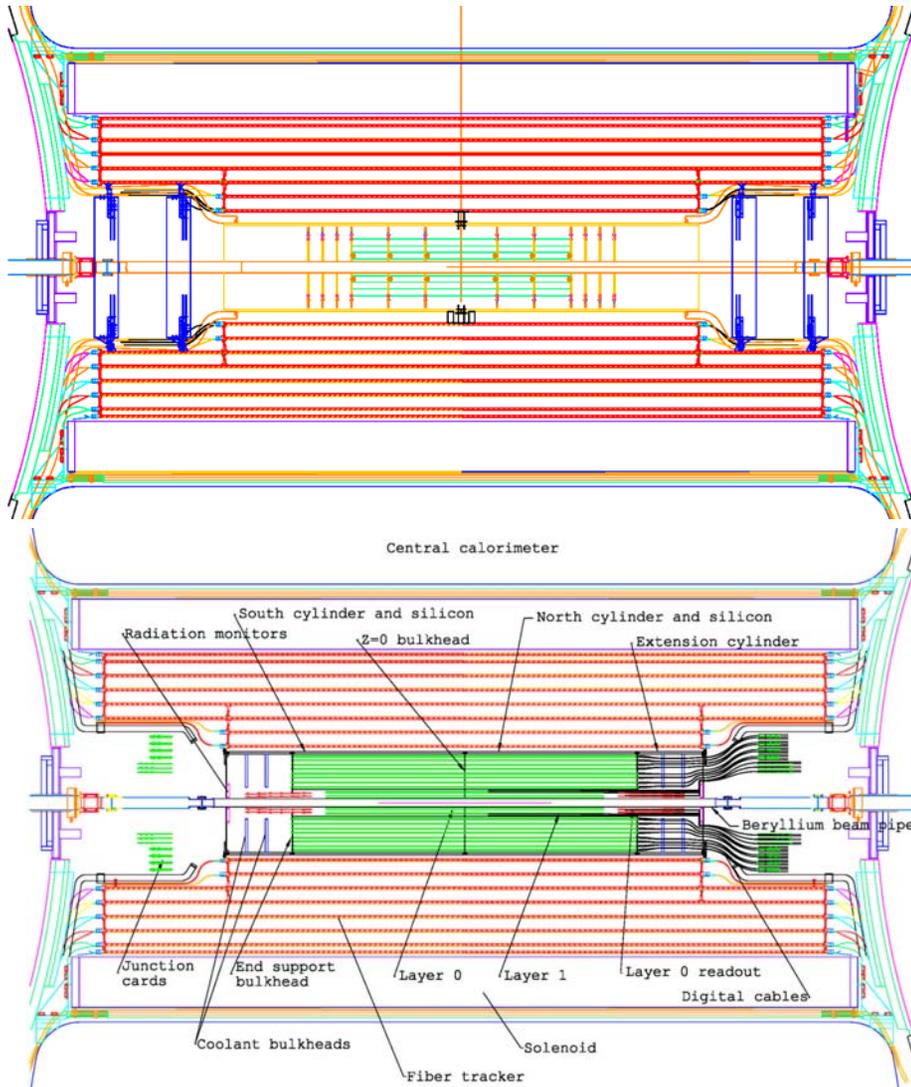
Archivers backed up (For Friday Day Shift Only) (p.162)

Comments:

uneventful, beam all shift. Just turned off for the shutdown



Plan View

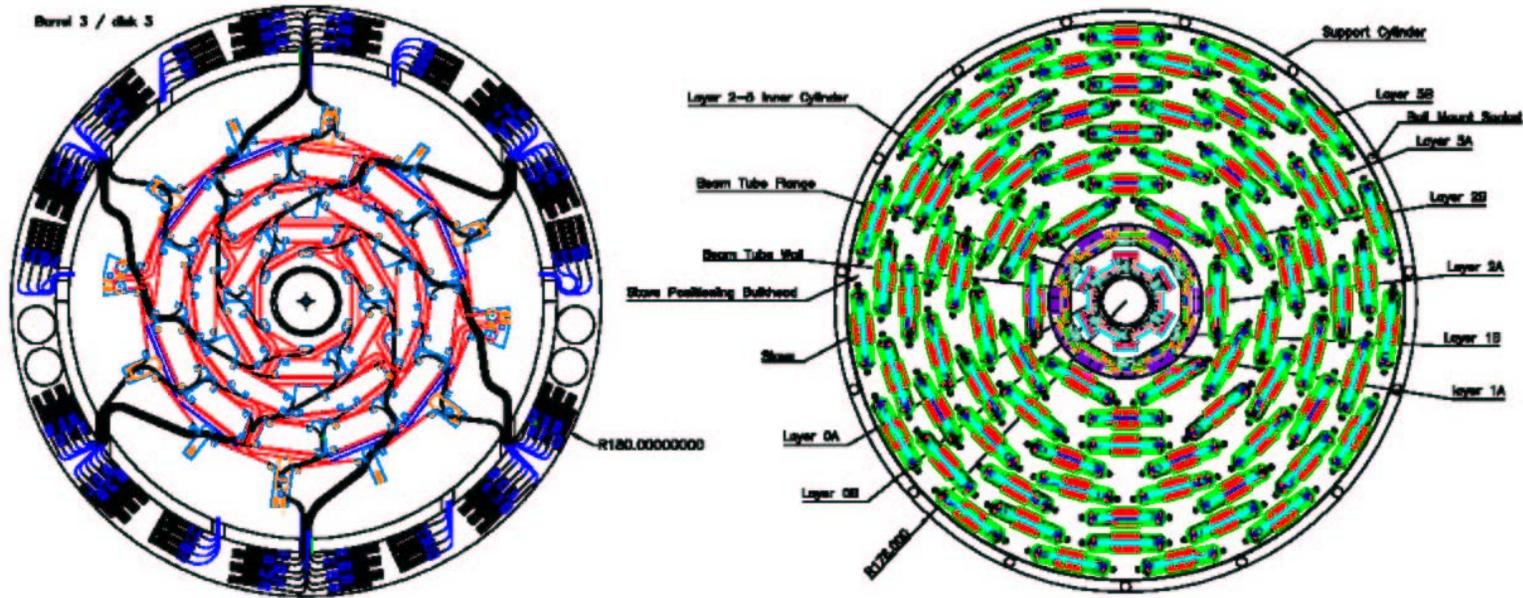


- Run IIa:
- 18.542 mm IR beam tube
- Six barrels, twelve F-disks, four H-disks
- 1070 mm long barrel plus F-disk region
- 4.8 m² silicon (4.3 m² active)

- Run IIb:
- 14.224 mm IR beam tube
- 12 sensors long (all layers)
- L0 - L1: 8 cm sensors
- L2 - L5: 10 cm sensors
- 1220 mm long barrel region
- Support from "bulkheads" at z = 0 and z = ±610 mm
- 8.6 m² silicon (8.0 m² active)



Silicon End View (Barrels)



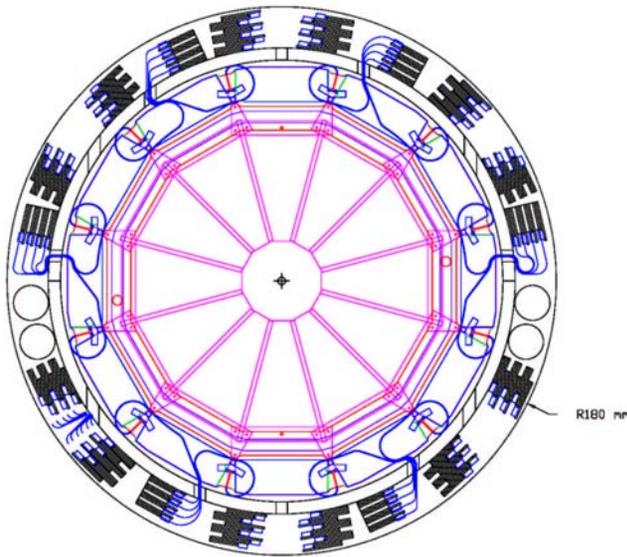
- Run IIa barrels:
- 2.6 m² silicon (2.4 m² active)
- 4 layers
- 864 sensors
- Double-sided except for layers 1 and 3 of the outermost barrels

- Run IIb barrels:
- 8.6 m² silicon (8.0 m² active)
- 6 layers
- 2304 single-sided sensors
- Stereo and axial sensors in layers 2-5, axial only in layers 0-1

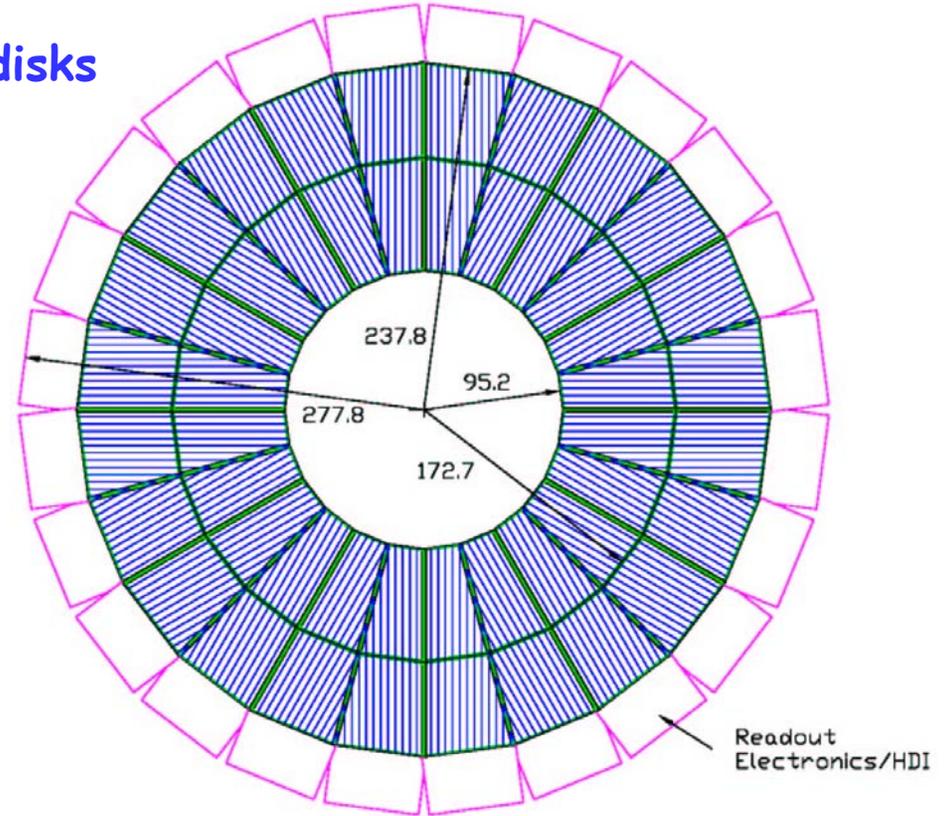


Run IIa Disks

F-disks



H-disks



- 0.9 m² silicon (0.7 m² active)
- 12 disks
- 144 sensors
- Double-sided

- 1.3 m² silicon (1.2 m² active)
- 4 disks
- 384 sensors
- Single-sided, mated back-to-back to form double-sided

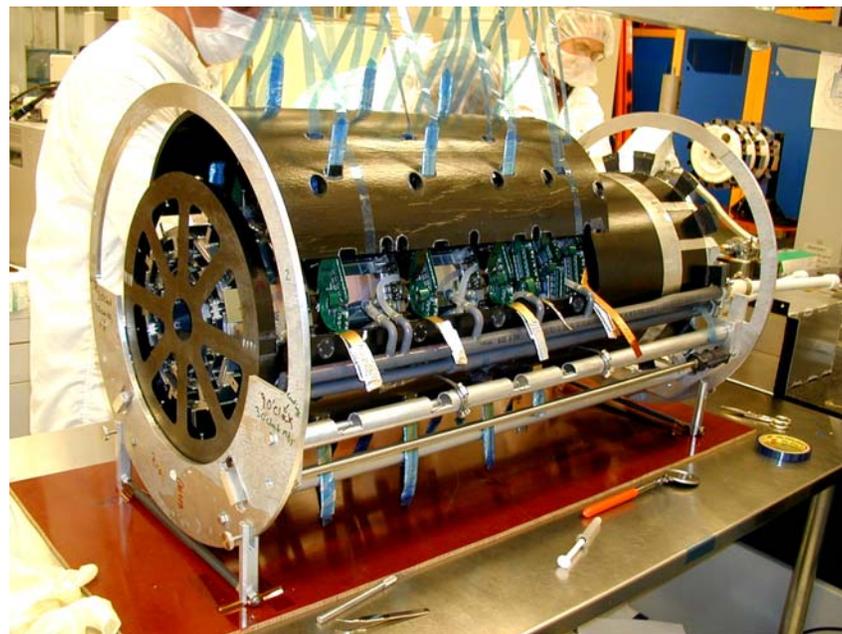


Run IIa Silicon



Silicon modules installed in the first of two support cylinders

Nominally identical north and south silicon



Installation of the support cylinder cover

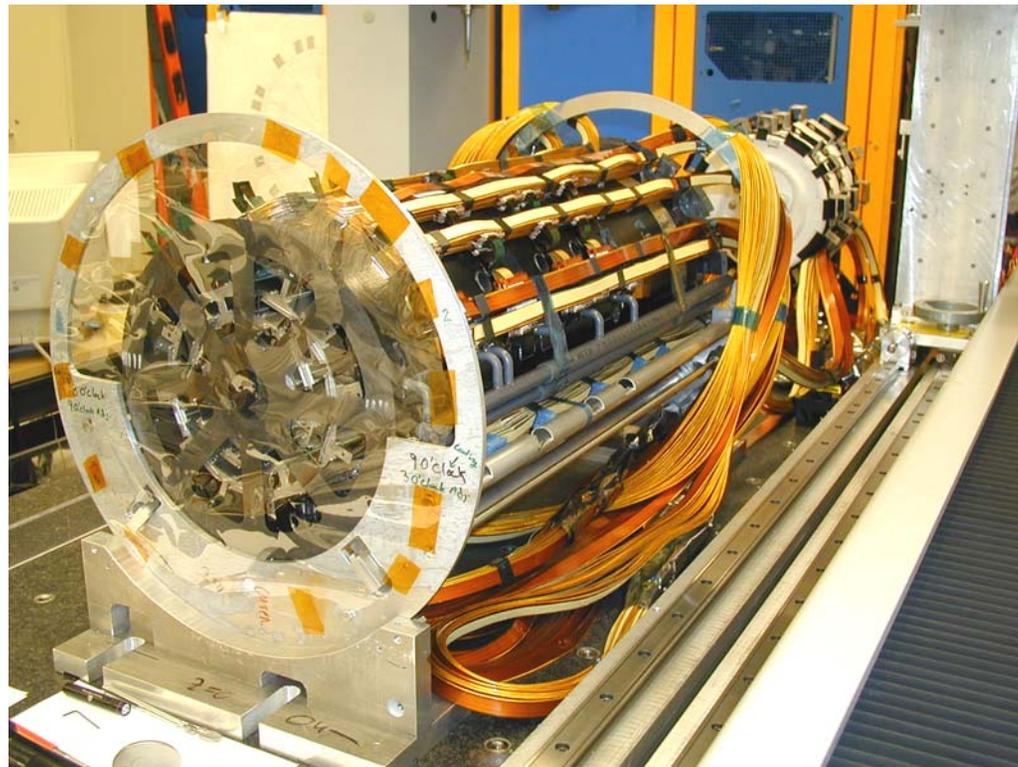
Many more fabrication and assembly photos and details were shown in Eric Kajfasz's presentation at Vertex 2002.



Run IIa Silicon



After adding the initial few low-mass cables



Silicon cabled and ready for shipment

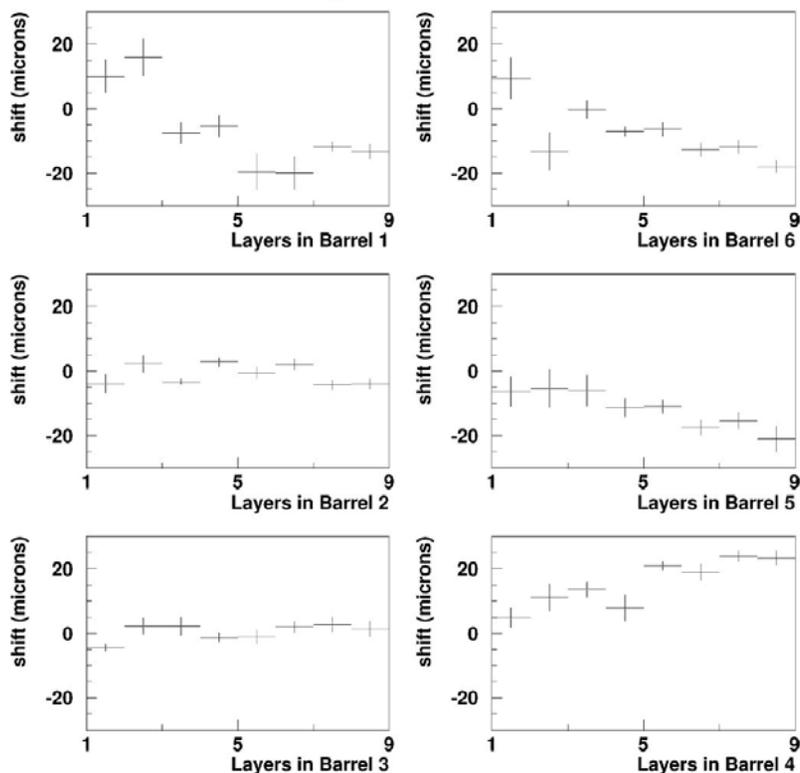


Shifts in Run IIa Ladder Alignment Based upon Tracking

- Difference between reconstructed location and expected location

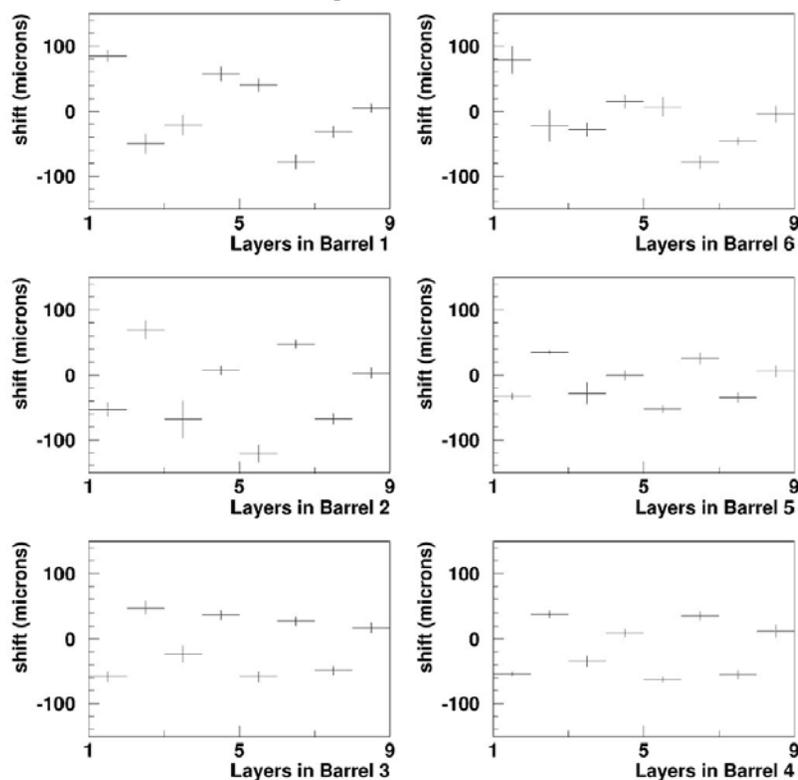
2002/05/15 19.14

Average Parallel Shift of Ladders



2002/05/15 19.14

Average Radial Shift of Ladders



Transverse position

Radial position

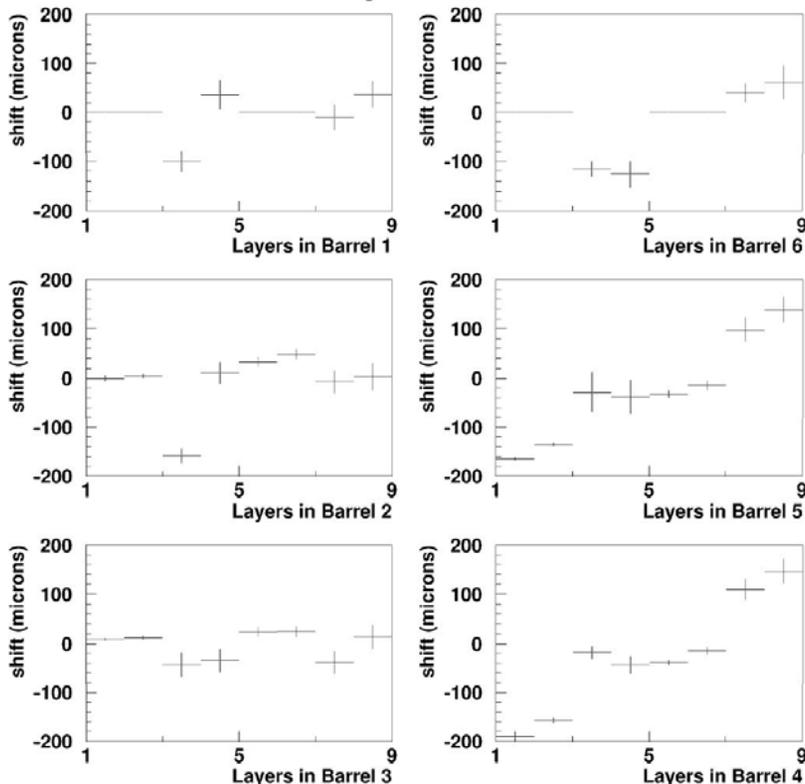


Shifts in Run IIa Ladder Alignment and Impact Parameter Resolution

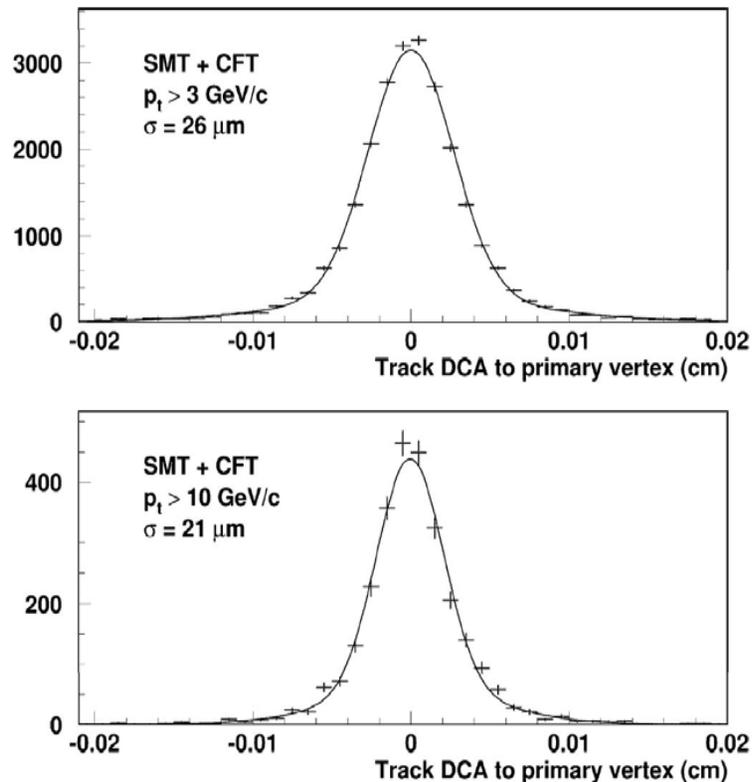
- Difference between reconstructed location and expected location
- Impact parameter resolution

2002/05/15 19.14

Average Z Shift of Ladders



Longitudinal position



Plots courtesy of
Guennadi Borissov



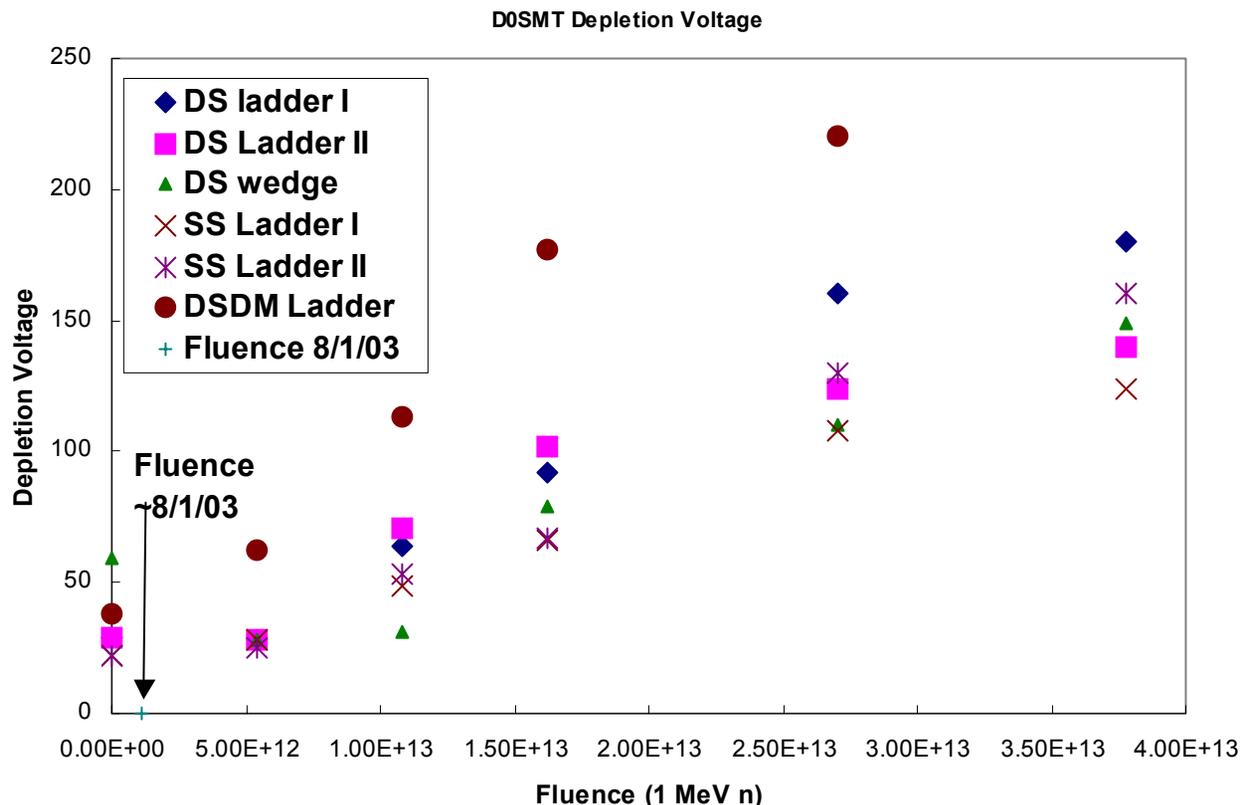
Run IIa sensors

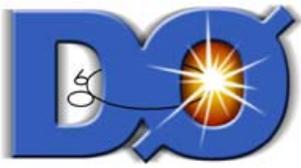
- Barrel sensors were provided by Micron
 - ◆ 144 9-chip, double-sided, 2 degree stereo sensors per barrel, 50 μm pitch on axial surface, 62.5 μm pitch on stereo surface
 - ◆ 144 6-chip, double-sided, 90 degree stereo sensors in the central four barrels, 50 μm pitch on axial surface, 153.5 μm pitch on stereo surface
 - ◆ 144 3-chip, single-sided sensors in outermost barrels, 50 μm pitch
 - ◆ Two 60 mm long sensors, end-to-end, per ladder
- F-disk sensors were provided by Micron and Eurisys.
 - ◆ Twelve sensors per F-disk
 - ◆ Double-sided, 30 degree stereo, 50 μm pitch on p-side, 62.5 μm pitch on n-side
- H-disk sensors were provided by ELMA.
 - ◆ Single-sided, mated back to back to provide 15 degree stereo
 - ◆ Two back to back sensor pairs per wedge, one pair at smaller radius and the second at larger radius
 - ◆ The two sensors of a given wedge surface are wire bonded and share a common readout
 - ◆ 24 wedges per H-disk
 - ◆ 4 sensors per wedge, 80 μm pitch with intermediate strips



Run IIa Depletion Voltages

- As of 1 August 2003, we had accumulated $\sim 280 \text{ pb}^{-1}$. That corresponds to an effective fluence between 9 (DO flux measurement) and 12 (CDF run2a parameterization) $\times 10^{11} \text{ 1 MeV n/cm}^2$. Changes in depletion voltage are small ($\sim 10 - 20 \text{ volts}$).

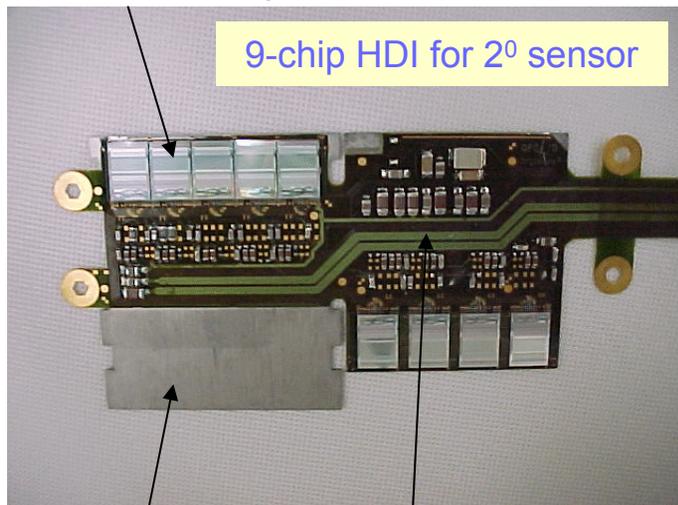




Run IIa HDI's and Ladders

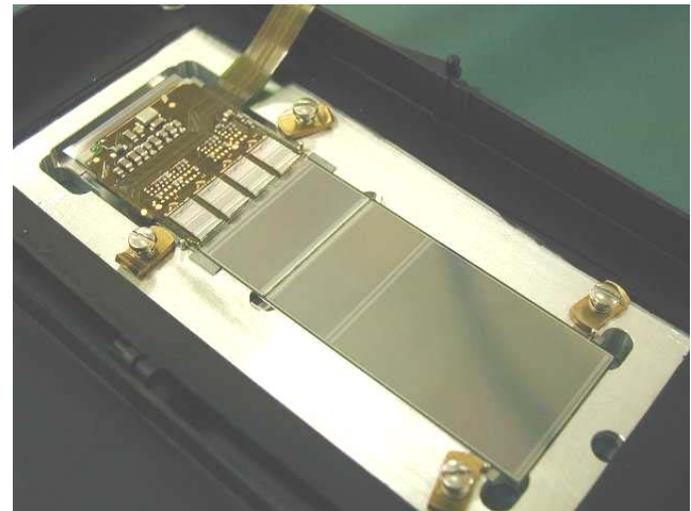
- SVX chips are mounted on and connected by kapton and copper flex circuits with 0.2 mm pitch.
- Flex circuits are laminated to beryllium substrates which are glued to the silicon sensors.
- Connections are made via aluminum wedge bonding.
- The flex circuit "pigtail" connects to a low-mass cable via a Hirose connector.
- The low mass cables carry signals out of the interaction region.

SVXIIIE chips



Be substrate

Bus control and power traces



n-side of 2° stereo ladder

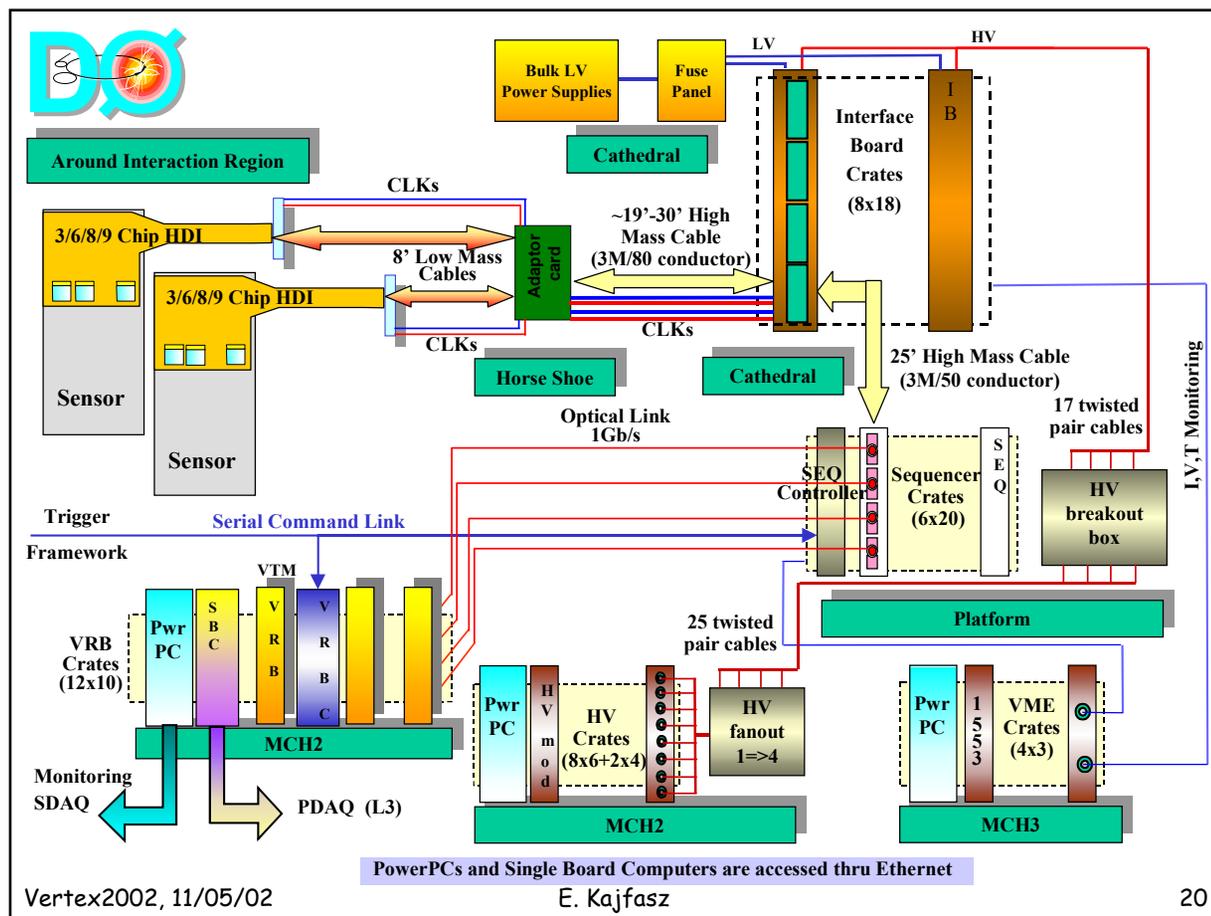


Run IIa Readout

Most recurring types of readout problems have been in the collision hall, to which access is limited.

Except for the adapter card end of low-mass cables, the portion of the readout from the HDI's to the adapter cards is inaccessible without silicon removal.

No access has been made to the silicon itself.



Vertex2002, 11/05/02

PowerPCs and Single Board Computers are accessed thru Ethernet

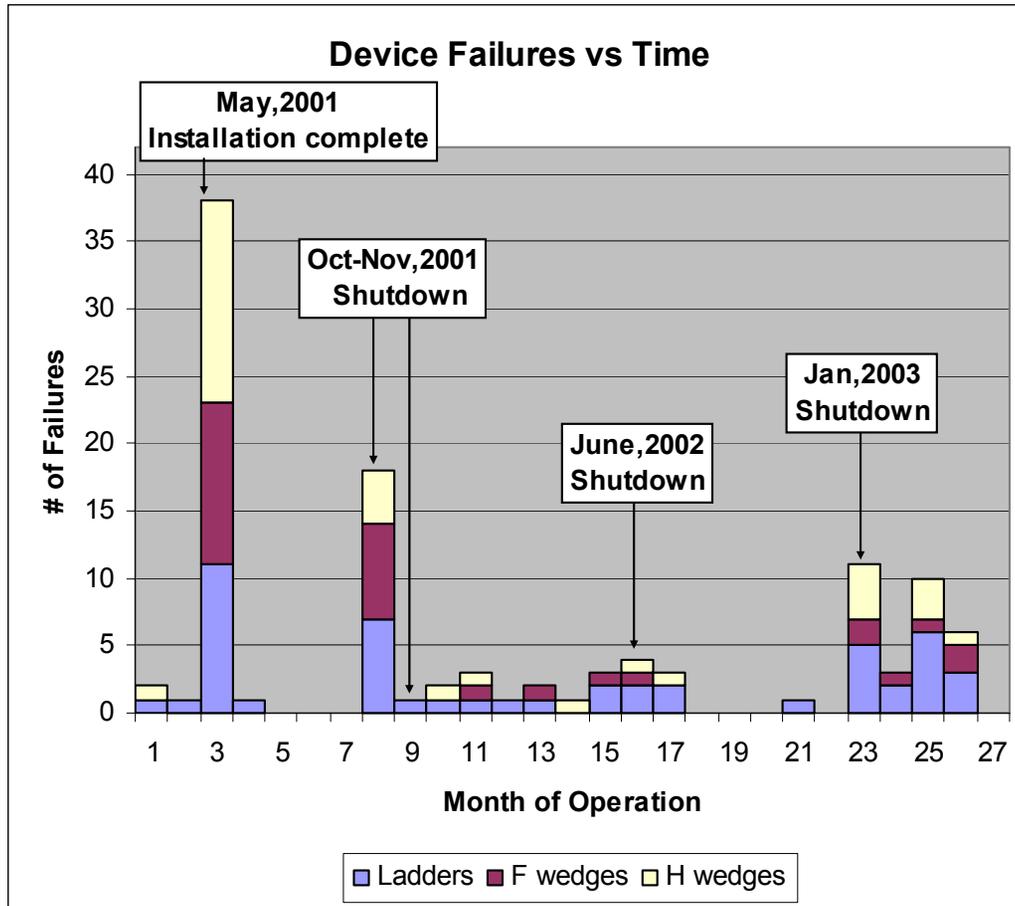
E. Kajfasz

20



Disabled Devices

- "SMT Longevity", Eric Kajfasz and Breese Quinn, 29 May 2003



Total of 912 devices.

Devices which malfunctioned and were recovered are not included.

The majority of devices were disabled after detailed diagnostics during major service periods.

Typically, they had failed earlier.

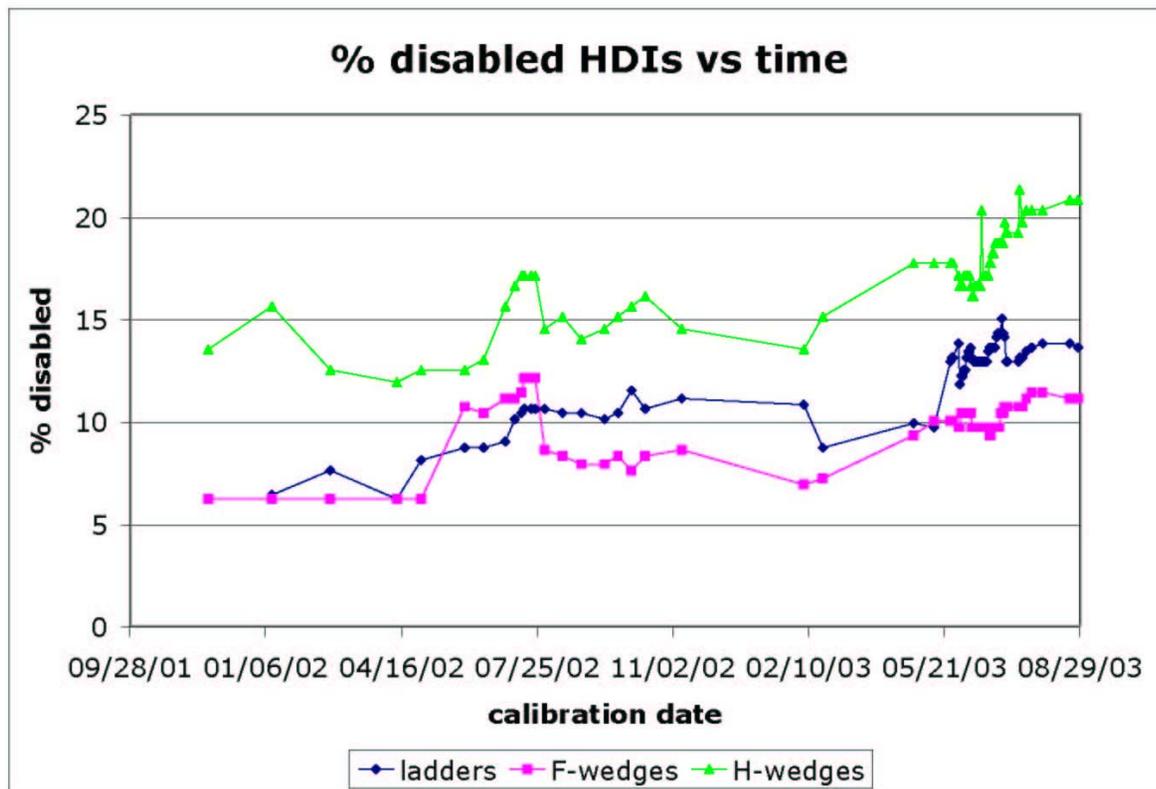


Disabled HDI's versus Time

Standard repairs:

Clock cables and their terminations, replacement of sequencers, re-cabling interface boards to use good channels

The emphasis since early this year has been on minimizing interruptions to data acquisition.



Provided by Michael Weber



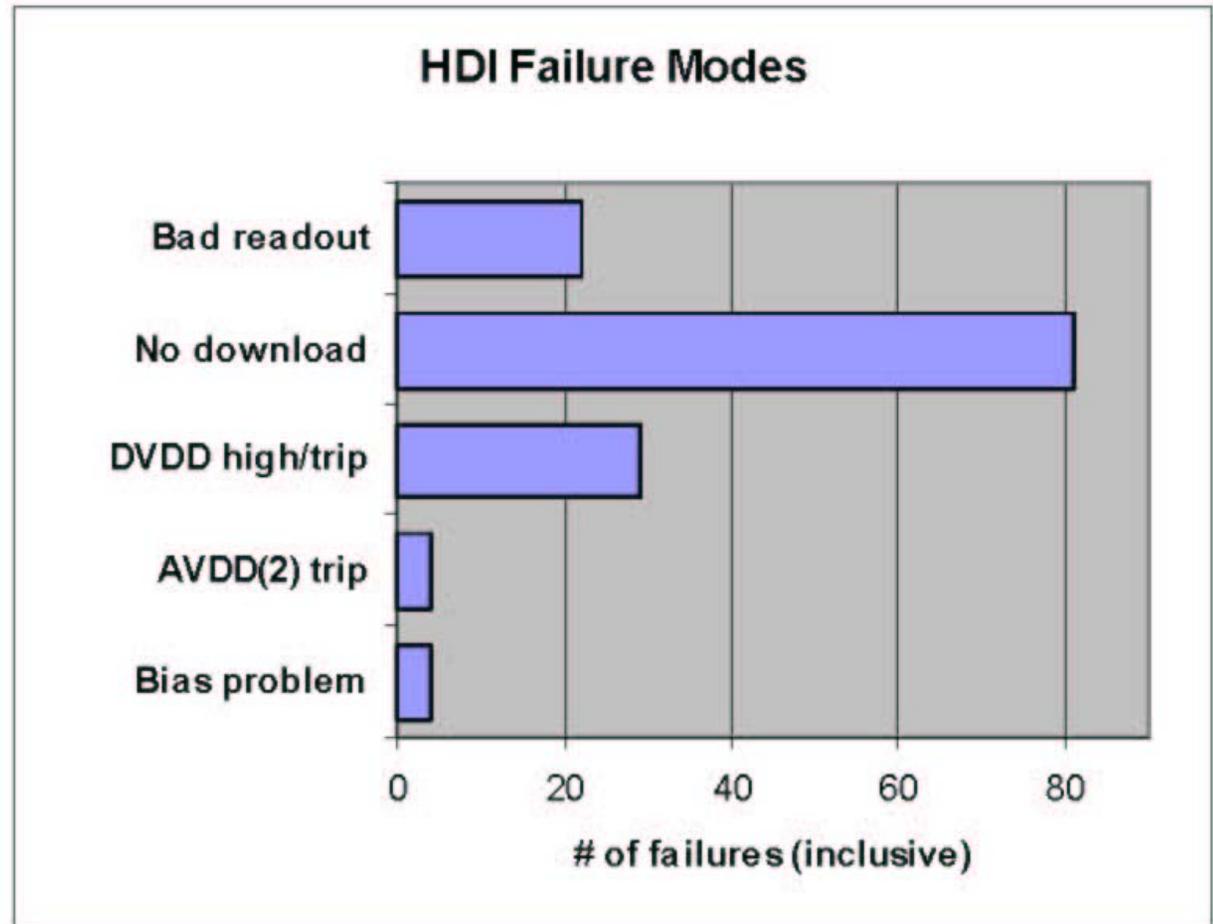
HDI Failure Modes

The ratio of "no download" to "bad readout" may be a clue to the cause of some failures.

As recently pointed out by Marvin Johnson, it should be about 1 based upon the number of connections required for functionality.

In addition, he noted that the failure rate of SVX-II chips used for fiber tracker readout has been ~ 1.2% of installed chips and the ratio is about 1 for those devices.

Emphasis during the present shutdown will be given to understanding the causes of failures.





Locations of Disabled Ladders

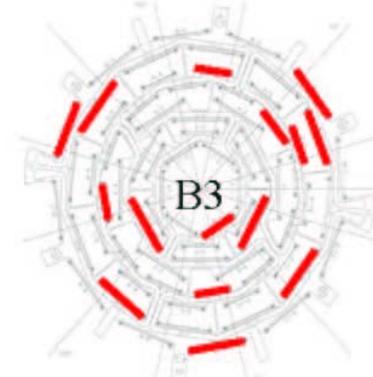
$6/72 = 8\%$



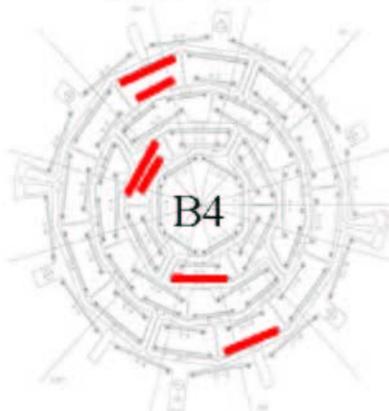
$7/72 = 10\%$



$15/72 = 21\%$



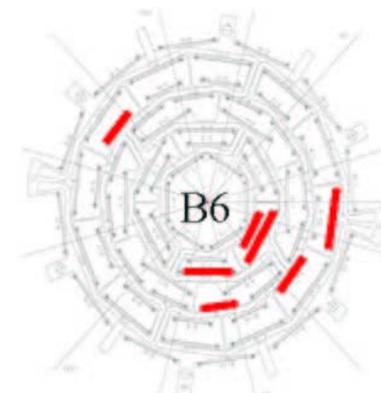
$6/72 = 8\%$



$10/72 = 14\%$



$7/72 = 10\%$



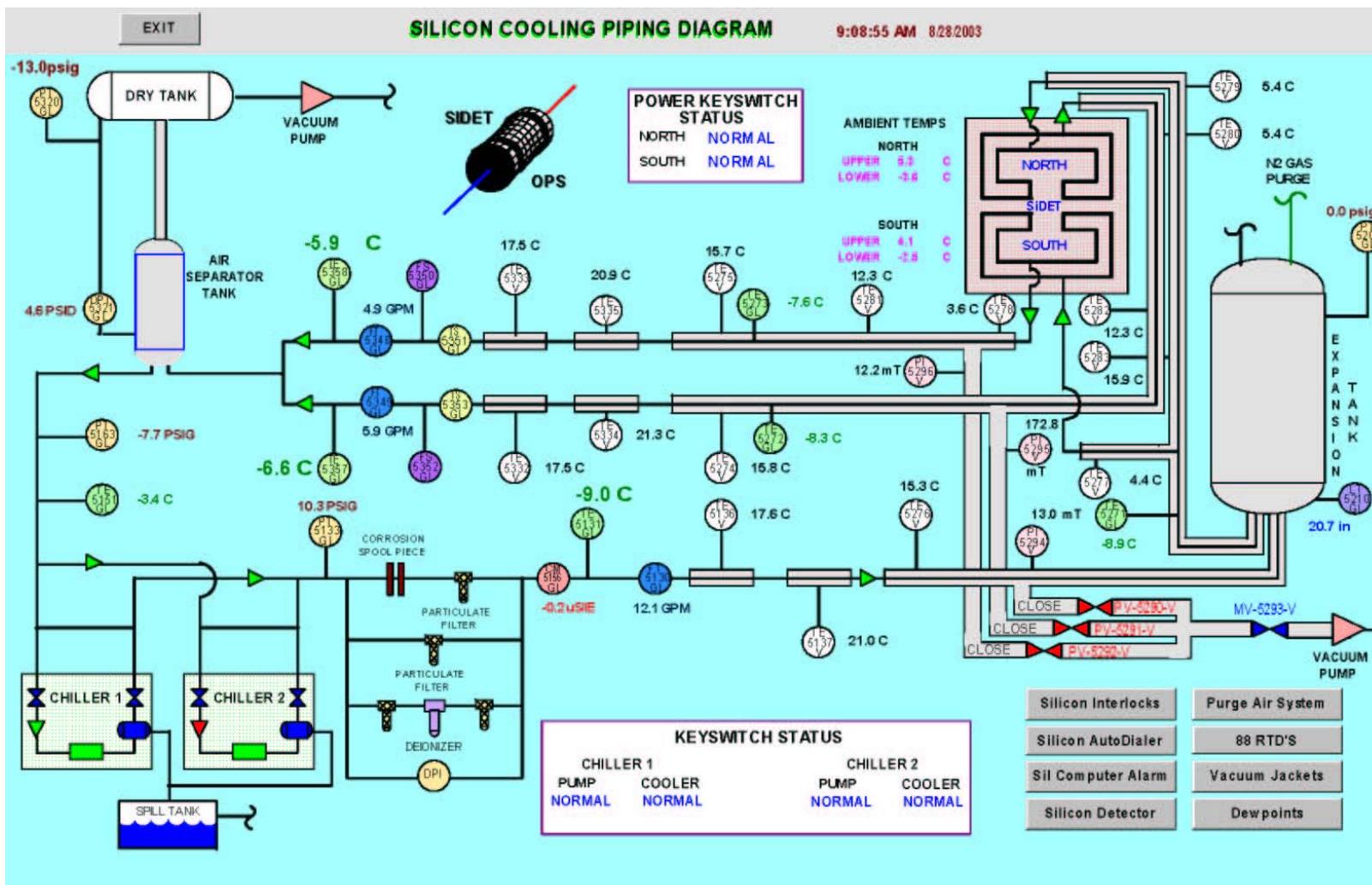


Run IIa Silicon Cooling

- The Run IIa cooling system has performed as designed.
 - ◆ It employs single-phase flow of a -8°C , deionized, ethylene glycol - water mixture with a freezing point of -15.3°C . One operating and one standby air-cooled Freon chiller are available for refrigeration.
 - ◆ Coolant is drawn through beryllium cooling passages of the silicon from a reservoir maintained at atmospheric pressure but purged with dry nitrogen. The pressure at the silicon tracker is approximately 0.6 atmospheres.
 - ◆ Elevation differences partially compensate frictional losses and lead to a pressure of 0.3 atmospheres at chiller pump suction.
 - ◆ Chiller pumps, heat exchangers, and coolant lines are insulated from ground to minimize the possibility of beryllium corrosion.
- The system was designed for simplicity of operation with minimal controls.
 - ◆ Chillers are in the assembly hall for easy access.
 - ◆ One supply line and two return lines run from the chiller skid into the collision hall.
 - ◆ All lines from the chiller skid to the fiber tracker, within which the silicon sits, are vacuum insulated stainless steel.
 - ◆ Silicon temperature is set by the chiller temperature control.
 - ◆ Flows from north and south silicon are set by manual valves and rotameters on the chiller skid. Once set, no changes have been needed.



Online Cooling System Display





Run IIa Silicon Cooling

- Duplicate compressors and duplicate air driers, with cylinder and tube-trailer back-up, provide dry purge air flow.
 - ♦ Dew points are measured via sample lines from 10 locations within the silicon enclosure. Redundant dew point measurements are made in the dry air supply lines, also. The dew points at the silicon range from -50°C to -65°C .
- A cooling and dry gas system permit is required for silicon power to be on.
 - ♦ Primary silicon protective devices (flow switches, pressure switches, temperature switches) are hard-wired for redundant and fail-safe operation.
 - ♦ Monitoring and secondary protection rely on an industrial PLC, which is part of the DO cryogenic control system. At least one cryogenic operator is on duty.
 - ♦ Tertiary protection is provided by the silicon readout system. Temperature sensors incorporated in HDI's automatically disable the HDI's individually. Over-current protection is provided individually.
- The chillers, compressors, and interlock system have generator back-up to address power outages. The interlock system has an uninterruptible power supply.
 - ♦ We deliberately chose to require that an operator restart the chiller and reset the interlocks manually after a power interruption. Chiller restart is accomplished by pressing and holding the chiller start button until flow switches are satisfied (< 5 seconds). The interlocks are made up by pressing a button on a nearby panel.



Run IIa Silicon Cooling

- Silicon permit panel and chiller enclosure.
- Chillers are at the left and right towards the back.



- Foreground: ion exchange resin vessel, filters, rotameters and electronic flow meters, pressure gauges and sensors.
- Background: suction buffer tank and air separator, chiller (view obstructed)

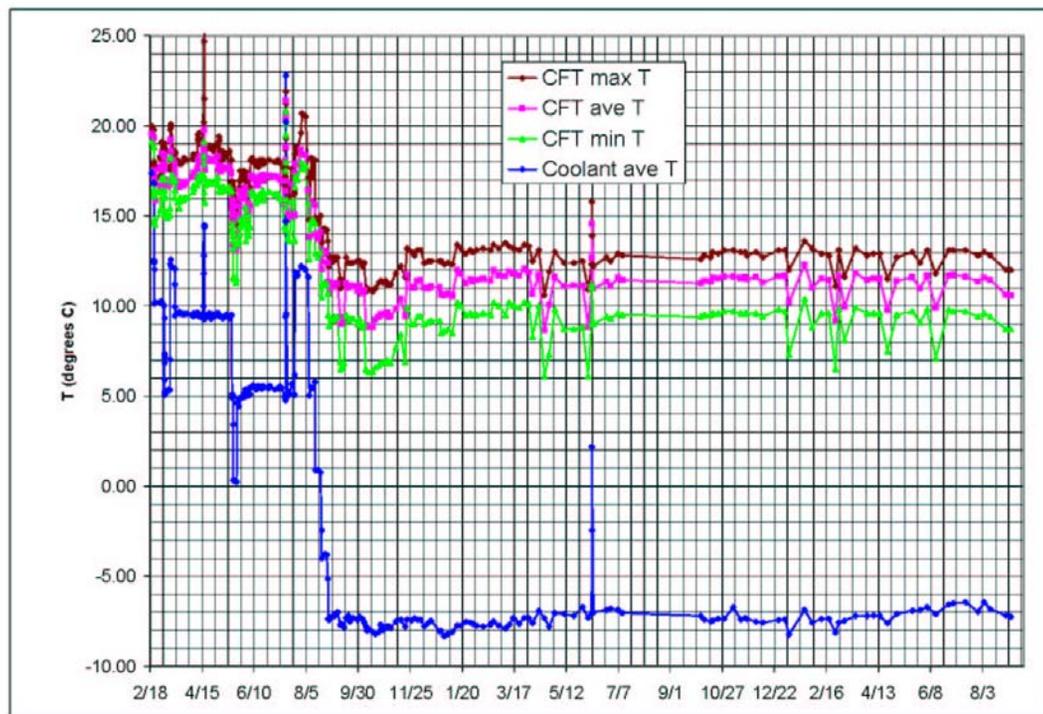




Run IIa Silicon Coolant Temperature

- The silicon and the fiber tracker reside within a space bounded by the vacuum vessels of the central calorimeter, the superconducting solenoid, and the end calorimeters.

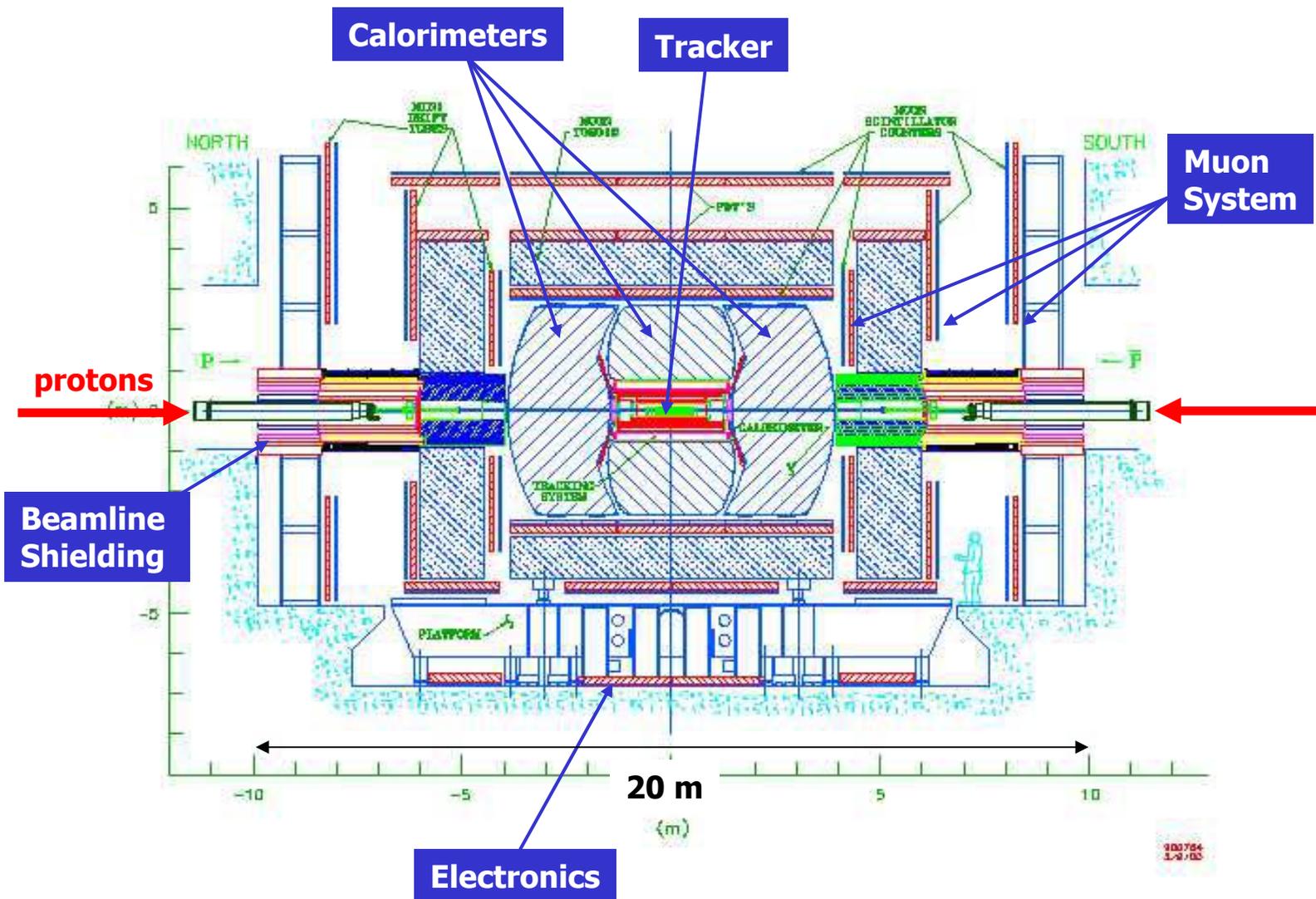
The central fiber tracker (CFT) must be kept sufficiently warm to ensure good light transmission through optical couplings from the scintillating fibers to clear waveguides. Scintillating fibers contract as temperature is lowered; carbon fiber support structures do not.

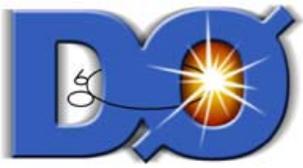


Dry gas purge flow between silicon and CFT ~ 1330 slpm.



Hermeticity of Run IIa Silicon

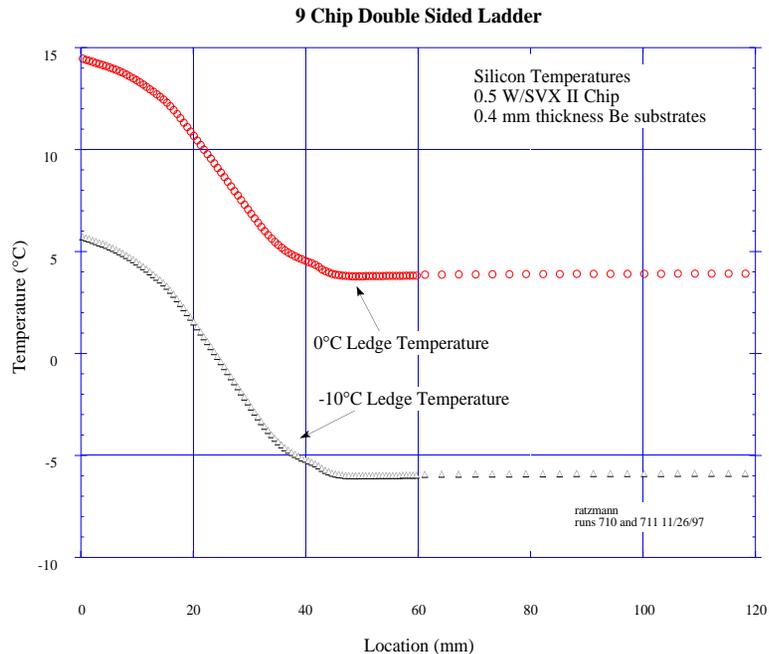




Run IIa temperatures

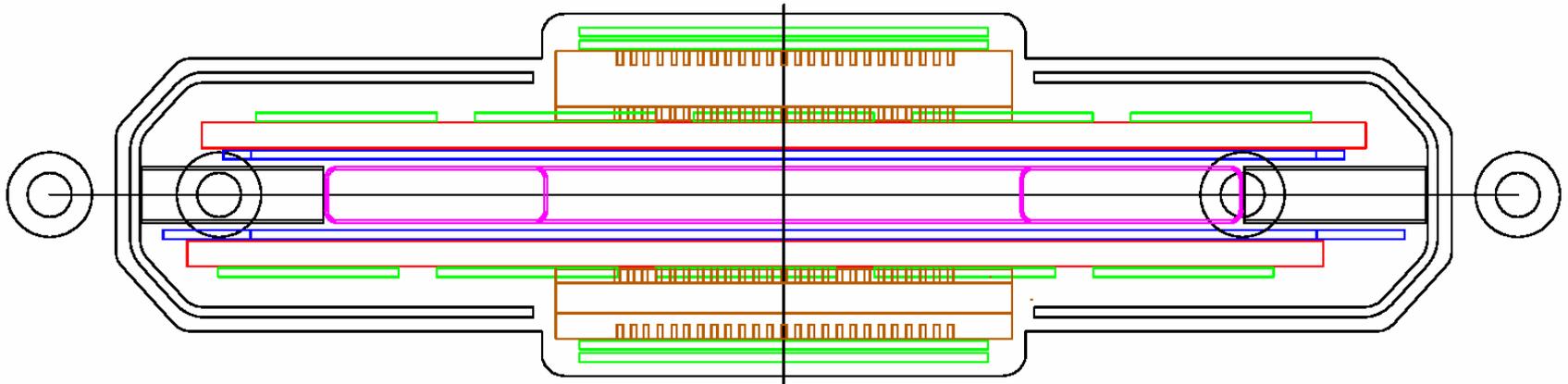
- HDI power dissipation averages ~ 0.43 watts per chip.
- With -8°C coolant, average silicon temperature of ladders is $\sim -3^\circ\text{C}$.
- Maximum silicon temperature, near the end of a ladder, is $\sim +3^\circ\text{C}$.
- Coolant temperature rise through the silicon region is about 1°C .

Predicted
temperatures of
Run IIa ladder
silicon





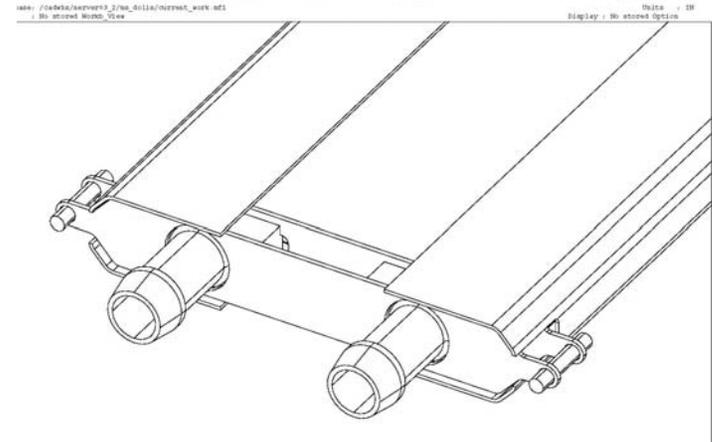
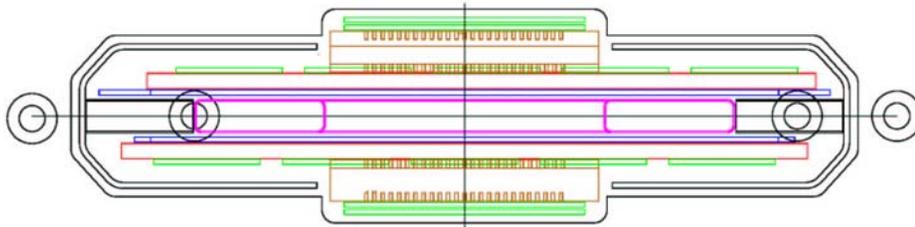
Run IIb L2-L5 Stave End View



- In this picture (L3 or L5), the axial sensors (blue) are on the top surface and the stereo, on the bottom.
- In L2 and L4, the opposite stereo sense is obtained by rotating the staves 180° about their longitudinal axis. L2 and L3 staves are identical as are those of L3 and L5.
- Digital cables run along the stave outer surfaces from connectors on the hybrids to (and beyond) the $z = 605$ end of each stave. All cooling connections are at the $z = 605$ mm end.
- Pins at $Z = 0$ and $Z = 605$ mm locate the stave. The $Z = 0$ pins are offset so that the pins of north silicon miss those of south silicon.
- The stave structure is nearly symmetric about its central plane. That minimizes thermal bowing.



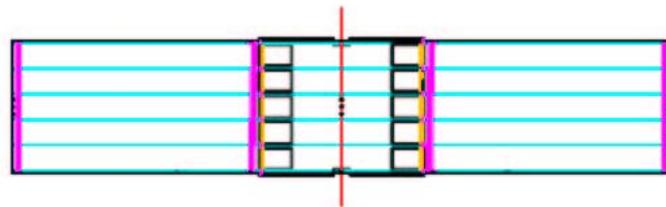
Layer 2-5 Staves



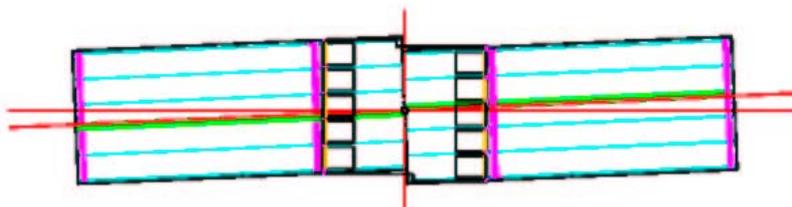
- The central core, with a formed PEEK cooling tube is fabricated first. Structures at the ends of the stave core integrate the core with stave locating pins, cooling tube nozzles, and C-channels.
- In a coordinate system based upon the positioning pins, four previously fabricated sensor-hybrid modules (two per surface) are positioned on the core and glued to it.
- The C-channels, which provide structural stiffness, are added.
- Stave weight, including a relevant portion of cables, = 145 grams.
- Maximum gravitational deflection, with simple support at pins, = 49 μm .
- Average thickness \sim 2% of a radiation length at normal incidence.



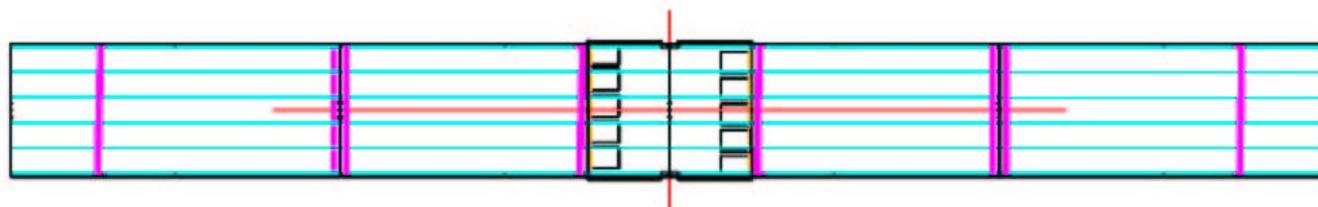
Run IIb Hybrid - Sensor Layout



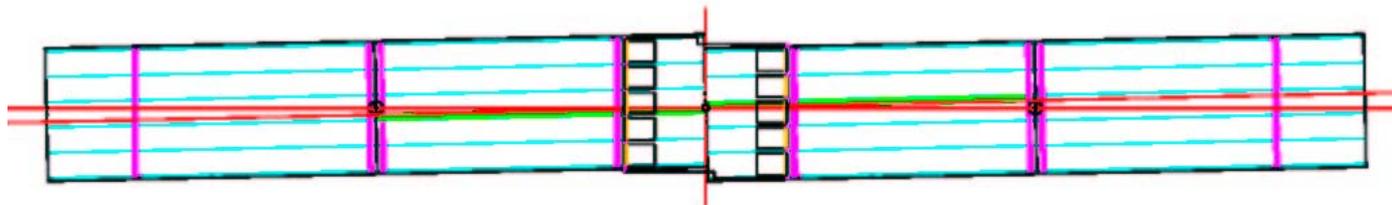
200 mm axial



200 mm
2.48° stereo



400 mm axial



400 mm
1.24° stereo



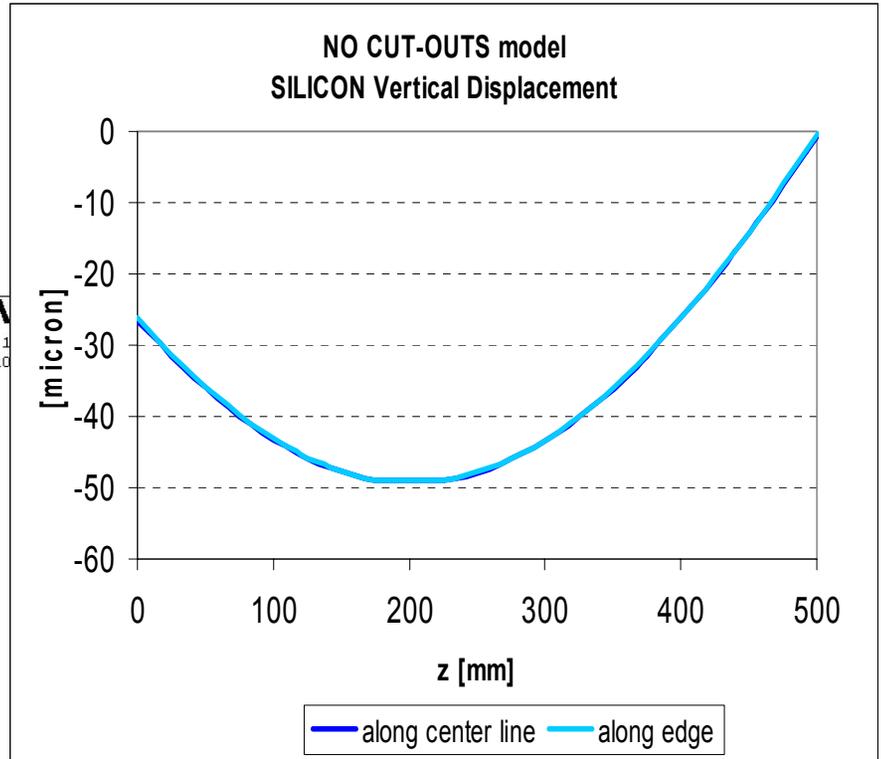
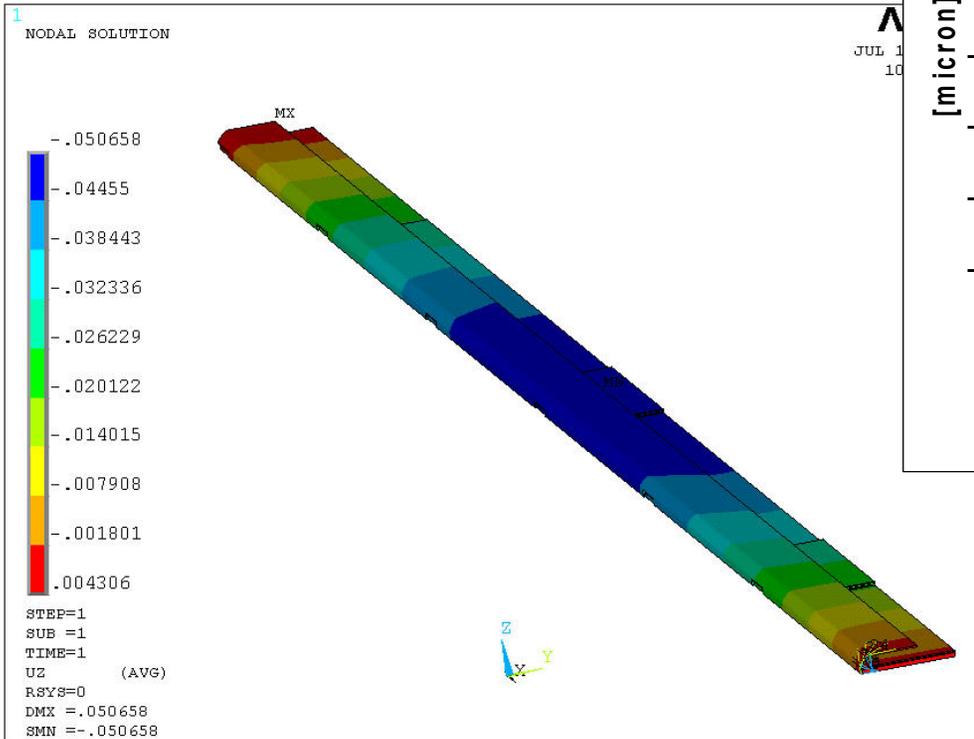
FEA for Run IIb Staves

Units in mm

Restraints on 4 end node

$z = 0$ mm, free to slide longitudinally

$z = 600$, clamped

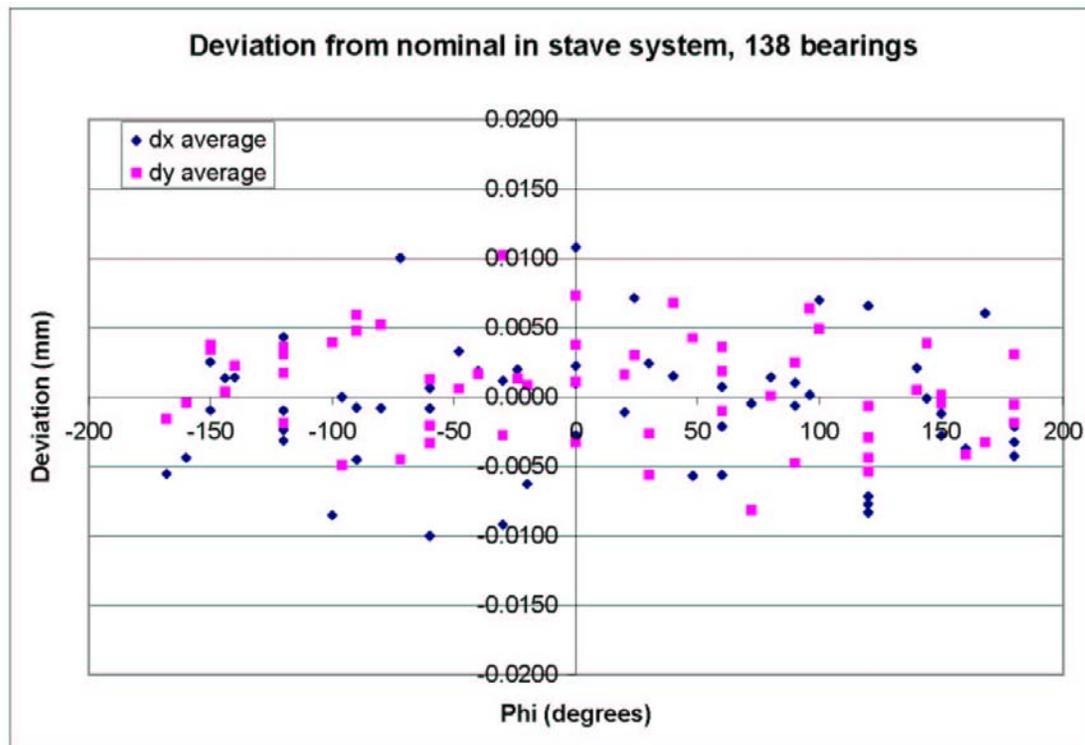
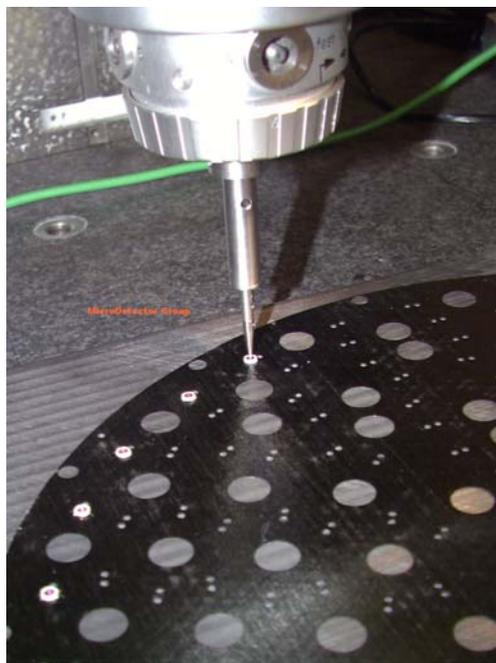


Giobatta Lanfranco
SiDet Mechanical Engineering Group
Fermilab



Run IIb Stave Positioning

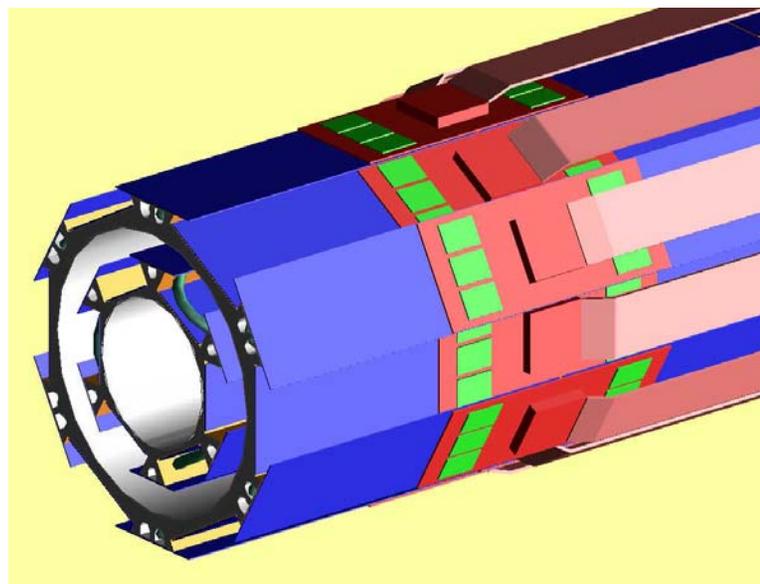
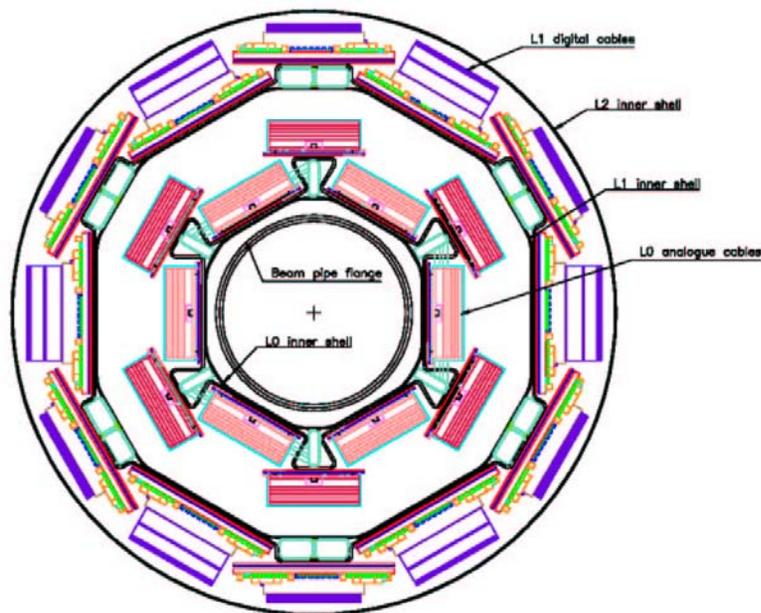
- Sapphire pins and bearings at each stave end position the stave relative to the carbon fiber - epoxy bulkheads of the support cylinder



The use of a coordinate measuring machine to install and position stave locating bearings. The layer 0 and 1 structures are joined and located within layers 2-5 using similar pins and bearings.



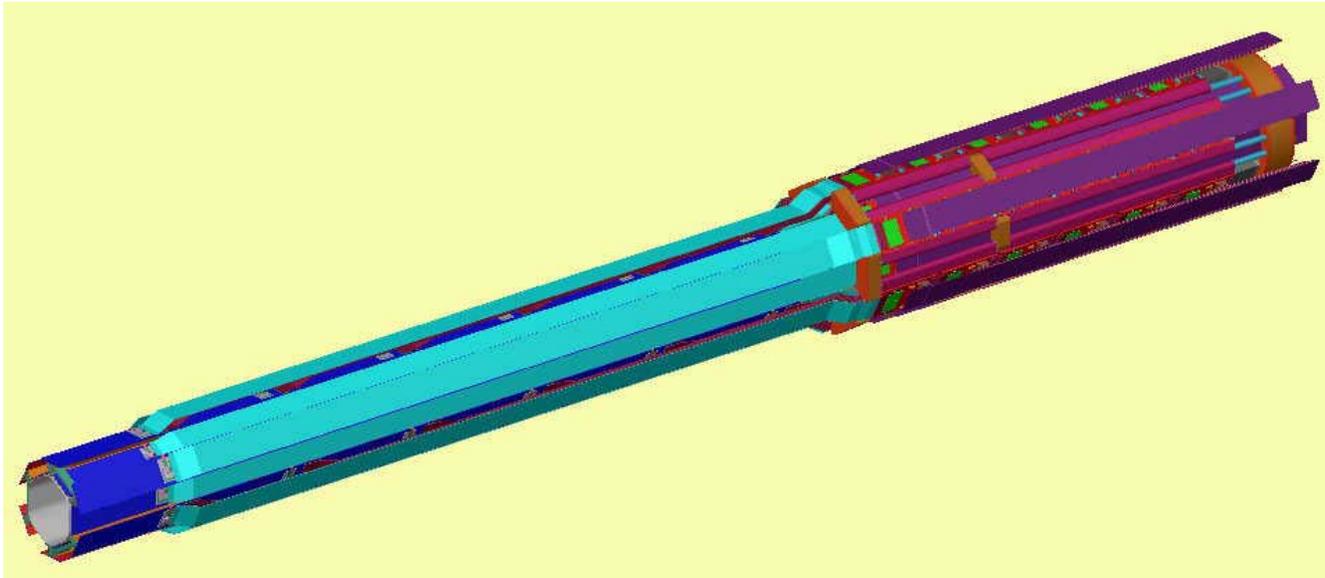
L0 - L1 (University of Washington)



- Sensors at twelve azimuthal positions and two radii for each layer
- Support is via carbon fiber reinforce epoxy cylinders
- The outer cylinder is castellated to provide the two radii
- The inner cylinder is either round or hexagonal
- Support for the cylinders is at $z = 0$ and $z = 61$ cm
- In the sensor region, $L0 \sim 1.6\%$ of a radiation length at normal incidence
- In the sensor region, $L1 \sim 2.4\%$ of a radiation length at normal incidence



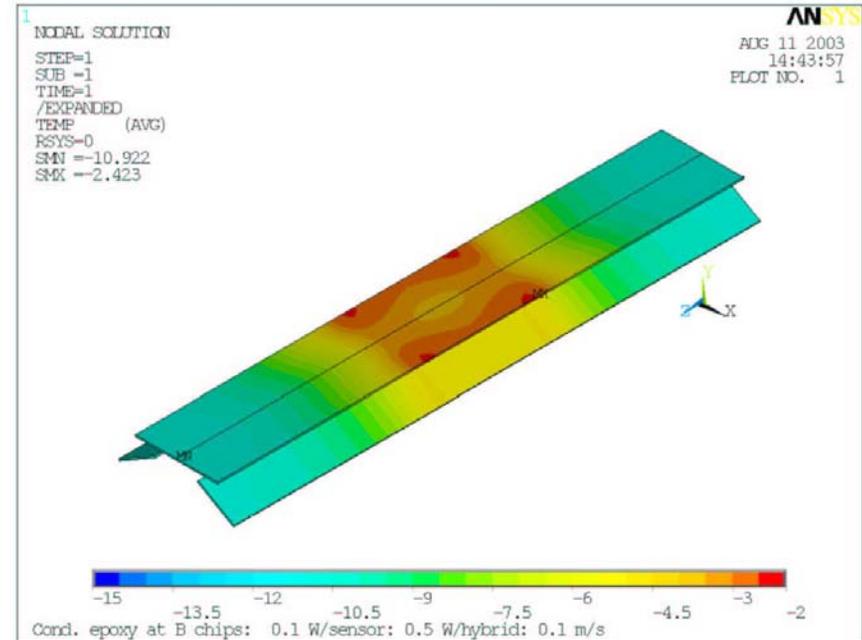
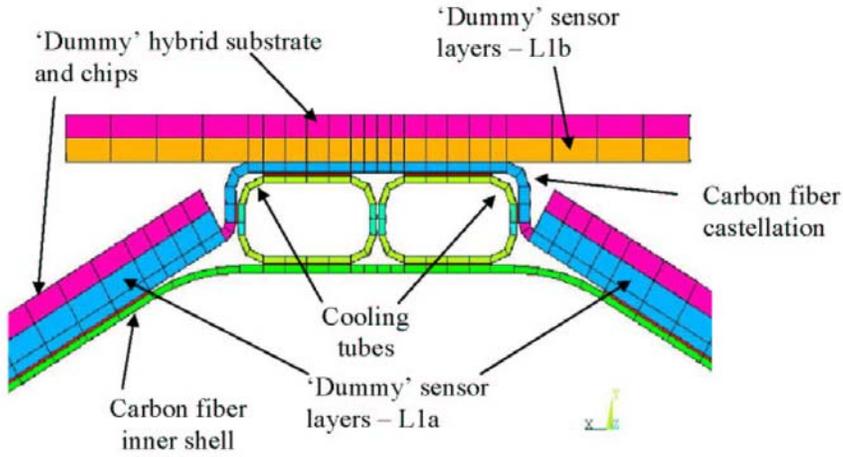
LO Geometry



- Hybrids are located at the end of the sensor region and connected to the sensors via analogue cables
- Independent cooling is provided for the sensors and the hybrids to simplify heat removal from the silicon. A maximum silicon temperature below -10 C is easily achieved.



L1 Thermal Studies (UW)



- FEA calculation of the temperature distribution at one of eighteen identical sensor – hybrid module locations. The maximum silicon temperature is -2.4°C with an inlet coolant temperature of -15°C . A coolant flow velocity of 0.1 m/s was assumed.



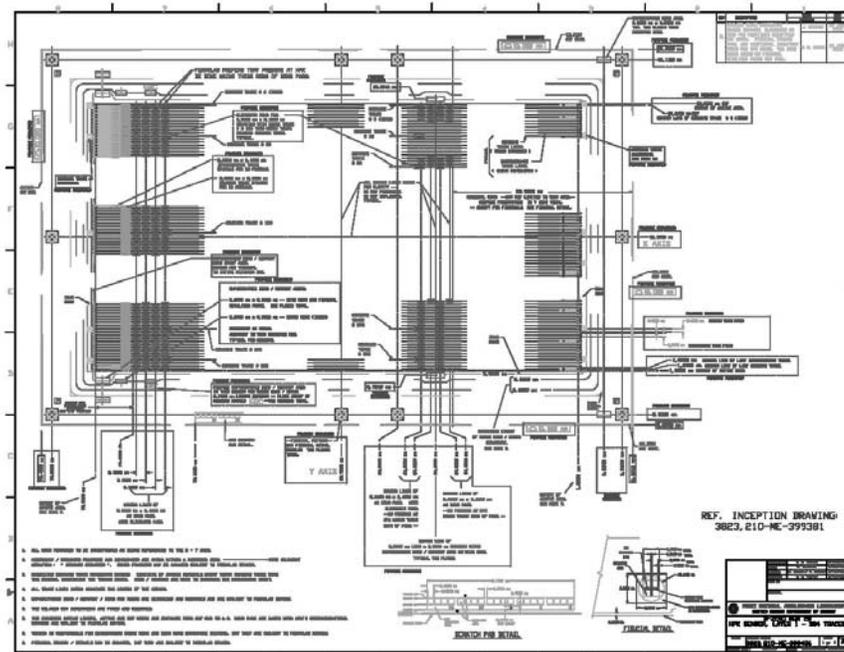
Run IIb Sensors

- Sensor procurement was to be based upon written sensor specifications (Regina Demina, Frank Lehner), sensor drawings, and qualification of the vendor and the design via the testing of prototypes.
- Prototype testing included visual inspections, electrical (probe station) testing, irradiation, and mechanical testing.
- This process was completed for L1 and L2-L5 sensors. Qualification of a vendor for L0 sensors was based upon L1 results.

Sensor website:

www.physik.unizh.ch/~lehnerf/dzero/run2b.html

Typical Fermilab sensor drawing (L1). HPK also provided fabrication drawings to allow us to verify concurrence in the design.





Run IIb: Sensors (2)

- All Run IIb sensors are single-sided to provide high radiation hardness for the tracker.
- Three sensor varieties: 2-chip, 3-chip, and 5-chip
 - ◆ The 2-chip (50 μm pitch) and 3-chip (58 μm pitch) sensors of layers 0 and 1 are positioned with no stereo angle.
 - ◆ The 5-chip sensors (60 μm pitch) of layers 2 through 5 are supported in stave structures with stereo angles obtained by rotating the sensors.
 - ▲ Stereo angle = 2.5 degrees for modules closer to $Z = 0$
 - ▲ Stereo angle = 1.25 degrees for modules further from $Z = 0$.
- Based upon vendor qualification, all Run IIb sensors were planned to be obtained from HPK.
 - ◆ All have intermediate strips.
 - ◆ Delivery of L2-L5 sensors has begun.
 - ◆ Procurement of L0 and L1 sensors has been postponed.

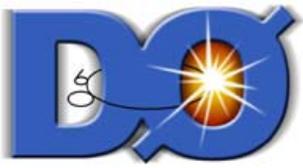


Run IIb Sensors (3)

- HPK L2 - L5 sensor deliveries have been on schedule.

HPK Sensor Delivery Schedule

| Month | Type | L1 | L2-L5 | Total |
|----------------|------|-----|-------|-------|
| | L0 | | | |
| April 2003 | | | | |
| May 2003 | | | | |
| June 2003 | | | | |
| July 2003 | | | 130 | 130 |
| August 2003 | | | 130 | 130 |
| September 2003 | | | 270 | 270 |
| October 2003 | | 110 | 270 | 380 |
| November 2003 | 50 | | 270 | 320 |
| December 2003 | 50 | | 270 | 320 |
| January 2004 | 60 | 106 | 270 | 436 |
| February 2004 | 56 | | 270 | 326 |
| March 2004 | | | 400 | 400 |
| April 2004 | | | 400 | 400 |
| May 2004 | | | 55 | 55 |
| June 2004 | | | | |
| July 2004 | | | | |
| | | | | |
| Total | 216 | 216 | 2735 | 3167 |



Run IIb Readout

- Hybrid design has been led by Andrei Nomerotski, with assistance from Kazu Hanagaki, Marvin Johnson, and Mike Utes
 - ◆ Mechanical input from Jim Fast and myself
 - ◆ Vendor interfacing by George Ginther and Johnny Green
- Extensive studies of grounding and shielding have been conducted by Marvin Johnson and Kazu Hanagaki.
- Frank Lehner worked with Dyconex to develop fabrication techniques for analogue cables.
- SVX-4 chips were developed by LBL and Ray Yarema's group at Fermilab.
- Kansas State University was responsible for adapter cards, junction cards, cables other than those at the silicon, and interface boards.
- Linda Bagby organized cable mapping for readout and trigger and plans associated with readout infrastructure and installation.

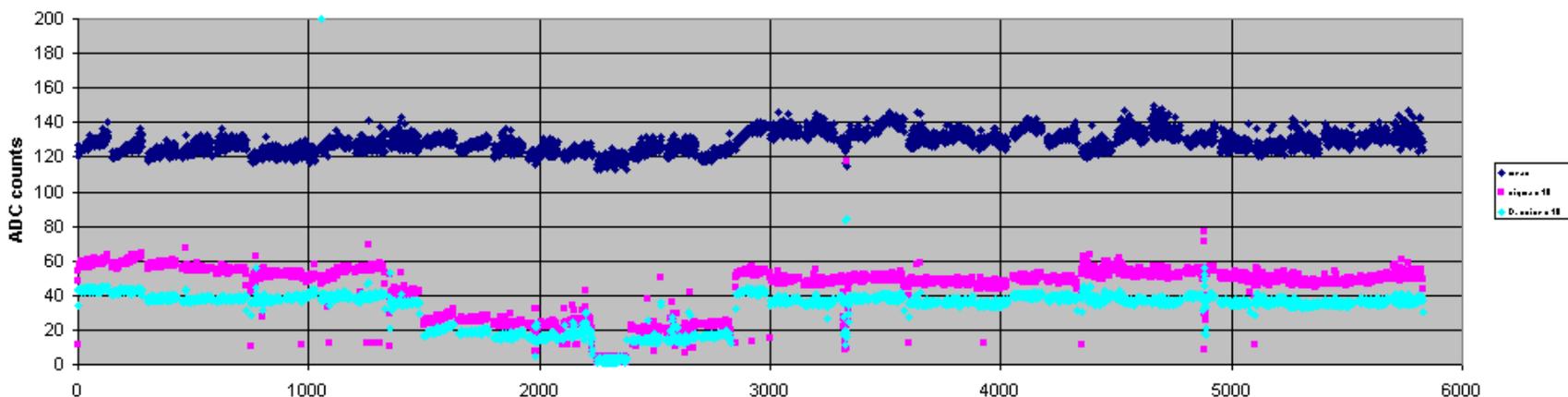


Run IIb Layer 2-5 Electrical Stave

- A layer 2-5 stave was successfully read out on 2 September 2003.



Stave 001: 20-20A, 20-20S (full chain rev. 2), 10-10S, 10-10A (full chain rev. 1). 14% readout errors (caused by rev. 1 chain)



Pedestal, total noise ($\times 10$), and differential noise ($\times 10$) with no sensor bias, one faulty test system connector, and no effort to reduce noise. (Courtesy of Kristian Harder)



Thoughts on Modified Run IIa Silicon

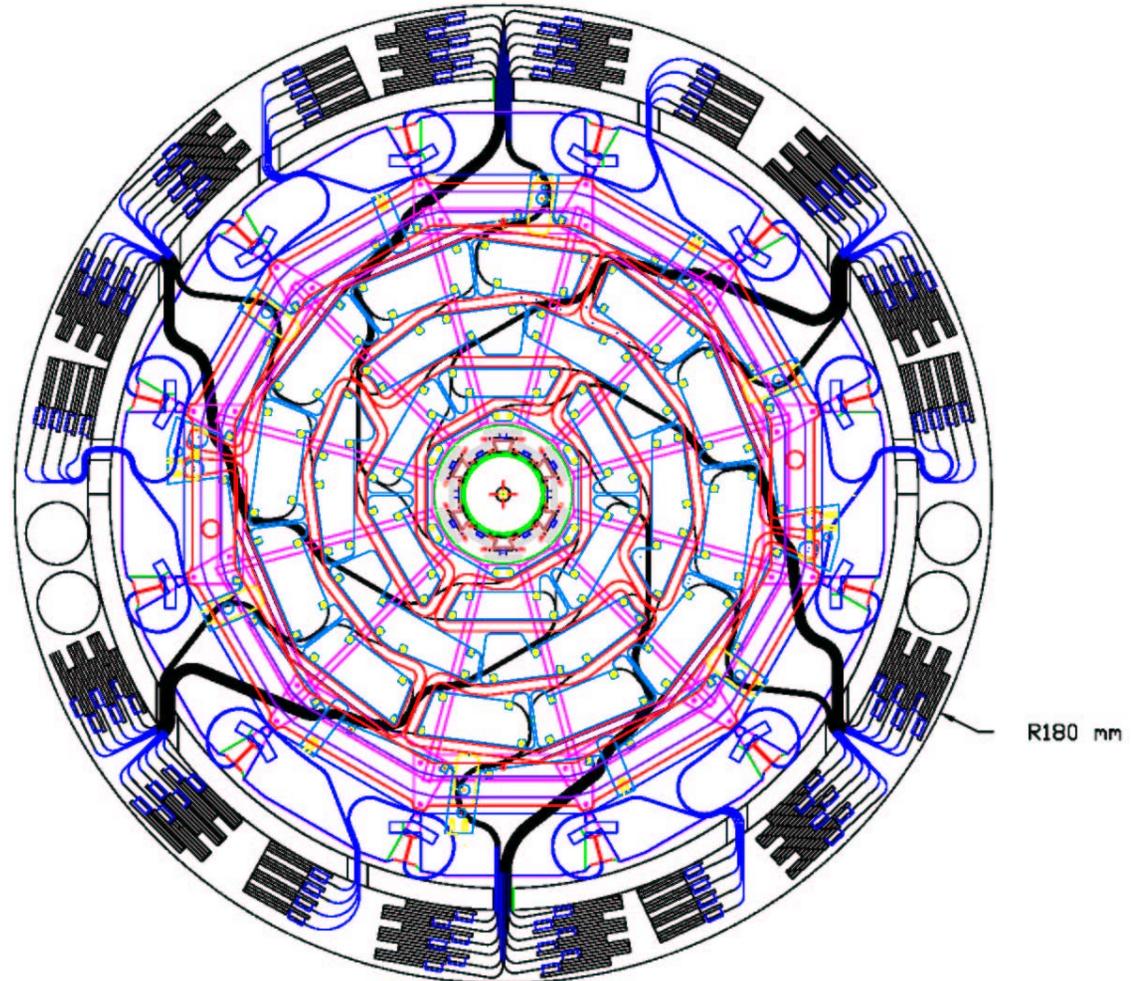
- New layer 0 within Run IIa silicon

Not yet at the proposal stage

To be discussed during the next few weeks

Many design details remain to be developed and investigated.

That is necessary before we will have confidence that an inner layer will fit.





Modified Run IIa Silicon (2)

(Still needs to be made more compact)

Run IIa layers 1-4

Run IIb beam pipe

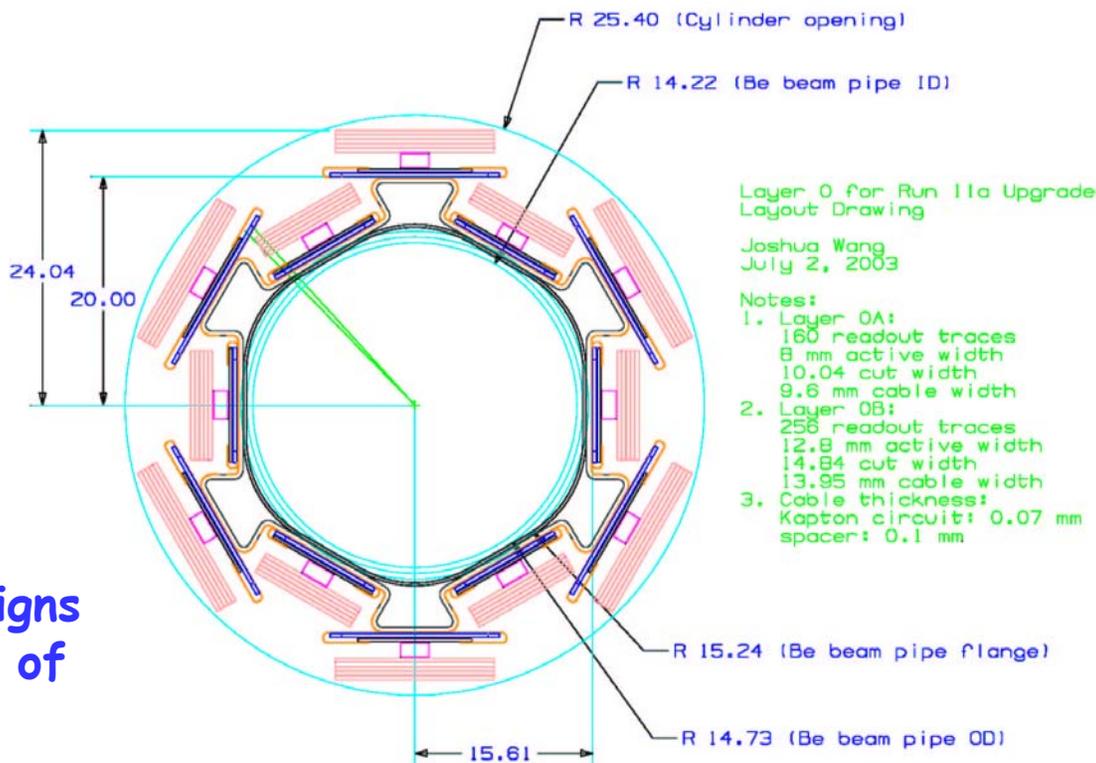
Additional 30K channel layer 0 with silicon radii of approximately 15.77 mm and 20.16 mm

Readout with Run IIa SVX-IIe chips

Layout & support follow designs developed by the University of Washington for Run IIb

Layer 0A sensor: pitch = 50 μm , width = 160 channels

Layer 0b sensor: pitch = 50 μm , width = 256 channels



Alternative for Layer 0A: pitch = 62.5 μm , width = 128 channels



Summary

- Run IIb silicon

- ◆ The design is essentially complete. All known technical issues have been addressed.
- ◆ Sensor designs and irradiation of prototype sensors have been completed. HPK deliveries of layer 2-5 sensors have been on time.
- ◆ The development of SVX-4 chips has been highly successful.
- ◆ Reliable analogue cables have been developed and tested for LO.
- ◆ Prototypes of staves, bulkheads, and layer 0-1 structures have progressed well.
- ◆ Hybrids, mechanical staves, and electrical staves have been fabricated and tested successfully.
- ◆ The cable mapping for readout and trigger has been determined.
- ◆ A plan allowing installation in fourteen weeks has been developed.
- ◆ While this silicon tracker will not be built, we believe its design is sound and may be helpful to others.



Summary (2)

- Run IIa silicon

- ◆ Silicon alignment based upon tracking agrees well with predictions from design and fabrication.
- ◆ Silicon impact parameter resolution is good.
- ◆ The silicon cooling operates as planned and has been reliable.
- ◆ Significant effects from fluence are not yet clearly seen.
- ◆ The readout system requires regular attention.
- ◆ Preliminary designs to add an inner, fifth layer are being considered.
- ◆ DO will make a concerted effort to maintain and improve the Run IIa silicon tracker, and to utilize its full potential for physics at the Tevatron.